A Study on the SEU in the SRAM to proton Irradiation

Young Hwan Lho, Bo Kyun Park, and Bong Sun Kim

School of Computer, Electronic & Communication Engineering
Woosong University, Daejon, Korea 300-100
(Tel: +82-42-630-9702; E-mail: yhlho@lion.woosong.ac.kr)

Abstract: The major problem encountered in satellite design is EMI (Electro-Magnetic Interference) and EMC (Electro-Magnetic Compatibility). Here, our focus is on the effects of protons on the electronic system. The SEU (Single Event Upset) results from the level change of stored information due to photon radiation and temperature in the space and the nuclear power plant environment. The impact of SEU on PLD (Programmable Logic Devices) technology is most apparent in ROM/SRAM/DRAM devices wherein the state of storage cell can be upset. In this paper, a simple and powerful test techniques is suggested, and the results are presented for the analysis and future reference. The test results are compared with that of JPL test report. In our experiment, the proton radiation facility available at KIRAMS (Korea Institute of Radiological Medical Sciences) has been applied on a commercially available SRAM manufactured by Hynix Semiconductor Company.

Keywords: SEU, SRAM, proton, radiation

1. INTRODUCTION

The radiation hardening parts are to be used for satellite and nuclear power plant since there exist various kinds of radiation particles in space and radiation environment. For the past 40 years, the countries with advance of radiation technology are doing research in the field of radiation effects of passive and active components for electronic circuit mainly for space and defence. The researchers in these countries have been sharing many reports that lead to exchanges of radiation technology. However, the level of the technology in Korea is far behind and it is the time for all researches to focus our attention. In order to subject the components and the circuits in the radiation environment, we need the radiation simulation facility. The types of radiation are generally divided into particle radiation and photon radiation. The particle radiation consists of the charged particles which have protons, electrons, α particles, ions, and neutral particles that are the neutrons.

When an energetic nuclear particle penetrates any semiconductor material, it loses energy through Rutherford scattering with the semiconductor lattice structure. Unlike total dose radiation [1, 2] which causes gradual global degradation of device parameters and dose-rate radiation which causes photocurrents in every junction of a circuit, a single event interaction is a very localized effect, and can lead to a seemingly spontaneous transient within a region of the circuit. If this transient influences a node which is storing information, it may lead to an upset; that is, the corruption of the information to an unrecognizable, unreadable, or unstable state.

TID (Total Ionizing Dose) can be caused by either the natural environment such as electrons or protons trapped in the Van Allan Belts [3] or by x-rays and gamma rays, engendered by a nuclear weapon detonation, impinging on a semiconductor device. The Van Allen belt is a region of charged particles trapped by the earth ' s magnetic field. The region closest to earth is composed mainly of protons, while electrons extend out to 35,000 miles. In most cases, Van Allen protons and electrons consist of the primary classical radiation problem for spacecraft. The maximum proton fluxes are about 10^4 protons/cm^2; this converts to 0.001 rad/sec. The electron flux is around 10^{10} electrons/cm^2; this changes to about 0.028 rad/sec at the worst altitude. In case the solar flares occur, the proton flux may increase several orders of magnitude for a few days.

SEE (Single Event Effects) can be engendered by the impact of either heavy ions or energetic protons and neutrons, that occur naturally in space or the atmosphere, on sensitive areas in microcircuits in nuclear power plant. These particles deposit ionizing energy into the circuit that can cause either a 'soft' or non-permanent error or, in some cases, permanent damage to the circuit. Concerning PLD technology, the most important SEEs are SEU (Single Event Upset), SEL (Single Event Latchup), SEB (Single Event Burnout), SET (Single Event Transient), and SED (Single Event Disturb), etc.

2. SEU IN SRAM

When it is caused by a burst of ionizing radiation from an extended source, it is generally referred to as a transient upset; when caused by a single energetic ion, it is generally referred to as a SEU. Memory data loss in a number of satellite systems has occurred because of cosmic-ray induced SEU in MOS memory circuits. Information is stored as charge, and the node storing the information comprises the gate node of one inverter and the output node of the other inverter in the cell. In a SRAM cell, the stored charge is continuously refreshed. For a single event, which affects only one information node of the SRAM cell, to reverse its logic state, the induced perturbation must exceed the restorative capability of the cell. Protons occur in every imaginable orbit with variations in spectral energy composition, arrival rates, and sometimes arrival trajectories. The three sources [3] are trapped protons in the inner Van Allen radiation belt, the proton component of solar particle events and hydrogen nuclei from intergalactic cosmic rays. The near-Earth, interplanetary, and other planet proton enviroment models are available in the notes [3]. In order to experiment SEU of the SRAM, the Cyclotron accelerator at KIRAMS is utilized. The capacity of the accelerator has the maximum energy of 50 MeV and the beam current is 3 nA to 60 uA.

A commercial SRAM, attractive candidate for space applications have been irradiated with energetic protons to study resulting single event upsets. Upsets have been measured individually for each of these types of storage elements for both one-to-zero and zero-to-one upsets. Upsets can cause a variety of malfunctions. Additionally, proton causes occasional memory logic state exceptions to be invoked, albeit with lower statistics.

3. IMPLEMENTATION OF TESTING CONTROLLER BOARD

The fundamental scheme of the micro-computer as shown in Fig. 1 can be thought as the small size of computer. The basic structure of computer is input, output, control, and memory equipment. The operation and control equipment constructs CPU. The circuit of micro-computer [4] executes the functions of processor with 8031 chip, latch dividing address and data, EPROM controlling processor, GAL setting memory map, SRAM in stand alone to be irradiated to proton, 8255 for extending the bus line, and FND counting the time and the number of upsets. The commands are come to CPU through the input equipment and are carried out. After the micro-computer completes the operation, the one sends the results to the output equipment. The 8031 is one-chip micro-computer with four kinds of input/output ports for 8 bits operation, clock generator of 11.0592 MHz, two 16 bits timer/counter (T0, T1) for 4 kinds of modes, and one serial communication port, which can be used input/output extension mode.

3.1. Hardware structure

1) Structure of 8051

The 8031 chip should use ROM outside the 8031 chip since it does not have ROM in 8031 itself. In case the output memory will not be used, all pins can be used for the common input/output mode. However, the output memory is used since 2 ports can be switched for bus operation in order to control the address and data bus.

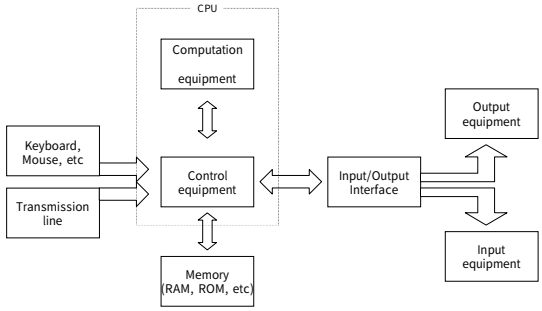

Fig. 1 Block diagram of a micro-computer

2) Address latch

The 74HC573 [4] is used for address latch. The port of OC (output control) is connected to ground, C (control) can be the state of '0' or '1'. The state of '0' makes the input signals to D1 ~ D8 ports be delivered to Q1 ~ Q8 as the output, and the one of '1'makes them keep up the previous data. The D1 ~ D8 ports are connected to port 0 of CPU, and C (11) is to ALE port of 8051 processor. As the result, the address signal (port 0) is sent to Q ports through D port of 74HC573 and keeps the signal until the next signal of ALE comes in.

3) GAL16V8

The circuit of address decorder is used for establishing the memory map, which plays the role of assigning the addresses of the devices of ROM, RAM, or I/O to be used. Then, all devices can be executed by the assigned addresses. Here, the assignment of input/output equipment is called I/O map, assigning the memory address is accomplished by memory map. The circuit for choosing memory map is consisted of 'NOT', 'AND', 'OR' gate, and decorder (74LS139). The construction tends to be complex and needs more space in the board, and GAL (Gate Array Logic), which is one of PLD IC's, is utilized.

The functions of each pins [4] are defined as

Input: /RD, /WR, PSEN, A15, A14, A13, A12, A11, A10, A9

Output: /CS3, /CS2, /CS1, /CS0, LCD_EN, /RAM_WE, /RAM_OE, /ROM, CS

The kind of GAL can be chosen after confirming the number of input and output. Here, GAL16V8 is selected since the number of the input is 16 and that of output is 8.

4) SRAM

The product of SRAM(HY62CT08081E) is the kind of 62256, in which the memory size is 256 Kbit and the number of pins is 28. The pin number and the pin array is shown in the reference [4]. The SRAM has the function of Read/Write instead of Read which is used in EPROM/EEPROM.

3.2. Software structure

- 8051 test board header files supplied by Keil PK51 8051 C Compiler. The header files are for carrying out code, data, page, and outside memory.
- FND program assigning the addresses of 5 kinds of 7 segments
- 2 addresses of control register operate 2 kinds of 8255's, respectively
- Delay for representing time by FND
- Control input/output of 8255 after initializing

1) main program

- assigning data for representing number at segment
- calling 8255 function
- setting 300 seconds
- making operation program for counting the numbers of upsets by reading the memory ROM data outside
- writing data in FND
- adding program for writing data at RAM

2) GAL software

- burning the .JED file by ROM writer after creating the file through compiling by ABEL
- setting up input/output of PIN except Vcc is assigned to PIN20 and GND is PIN_10 as default
- controlling logic operation of addresses

4. EXPERIMENT RESULTS

The applied proton energy of the cyclotron accelerator is 25 MeV, and the beam current 1 uA and 3.1 uA, respectively. The proton is irradiated on the center of the chip of SRAM for 300 seconds. The testing controller board manufactured by the researchers at Woosong University, Korea, is surrounded by plumbum blocks to protect the proton particles of about 10^{13} particles/cm^2.

The energy of 25 MeV and the beam current of 1 uA is irradiated, the number of upsets is up to maximum of 8 for 290 seconds. The increasing shape is like the exponential curve as shown in Fig. 3. The energy of 25 MeV and the beam current of 3.1 uA is applied, the number of upsets is reached is to 9 for the shorter time of 5 seconds as shown in Fig. 4. The results agree with the linearity [5] as the duration of the applied beam goes by under the same energy.

Fig. 2 The testing controller board surrounded by plumbum (Pb) blocks at the Cyclotron accelerator

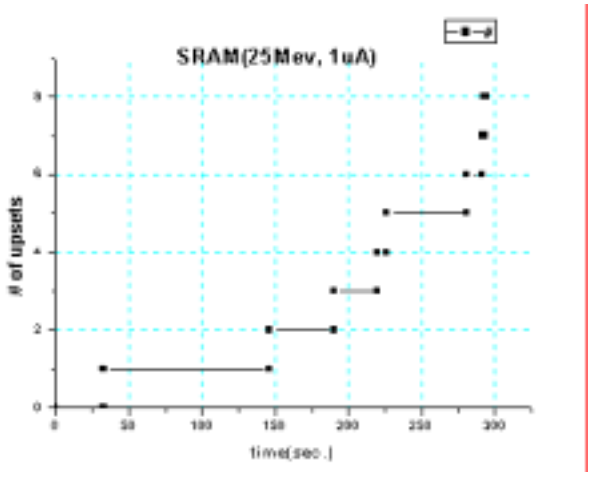

Fig. 3 Number of upsets (‘1’ ⇒ ‘0’) of SRAM under 25 MeV energy and 1 uA beam current

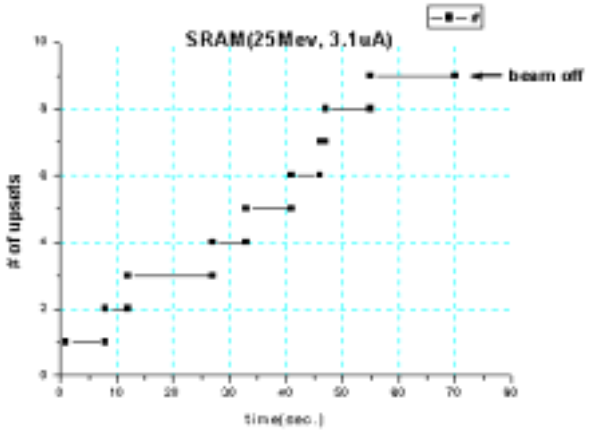

Fig. 4 Number of upsets (‘1’ ⇒ ‘0’) of SRAM under 25 MeV energy and 3.1 uA beam current

5. CONCLUSION

The testing controller board has been implemented with 8031 processor, and the number of upsets increases linearly as shown in Fig. 4 when the proton energy of 25 MeV and the beam current of 3.1 uA at the Cyclotron accelerator is applied to the commercial Hynix SRAM as the time goes by.

Under the test method, a simple self-inspection program for interface and operation is running during Proton irradiation. This result turns out to be quite successful.

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