A New Phase-Locked Loop System with the Controllable Output Phase and Lock-up Time

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Abstract: This paper, we propose a new phase-locked loop (PLL) system with the controllable output phase, independent from the output frequency, and lock-up time. This PLL system has a dual control loop is described, the inner loop greatly improved VCO characteristic such as faster speed response as well as higher operation bandwidth, to minimize the effect of the VCO noise and the power supply variation and also get better linearity of VCO output. The main loop is the heart of this PLL which greatly improved the output frequency instability due to the external high frequency noise coupling to the input reference frequency also the main loop can control the output phase, independent from the output frequency, and reduce the lock-up time of the step frequency response. The experimental results confirm the validity of the proposed strategy.

Keyword: Phase locked loop, Dual-loop feedback VCO, PI-controller, Frequency stability, Controllable the output phase, Reduce the lock-up time

1. INTRODUCTION

The voltage-controlled oscillators (VCO) are widely used in such application as phase-locked loops (PLLs), FM modulator, frequency synthesizers, timing recovery, and many others. The characteristic of the VCO are generally the most important in determining the overall system performance of the PLLs. Most of the researches about VCO is the attempt to improve the temperature stability of the VCO's frequency at high frequency [1-4]. The VCO phase noise in the PLL is not attenuated by the small bandwidth loop in the range of interest [5]. Thus, it is usually necessary to resort to an off-chip, high Q VCO. This results in higher power consumption, large size and more importantly, greater interference problems.

One technique to solve these problems is to use a closed-loop voltage-to-frequency converter architectures [6, 7]. This architecture can achieves a wide bandwidth for good VCO phase noise suppression. The another consideration on the PLL's characteristic is the lock-up performance which is one of the most important target items in designing PLLs. In a digital PLL, it is difficult to control the frequency and phase independently, which make it difficult to improve lock-up performance. A new PLL system with controllable the output phase and lock-up time is introduced here.

This PLL system has a dual control loop in which the inner loop is the VCO regulation system which composed of PI controller and phase-locked loop acted as the feedback part in order to convert the VCO output to be a voltage signal. The PI controller of inner loop is designed for optimum output response [8] of VCO and minimizing VCO noise disturbances and the power supply variation. In otherwise the inner loop is used to improve the characteristics of VCO, especially the nonlinearity at high frequency. The main loop is the heart of this PLL system, it has a two inputs signal, one is the reference frequency (Fref) input to be used for set-up the output frequency of the VCO. This input has the high noise immunity resulting from limited bandwidth of a low pass filter (LPF_2) to the external noise coupling at high frequency. The another input signal of this PLL system is the control input represented by a voltage signal in order to control the phase of the VCO output independently from the frequency output as well as reduction of the lock-up time of the system response. The PI controller of the main loop is designed for the optimum loop response [8] as well as minimizing the lock-up time. The validness of this PLL system is confirmed by experimental results.

2. DUAL-LOOP FEEDBACK CONFIGURATION OF VCO

The inner closed-loop VCO circuit is shown in Fig.1. An ordinary VCO is configured in a feedback loop which has a phase-locked loop acted as the feedback element for providing a voltage output of LPF that is proportional to the input frequency. The used phase-locked loop as the feedback element instead of a frequency-to-voltage converter (FVC) for some advantages of no need a large frequency division element (1/N) in the feedback part. In case FVC is used as the feedback element the output of VCO must be divided down to an intermediate frequency where a FVC could be easily designed. The another advantage when feedback by PLL, the wide bandwidth of closed-loop VCO is possible designed.

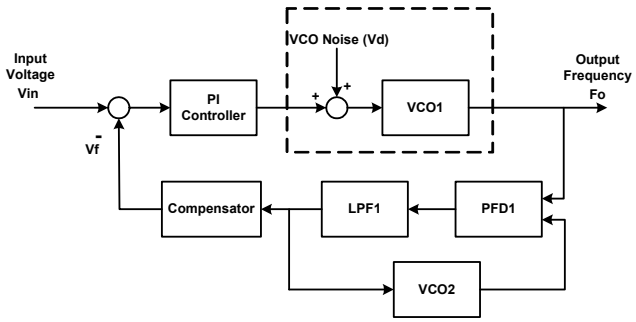


Fig.1 Shows the dual-loop feedback configuration of VCO.

In case the closed-loop VCO is feedback by PLL, the voltage output of LPF is passed through a compensator to be a feedback voltage (Vf), this voltage is subtracted from a forward part input voltage and the error signal is subjected to the PI-controller which is designed for close-loop VCO by mean of the symmetrical optimum [8] to minimizes the effect of VCO noise disturbance and to get the optimum output response.

From Fig.1, we can transform each element to be a transfer function in the frequency domain as shown in Fig. 2.

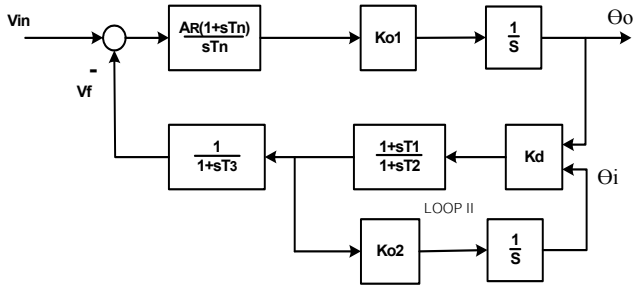


Fig.2 S-domain block diagram of the closed-loop VCO.

Where K_O is the VCO conversion constant in Hz/Volt, and K_d is the conversion gain of the PFD in volt/radian.
Fig.2 shows S-domain block diagram of the closed-loop VCO which has a PLL in the feedback part. A first we can simplify the block diagram of the loop no.II (PLL) to be an open-loop transfer function $(F_{o2}(s))$ and a closed-loop transfer function $(F_{c2}(s))$ respectively.

$$F_{o2}(s) = \frac{K_d K_{o2}}{s} \frac{(1+sT_1)}{(1+sT_2)} \tag{1}$$

From Eq. (1), the closed-loop transfer function is found as follow,

$$F_{c2}(s) = \frac{(1+sT_1)}{1+\frac{s(K_d K_{o2} T_2+1)}{(K_d K_{o2})}+\frac{s^2 T_2}{(K_d K_{o2})}} \tag{2}$$

From Eq. (2), we can reduce its order to be a equivalent transfer function $(F_{c2}^{*}(s))$ in the case of $K_d K_{o2} > T_2$

$$F_{c2}^{*}(s) = \frac{(1+sT_1)}{(1+sT_4)} \tag{3}$$

where

$$T_4 = \frac{(K_d K_{o2} T_2+1)}{(K_d K_{o2})}$$

Since the block diagram of Fig. 2 can be simplified as shown in Fig. 3 in order to use for designing the PI-controller of this loop.

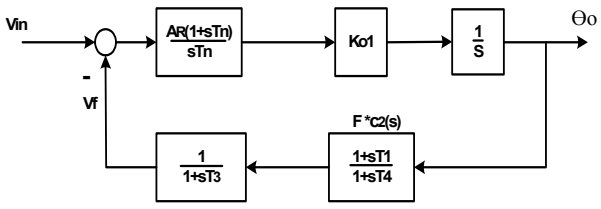


Fig.3 Shows the simplified block diagram of the close-loop VCO.

From Fig. 3, we can find the open-loop transfer function $(F_{o1}(s))$ and close-loop transfer function $(F_{c1}(s))$ as follow;

$$F_{o1}(s) = \frac{A_R(1+sT_n)}{sT_n} \cdot \frac{K_{o1}}{s} \cdot \frac{1}{(1+sT_4)} \tag{4}$$

where we let T_3 equal to T_1.
From Eq. (4), the close-loop transfer function is found as follow;

$$F_{c1}(s) = \frac{A_R K_{o1}(1+sT_n)}{A_R K_{o1} + sA_R K_{o1} T_n + s^2 T_n + s^3 T_n T_4} \tag{5}$$

From Eq. (5), the PI-controller $\frac{A_R(1+sT_n)}{sT_n}$ can be designed by symmetrical optimum method [8], the parameter of controller can be found as follow;

$$T_n = 4T_4,\ A_R = \frac{1}{(2K_{o1}T_4)} \tag{6}$$

3. A NEW PLL CONFIGURATION

When we combined the dual-loop VCO with the main loop which composed of a PFD_2, LPF_2, compensator and PI-controller, the new PLL configuration can be achieved as shown in Fig. 4.

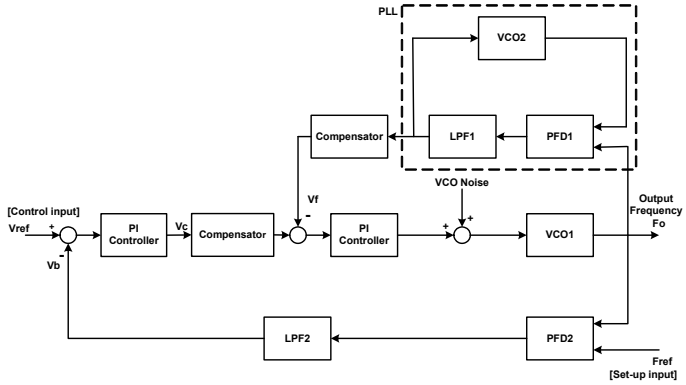


Fig.4 A new PLL system with controllable output phase and lock-up time.

In Fig.4 shows the new PLL system with controllable output phase and lock-up time. The main loop is the heart of this PLL system, it has a two input signal, one is the reference frequency (F_{ref}) input to be used for setup the output frequency of the VCO. This input has the high noise immunity resulting from limited bandwidth of a low pass filter (LPF_2) to the external noise coupling at high frequency. The another input signal of this PLL system is the control input represented by a voltage signal in order to control the phase of the VCO output independently from the frequency output as well as reduction of the lock-up time of the system response.
From Fig.4 can be simplified as shown in Fig.5, the PI-controller of this loop can be designed based on Fig.5.

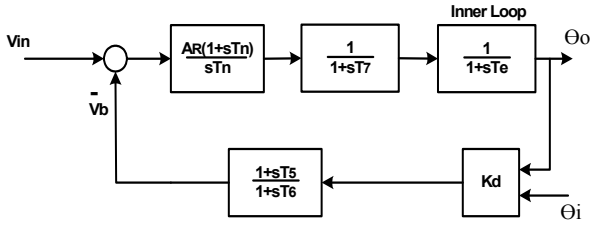


Fig.5 Shows the transfer function of a new PLL system.

From Fig.4, the inner loop (dual-loop of VCO) can be reduced to be equal $1/(1+sT_e)$ where $T_e = 4T_4$

From Fig.5, we can find the open-loop transfer function $(F_{o2}(s))$ and closed-loop transfer function $(F_{c2}(s))$ as follow;

$$F_{o2}(s) = \frac{A_R(1+sT_n)}{sT_n}.\frac{1}{(1+sT_e)}.K_d.\frac{(1+sT_5)}{(1+sT_6)}.\frac{1}{(1+sT_7)} \qquad (7)$$

where, we let the time constant $T_7 = T_5$.

From Eq. (7), the closed-loop transfer function is found as follow;

$$F_{c2}(s) = \frac{A_R K_d(1+sT_n)}{A_R K_d + sT_n(A_R K_d + 1) + s^2 T_n(T_e + T_b) + s^3 T_n T_e T_b} \qquad (8)$$

From Eq. (8), the PI-controller $\frac{A_R(1+sT_n)}{sT_n}$ can be designed by symmetrical optimum method [8] the parameter of controller can be found as follow;

$$A_R = \frac{T_6}{(2K_d T_e)} \text{ and } T_n = 4T_e\frac{T_6}{T_6 + 3T_e} \qquad (9)$$

The PI-controller of the main loop is designed for the optimum loop response as well as minimizing the lock-up time.

4. EXPERIMENTAL RESULTS

To verify this concept, we implement the dual-loop feedback configuration of VCO and the new PLL system with respect to Fig.1 and Fig.4 respectively

4.1 The dual-loop VCO characteristics

The on-chip VCO is MC14046B having the maximum frequency output 600KHz with V_{DD} 8 volt. The feedback path composed of PLL for providing a voltage output of LPF1 that is proportional to the input frequency and a compensator.

The controller is designed for closed-loop VCO according to the symmetrical optimum. The linearity of conventional VCO is greatly improved by dual loop VCO as shown in Fig. 6.

The transient response measurement of dual-loop VCO is setup with respect to Fig.1. This measurement the output of compensator is the voltage signal (Vf) then it is convenient to be measured by digital storage oscilloscope as the output response of dual-loop VCO. The Vin is the input command and the Vd is represented as the output of dual-loop VCO which used for measurement the step response due to d.c./a.c. signal or noise coupling at Vd input.

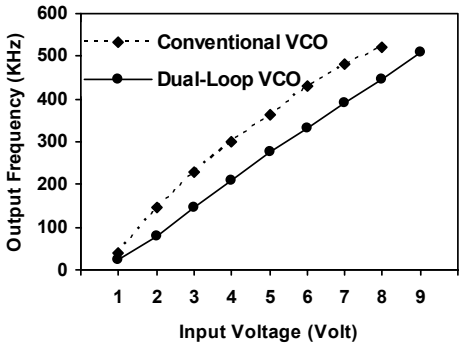


Fig. 6 Shows the linearity of conventional VCO is greatly improved by dual-loop VCO.

Fig.7 shows the output response of dual-loop VCO to the step d.c. signal coupling (Vd). The dual loop VCO has the ability to suppress the d.c. signal coupling.

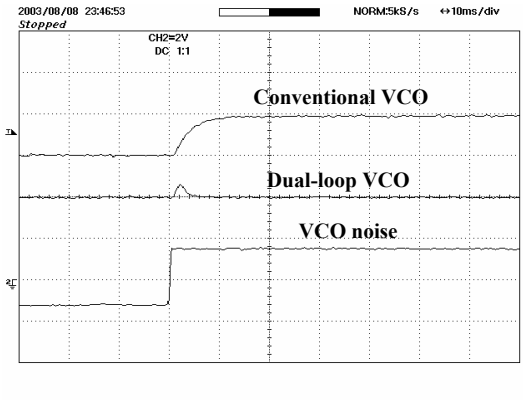


Fig. 7 Shows the output response to step d.c. signal coupling (Vd).

Fig. 8 shows output response to step a.c. signal coupling (Vd). The dual-loop VCO also has the ability to suppress the a.c. signal coupling at the frequency more than 1 MHz.

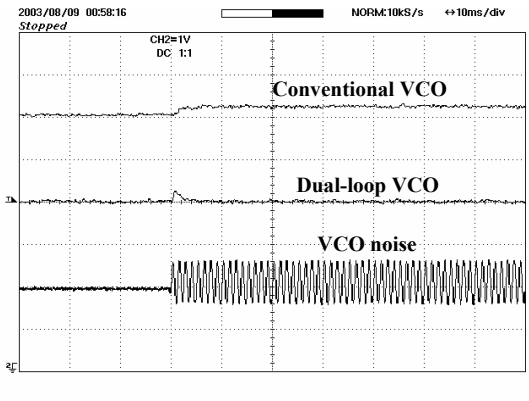


Fig. 8 Shows the output response to step a.c. signal coupling (Vd).

From Fig. 7 and 8, the dual-loop VCO has ability to suppress VCO noise better than conventional VCO. The frequency stability of dual-loop VCO measurement can be conducted by measuring the output frequency (Fo) of VCO which affected by the variation of the amplitude and frequency of the d.c./a.c. signal coupling and the variation of d.c. power supply. We set input of dual loop VCO to keep its output frequency constants at 300KHz. The measured data's can be plotted as the graphs shows in Fig.9 , Fig.10 and Fig.11 respectively.

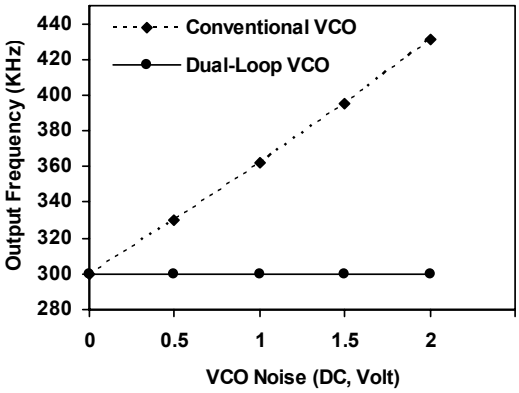


Fig. 9 Shows frequency stability against VCO noise (d.c.signal coupling).

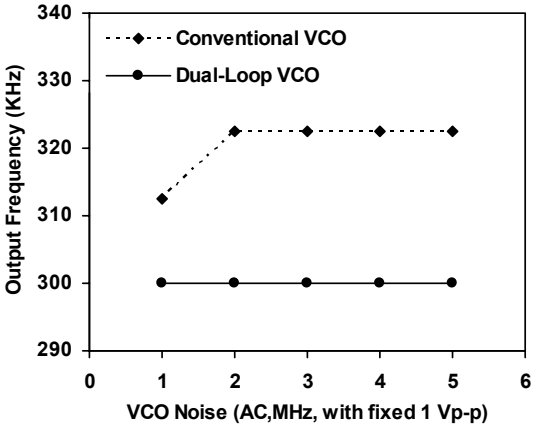


Fig. 10 Shows frequency stability against VCO noise (a.c. signal coupling).

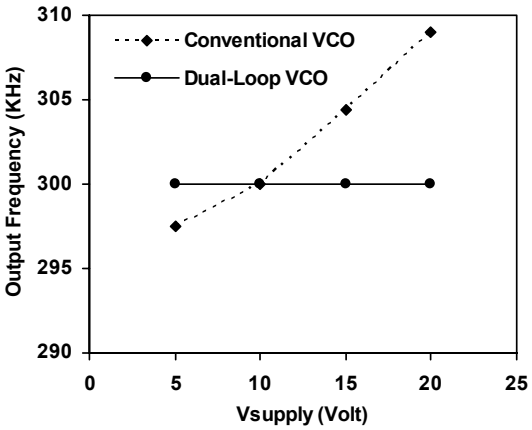


Fig. 11 Shows frequency stability against power supply variation.

4.2 The new PLL system

The new PLL system with controllable output phase and lock-up time is independent from output frequency which composes of the dual-loop VCO, PFD2, LPF2, compensator and PI controller as shown in Fig.4. The transient response measurement of the new PLL system is setup with respect to Fig.4. This measurement the output of PI-controller at the main loop is the voltage signal (Vc). The Vref is the control input used to control the phase of the frequency output and the lock-up time of the system response. The PI-controller of the main loop is designed by mean of the symmetrical optimum. Fig.12 show the transient response of the new PLL system to the step input frequency (Fref) when adjusting the control input (vref) equal to 1.5, 2, 2.5, 3 and 3.5 volt for reduce the lock-up times equal to 19, 9, 6, 4 and 3ms respectively. The new PLL system has the capacity to reduce the lock-up time.

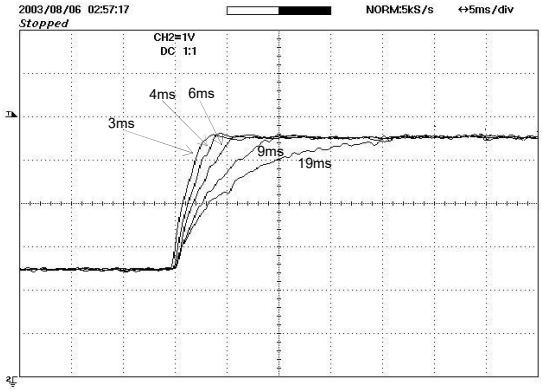
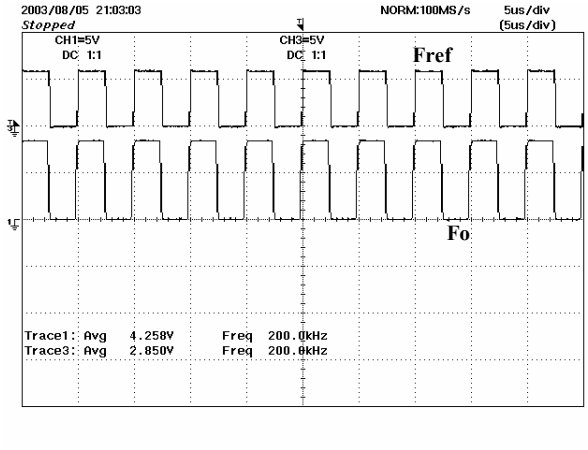
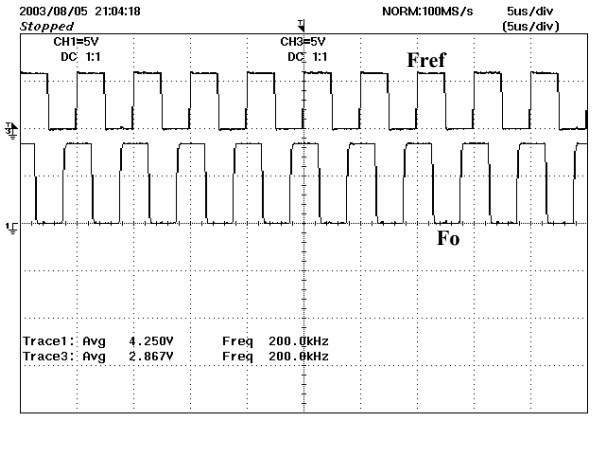


Fig. 12 Shows the lock-up times of the new PLL system with variable control signal (Vref).

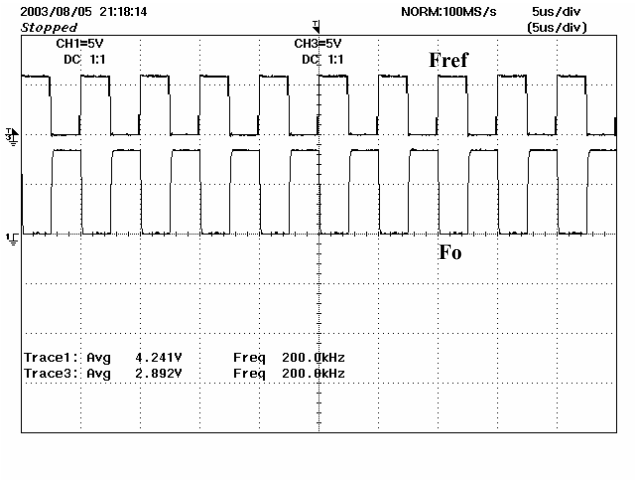
Fig. 13 shows the output frequency of the new PLL system to keep its output frequency constants at 200KHz when adjusting the Vref equal to 7, 8 and 9 volt for change the output phase equal to 0^o, 90^o and 180^o degree difference respectively.



a. output phase equal to 0^o degree difference.



b. output phase equal to 90^{o} degree difference.



c. output phase equal to 180^{o} degree difference.

Fig. 13 Shows the output phase control of the new PLL system.

5. Conclusion

The new PLL system is realized by combining the dual-loop VCO as the minor loop with the main loop consisted of PFD, LPF , compensator and PI-controller. The minor loop is the dual control loop of VCO acted as the VCO regulation system which has PI-controller and the feedback part to be a PLL. The purpose of minor loop can improve the performance of VCO such that linearity, frequency stability due to effected of VCO noise disturbances and the power supply variation. The main loop is the heart of new PLL system, it has a two inputs signal, one is used to setup the output frequency of system and another one is the control input using to control output phase independently from the output frequency. To minimize the lockup-time can also be controlled independently by the same input, Vref. The validness of this PLL system was confirmed by experimental results.

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