Improved the Noise Immunity of Phase-Locked Loop

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Abstract: This paper, we propose a new high noise immunity phase–locked loop(PLL) which can suppress the high incident noise coupling with large amplitude and long period to the input frequency of PLL and keeps constant frequency and phase of the VCO output for providing the high stability distribution clock pulse.

Keywords: Phase-locked loop, noise, adaptive filter, noise detector, locked detector.

1. INTRODUCTION

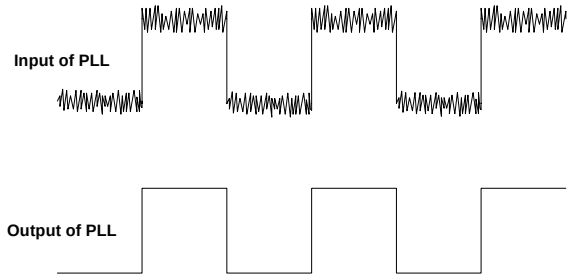
Clock distributor using PLL is becoming popular in digital system , because PLL efficiently perform clock generation with relatively low cost and it has the beneficial capability at the multiplying frequency which make the design of clock generation circuit easier and the radiated emission smaller, In the digital systems which include traditional PLL circuit provide the clock distribution system [1][2], the influence of the noise on the clock pulse lines which gives to the input of PLLs for the clock generation can cause the problem of unexpected clock phase shift .

The most research about the method obtaining stable clock pulse distributed to the digital circuits would use the method to adjust the bandwidth or the time constant of the low-pass filter of the low-pass filter of PLL [3],[4] for rejection the noise. Such method can reject the noise which coupled to the input frequency of PLL for a short period. In case large noise and long period which is given on the clock pulse line of the PLL input is still to be a problem.

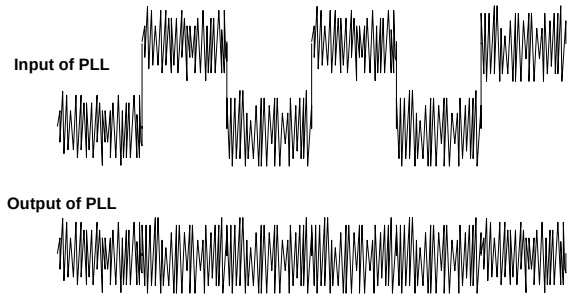
This paper presents the method to suppress the large noise which coupled to the input frequency line of the PLL for a long period with on affecting to the VCO output frequency. This method is achieved by modified the general phase-locked loop with connecting the locked detect(LD) and noise detector(ND) circuits in parallel to the input of the phase frequency detector (PFD) as shown in Fig. 4.2 . This proposed method is to improve the noise immunity of PLL, in a capture state or before locked condition the low-pass filter(LPF) is selected to the wide bandwidth characteristic in order to provide the fast locking operation of the system. After setting time of PLL going to lock, the lock detector(LD) will operate and give the output voltage to drive the switch(SW1) to be closed and at same time low-pass filter is adjusted to be a narrow bandwidth. After that it the noise is existing at the input reference frequency of PLL, the noise detector(ND) will operate to the switch(SW2) opened before the output voltage of the low-pass filter has any changing. As due to the narrow bandwidth of low-pass filter is characterized that it's output voltage will no any change when the switch(SW2) operated . After the existing noise disappears the switch (SW2) will turn to normally closed condition. The validness of this proposed PLL is confirmed by experimental results which compare to the general PLL characteristics.

2. THE INFLUENCE OF NOISE ON INPUT FREQUENCY OF PLL

The conventional PLL characteristics have an ability to suppress the finite incident noise at the input frequency of PLL due to the input frequency of the capability of the PFD(phase-frequency detector) which will detect only the leading edge of the input frequency and loop filter as shown in Fig. 2.1(a) of the incident noise is large amplitude and occurs in along period as shown in Fig. 2.1(b), the capability of PFD and loop-filter is not enough to suppress such noise so that the frequency stability of PLL will have a problem.



(a) Input frequency of PLL with finite incident noise.

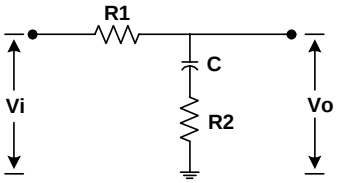


(b) Input frequency of PLL with large amplitude of incident noise.

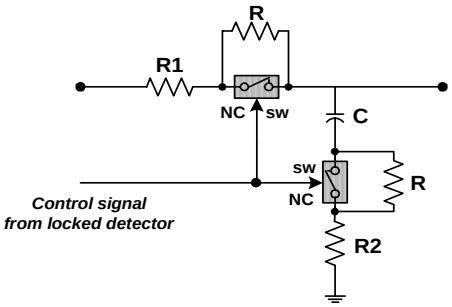
Fig. 2.1 Show the input frequency with different incident noise and the output signal of PLL.

3. ADAPTIVE LOOP-FILTER DESIGN

The loop-filter of filter the proposed PLL is an adaptive lead-lag filter, the convention one is shown in Fig. 3.1(a) and the adaptive lead-lag filter is shown in Fig. 3.1(b)



(a) Conventional Lead-Lag Filter.



(b) Adaptive lead-lag Filter.

Fig. 3.1 shown the conventional and adaptive lead-lag filters.

From Fig. 3.1(a), the function of lead-lag filter can be found.

$$F(s) = \frac{Vo}{Vi} = \frac{R_2CS+1}{(R_1+R_2)CS+1} \quad (1)$$

The general form of PLL transfer function can be found in [1].

$$\frac{\theta_o}{\theta_i} = \frac{\mathrm{N}\times \mathrm{K_d}\times K_o \times F(s)}{N\times S + K_d \times K_o \times F(s)} \quad (2)$$

Where: Kd = Gain constant of phase-frequency detector.
Ko = Gain constant of VCO.
F(s) = Transfer function of LPF.
N = The value of divider.

From Eq. (1) and (2), we can find ωn (Natural frequency) and ξ (Damping factor) as follow;

$$\omega n = \sqrt{\frac{K_d \times K_o}{N\times C\times (R_1+R_2)}} \quad (3)$$

$$\xi = 0.5\times \omega n \times (R_2C + \frac{N}{K_d \times K_o}) \quad (4)$$

At the condition before locked, this adaptive filter is characterized to have a wide bandwidth in order to provider PLL going to locked with faster lock up time by using ωn = $\frac{F_{ref}}{10}$ and ξ = 0.707 when the locked detector(LD) can detect the locking signal, the control signal from LD is sent to control the switch(NC) of LPF circuit to be opened in order to increases the resistance of R1 and R2.

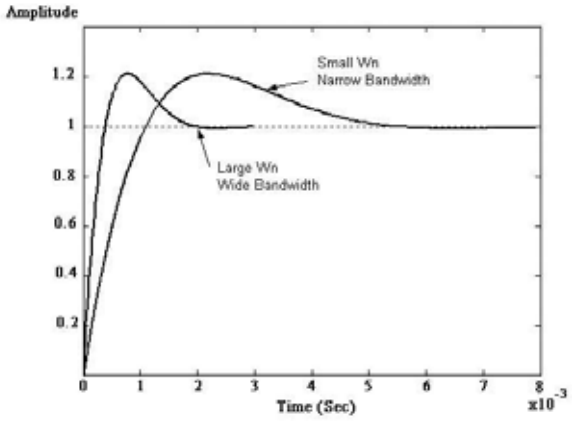
From Eq. (3), when resistances (R1 and R2) are increased, ωn will be decreased and loop bandwidth of LPF becomes smaller to provides slowly response of LPF to the step input. The output response of LPF to the step input can be found as follow;

$$\mathrm{Vo} = \frac{1}{s}\times\frac{(R_2CS+1)}{(R_1+R_2)CS+1} \quad (5)$$

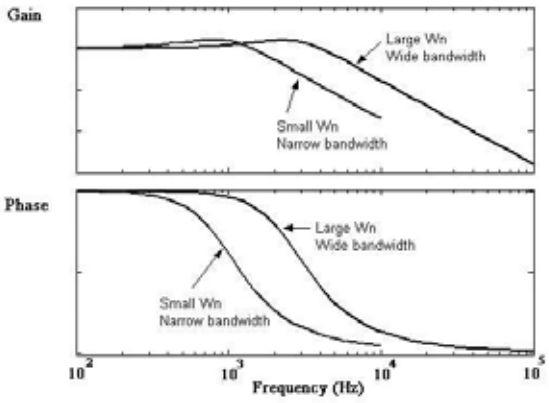
If we take inverse Laplace transform to Eq. (5), we can obtain.

$$\mathrm{Vo(t)} = 1 - R_1C\times e^{\frac{-t}{(R_1+R_2)C}} \quad (6)$$

From Eq. (6), we can see that the resistance (R1+R2) is inversed proportion to the bandwidth of LPF. The simulation of the output response to the step function and frequency response of LPF for a wide bandwidth compared with narrow bandwidth are shown in Fig. 3.2.



(a) Step response.

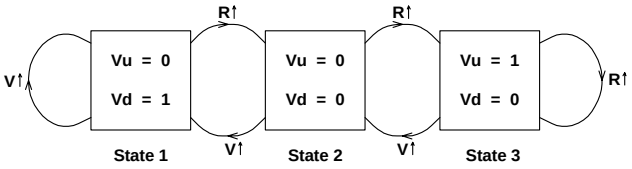


(c) Frequency response.

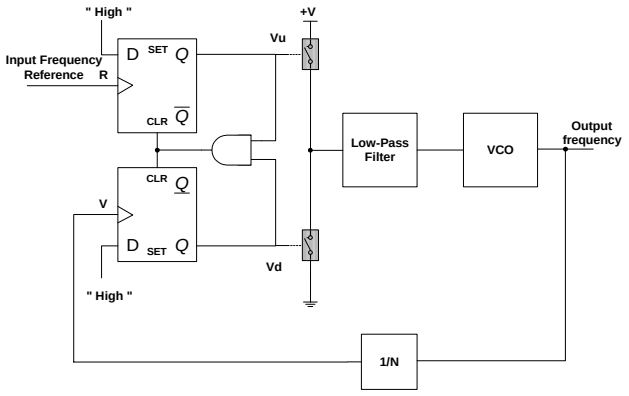
Fig. 3.2 Shows the step response and frequency response of LPF.

4. IMPROVED PLL ARCHITECTURE AND SYSTEM DESIGN

The PFD and Charge-pump is configured as the conventional PLL as shown in Fig. 4.1(b) which PFD and charge-pump will function to follow up the 3-state diagram as shown in Fig. 4.1(a).



(a) State diagram of PFD with 3-state.



(b) Conventional PLL.

Fig. 4.1 shows the conventional PLL and state diagram of PFD with 3-state.

From Fig. 4.1(a), PFD will be operated by the leading edge of a square pulse which given to both inputs (R,V), if the output of PFD has an initial state at state no.2 when PFD can the leading edge of pulse R before pulse V the output of PFD will charge to higher state and increasing the output voltage of charge-pump. And if the leading edge of pulse V comes to PFD input before pulse R, the PFD output will charge to lower state and decreasing the output voltage of charge-pump. If PFD can see that the leading edge of pulse R and V is existed at the same time, the output PFD will switch to the state No.2 which Vu and Vd are both zero that is mean pulse R and V have a same frequency and phase. This is the locking condition of PLL which has a PFD and charge-pump, LPF, and VCO in the loop operation.

From the conventional PLL in Fig. 4.1(b), we proposed the new high immunity PLL by adding some elements in the control loop such as ND (Noise Detector), LD (Lock Detector), switch(SW1) is the normally closed switch, and switch(SW2) is the normally opened switch as shown Fig. 4.2 .

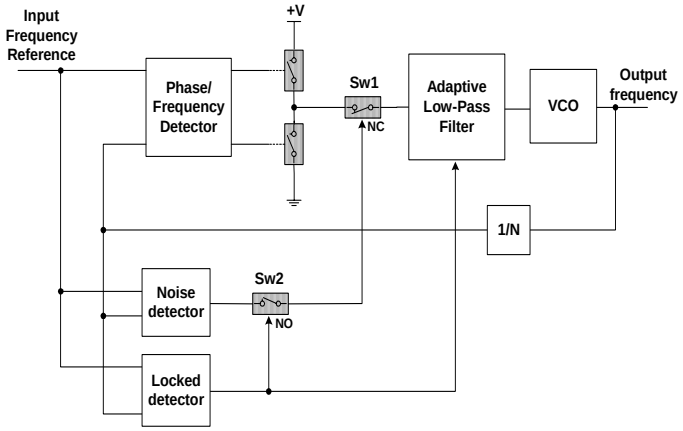


Fig. 4.2 Shown a new high immunity PLL.

From Fig. 4.2, when the switch, SW1 opened is the same condition as Vu and Vd are both zero that makes the output of LPF can keep a constant voltage for instant and can block the noise which cannot pass through an adaptive filter to VCO so that VCO output will give a stable clock pulse. The switch (SW1) is controlled by ND which input of ND is connected is parallel of input line of PFD for detecting noise on input line of PFD. The ND circuit will give the detecting signal output when the two inputs of PFD have a large difference frequency due to noise comes with one input. To prevent the error of noise detecting of ND, We must adding LD (locked detector) and adaptive filter which has 2 bandwidths in control loop as shown in Fig. 4.2 For instant PLL is going to lock, LD circuit will give the locking signal to control the switch (SW2) to be closed for accessing the output signal of ND. In other wise the changing bandwidth of adaptive filter is controlled by output signal of LD.

The operating condition of the proposed PLL has a three condition such as captive or before locking after locked with no noise and after locked with existing noise conditions is described in Table 1.

Low pass Filter	Wide Bandwidth	Narrow Bandwidth	Narrow Bandwidth	Narrow Bandwidth
Lock Detector	Unlock Detection	Locked Detection	Locked Detection	Locked Detection
SW1	Close	Close	Open	Close
SW2	Open	Close	Close	Close
Noise Detector	No noise Detection	No noise Detection	Existing Noise Detection	No noise Detection
	Capture or before locked condition	After locked and no noise condition	After locked and noise existing condition	After locked and no noise condition

Table 1. shows the operating condition of the low pass filter, locked detector, noise detector, switch sw1 and switch sw2 in case of capture or before locked, after locked and no noise, after locked and existing noise condition.

5. EXPERIMENTAL RESULT

A new high noise immunity PLL as shown in Fig. 4.2 has two important elements added in the control loop, such that locked and noise detectors. This two detector have the significant functions not only to manage the switching elements but also to control the bandwidth of LPF. The basic operation function of the locked detector is shown in Fig. 5.1.

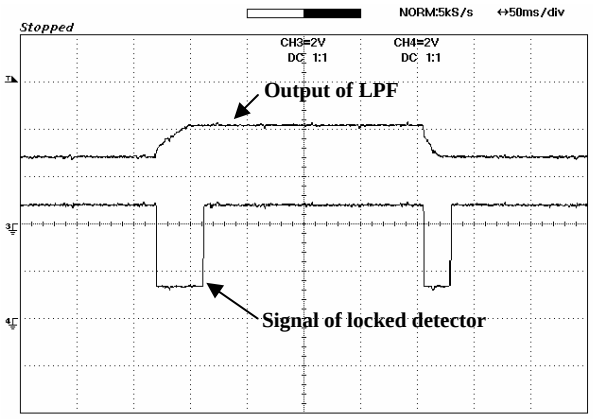


Fig. 5.1 Shown the basic operation function of locked detector.

From Fig. 5.1, we can see that the output signal of locked detector is charged from high to low when the input frequency of PLL is step from 200KHz to 300KHz. After PLL is in the locked condition, the output signal of locked detector will keep " High". During the output signal of the locked detector is changing from low to high or active high, this signal is send to the LPF for controlling the wide bandwidth to be a narrow bandwidth as shown in Fig. 5.2

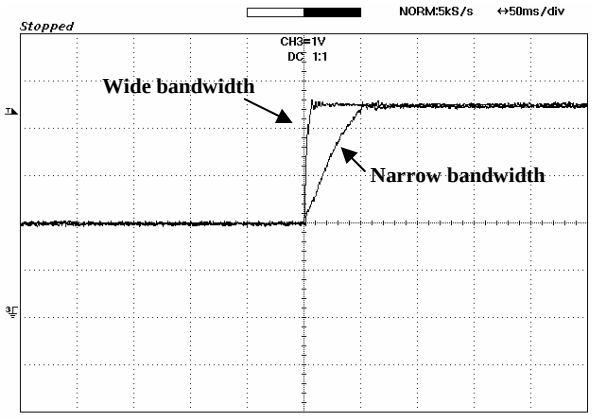


Fig. 5.2 shown the characteristic of adaptive LPF

The noise detector(ND) is also have a significant function to protect the adaptive LPF will have output signal with free of noise. The basic operation function of noise detector is shown in Fig.5.3. From Fig. 5.3 we can see that the output signal of noise will be changed from low to high. When noise is existing, if the noise disappear the output signal of ND will keep to "Low".

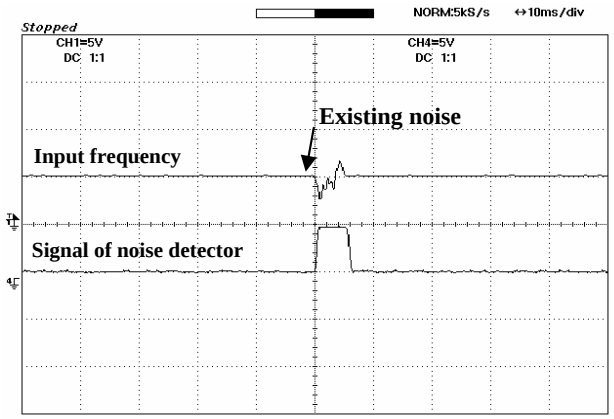


Fig. 5.3 shown the basic operation function of the noise detector .

After PLL is in the locked condition and the noise is existing at the input of PLL, the noise detector will give the output signal which changes from low to high or active high, this signal will go to drive the switch(SW1) in Fig. 4.2 is opened for protect the adaptive LPF to clear from noise as shown in Fig. 5.4.

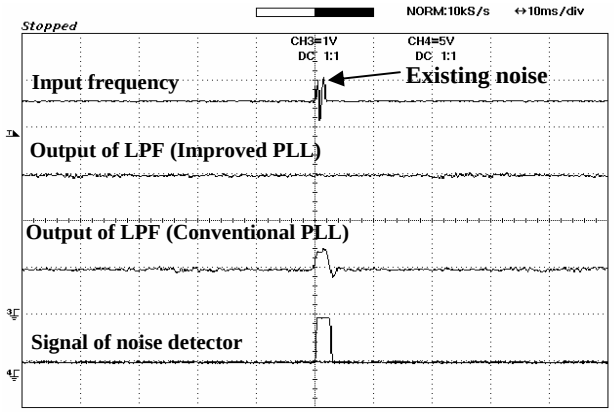


Fig. 5.4 shown the ability of new PLL to suppress the existing noise.

Fig. 5.5 shown the greatly improved characteristic of noise reduction of new PLL when comparing to the conventional PLL by measuring the error voltage (ΔV) at the both output of conventional LPF and adaptive LPF.

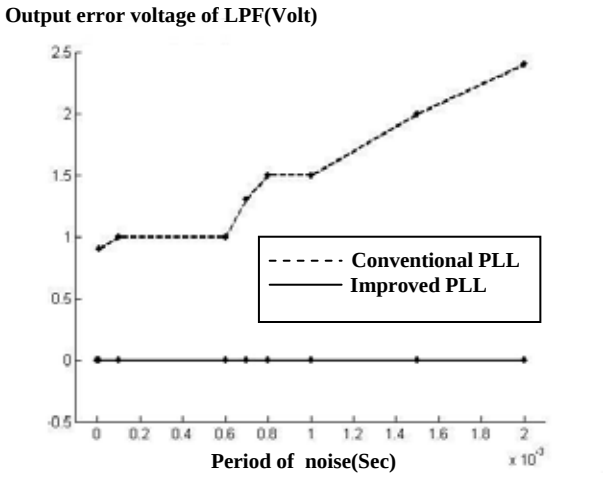


Fig. 5.5 Period disturbed by noise vs. output error voltage of LPF

CONCLUSION

The proposed PLL can suppress the large noise which coupled to the input frequency of the loop for a long period with no affecting to the VCO output frequency. The another advantage of this PLL is to has a high noise immunity and in capture or before lock condition the low pass filter(LPF) is selected to the wide bandwidth characteristic in order to providing the fast locking . After the system has been locked, the locked detector will operate to drive the switch sw1 to be closed for adjusting LPF to be a narrow bandwidth and providing the system has a high immunity of noise.

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