Implementation of PI Controllers with the FPGA

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Abstract: The implementation of PI controller with the FPGA is for controlling the speed of DC motor in the digital system. FPGA is assigned to 1. Outer speed control loop. The signal from the speed comparison will be in the PI controlling form transfer function of Direct Form I or PI Parallel Form. 2.Inner current control loop. The signal from the current comparison will be converted into switching function in sliding mode condition. Its output will be a controller of DC motor in the next step. The result from using FPGA will be close to the value of simulation in the analog control system. The sampling rate 40 kHz and 16 bit of 2's complement data are defined in this presentation.

Keywords: FPGA , PI Controller , Controller

1. INTRODUCTION

Field Programmable Gate Arrays (FPGAs) are one of the fastest growing parts of the digital integrated circuit market in recent times. They can be configured to implement complex hardware architectures. FPGA reconfiguration typically requires the whole chip to be reprogrammed even for the slightest circuit change. Dynamic reconfiguration means modifying the system when it is under operation. Dynamically reconfigurable FPGA systems can adapt to various computational tasks through hardware reuse. Numerous architectures that are dynamically reconfigurable have been proposed in the recent past. Unlike designers of static non-reconfigurable systems, designers of dynamically reconfigurable systems are required to analyze various design characteristics simultaneously. The search for a good design solution requires a thorough analysis of how the system can be dynamically reconfigured. This includes system throughput, reconfiguration time, sharing of reconfiguration data, selecting the target FPGA device, etc. [1]

2. BACKGROUND

2.1 Digital control [2]

Bilinear Transformation; This technique, also called the Tustin or trapezoidal approximation, uses the relationship

$$s = \frac{2}{T}\left(\frac{Z-1}{Z+1}\right) \tag{1}$$

to transform an s-domain function into the z-domain. Therefor it will be transform analog system into digital system.

The s-domain transfer function of analog controller $G_{PI}(s)$ obtained from the mathematical modeling can be given in the form

$$G_{PI}(s) = K_P + \frac{K_I}{S} \tag{2}$$

where K_P and K_I are the proportional and integral gains respectively.

The z-domain transfer function of discrete controller $G_{PI}(z)$ obtained from the mathematical modeling can be given in the form Eq. (3) for PI parallel structure and Eq. (4) for PI direct form I structure.

$$G_{PI}(z) = K_P + \frac{K_I T}{2}\left(\frac{Z+1}{Z-1}\right) \tag{3}$$

$$G_{PI}(z) = \frac{\left(\frac{K_I T}{2} + K_P\right)Z + \left(\frac{K_I T}{2} - K_P\right)}{Z-1} = \frac{b_0 Z + b_1}{Z-1} \tag{4}$$

2.2 Model of the DC motor [3]

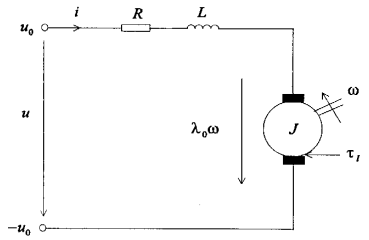

Fig. 1 Electric model of a DC motor with permanent excitation.

From the viewpoint of controllability, a DC motor with a constant excitation is the simplest electric drive. Fig. 1 shows the structure of the electric circuit of a permanently excited DC motor. The motor dynamics are governed by two coupled first-order equations with respect to armature current and shaft speed:

$$L\frac{di}{dt} = u - Ri - \lambda_0\omega \tag{5}$$

$$J\frac{d\omega}{dt} = k_t i - \tau_l \tag{6}$$

Where

i = armature current
u = terminal voltage
ω = shaft speed
J = inertia of the motor rotor and load
R = armature resistance
L = armature inductance
λ_0 = back-EMF constant
k_t = torque constant
τ_l = load torque

The motor parameters used to verify the design principles are L = 4.01 mH , R = 1.51 Ohm, J_m = 0.0000473 kg m^2 , k_t = 0.0832 Nm A^{-1} , λ_0 = 0.0833 V s rad^{-1} and $\tau_l = B\omega$ where B_m is coefficient of viscous friction equal to 0.0000269 Nm s rad^{-1}. The supplied link voltage is u_0 = 40 V

For speed control of a DC motor, a cascaded control structure is usually preferred, with an inner current control loop and an outer speed control loop. Control input u may be continuous or discontinuous, depending on the output power of the DC motor. A low-power system can use continuous control. A high-power system requires discontinuous control, perhaps in the form of pulse-width modulation (PWM), since a continuously controlled voltage is difficult to generate while providing a large current.

Since control discontinuities are the very nature of sliding mode control. Furthermore, discontinuous control of DC motors is universal in the sense that it can be employed for low-power systems and for high-power systems. Fig. 2 shows the typical control structure of a drive system based on a DC motor.

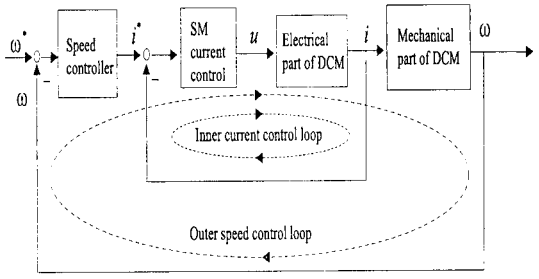

Fig. 2 cascaded control structure of DC motors.

2.3 Current control

At first, assume there exists an outer control loop providing a desired current i^* . Let us consider the current control problem by defining switching function

$$s = i^* - i \tag{7}$$

as the error between the real, measured current i and the reference current i^* determined by the outer-loop controller. Design the discontinuous control as

$$u = u_0 sign(s) \tag{8}$$

where u_0 denotes the supplied link voltage. To enforce the sliding mode, control gain u_0 should be selected such that $ss' \langle 0$. Now check this condition by evaluating ss' and select u_0 as

$$ss' = s\left(\frac{di^*}{dt} + \frac{R}{L}i + \frac{\lambda_0}{L}\omega\right) - \frac{1}{L}u_0|s| \tag{9}$$

$$u_0 \rangle \left| L\frac{di^*}{dt} + Ri + \lambda_0\omega \right| \tag{10}$$

then sliding mode can be enforced.

Examine inequality Eq.(10) If the reference current is constant, the link voltage u_0 need to enforce sliding mode should be higher than the voltage drop at the armature resistance plus the induced back-EMF, otherwise the reference current i^* cannot be followed. Furthermore, reference current i^* may not vary arbitrary; its time derivative di^*/dt should be bounded to ensure existence of sliding mode for a given link voltage u_0 .

2.4 Speed control

For the speed controller in an outer loop, the current control loop may be treated as an ideal current source, i.e. given a reference current i^* ,it will be tracked immediately. This assumption may become true only for systems in which the electrical time constant is much smaller than the mechanical time constant, or for systems where the dynamic response of the speed control is not critical problem. Any control design technique, linear or nonlinear, may be used speed control: PID (proportional integral derivative) control or a more sophisticated methodology, but without discontinuities like a sliding mode controller. The reason is that a sliding mode controller has already been employed in the inner current control loop; thus, if we ware to use another sliding mode controller speed control, the output of speed controller i^* would be discontinuous, implying an infinite di^*/dt and therefore destroying inequality Eq. (10) for any implementable u_0

In many industrial systems, PI (proportional integral) controllers are used with or without feedforward compensation, depending on the nature of the controlled system and the performance requirements. This type of controller is simple, but it may be sensitive to disturbances in mechanical subsystem. τ_l is unknown. Therefore it will be set as a disturbance in the system.

3. IMPLEMENTATION

In FPGA module, APEX DSP Development Board (starter Version) of Altera Co., Ltd will be used as a controller. The Quartus II Limited Edition development software provides a comprehensive environment for system–on–a–programmable - chip (SOPC) design. It controls DC permanent magnet motor MODEL E-587 of Electro-Craft Co., Ltd.

3 values of Analog Signals shown in Fig. 2 are ω^* , ω and i . They are for controlling a motor speed. To reduce a number of Analog to Digital (A/D), FPGA is then assigned as both of multiplex and de-multiplex shown in Fig. 3-4. Sampling rates of each channel are set at 40 kHz for 10 bit A/D. FPGA will convert 10 bit data to 16 bit (conv_10_16_bit). The receiving data will then be in the format of 16 bit as same as the processing data. In Fig. 4, there are 770 logic gates.

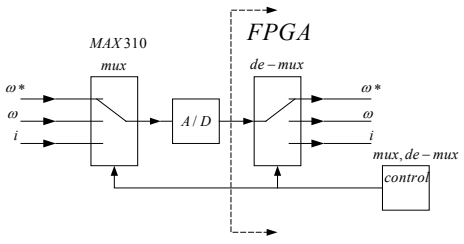

Fig. 3 Receiving of analog signal of FPGA

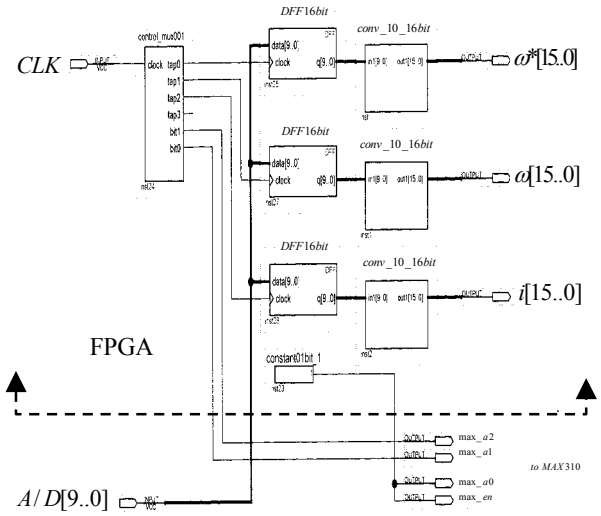

Fig. 4 Implementation of PI Controllers with the FPGA

In Sliding Mode of Current Control Module, the implementation is shown in Fig. 5 After comparing i^* with i, it will then create a PWM signal through D flip-flop which will set frequency of a switch. In Fig. 5, there are 400 logic gates.

+PWM is assigned as $+u_0$ of motor which will be a switch controller (SW1, SW4) shown in Fig. 6

-PWM is assigned as $-u_0$ of motor which will be a switch controller (SW2, SW3) shown in Fig. 6

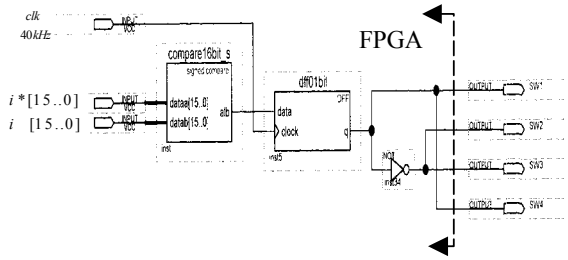

Fig. 5 Sliding mode Current Control

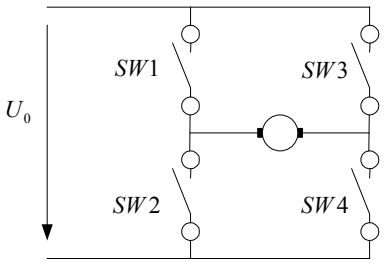

Fig. 6 H-Bridge switch

In Control Module, I signal is created from $(\omega^* - \omega)$ signal to be a control signal. The format is PI control. There are 2 structures as follows:

1. PI parallel structure or Eq. (3) as shown in Fig. 7 , there are 19900 logic gates.

2. PI direct form I structure or Eq. (4) as shown in Fig. 8 there are 19500 logic gates.

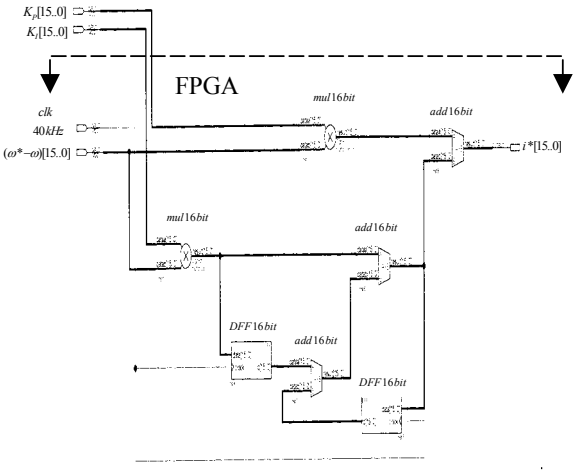

Fig. 7 PI controller Parallel structure

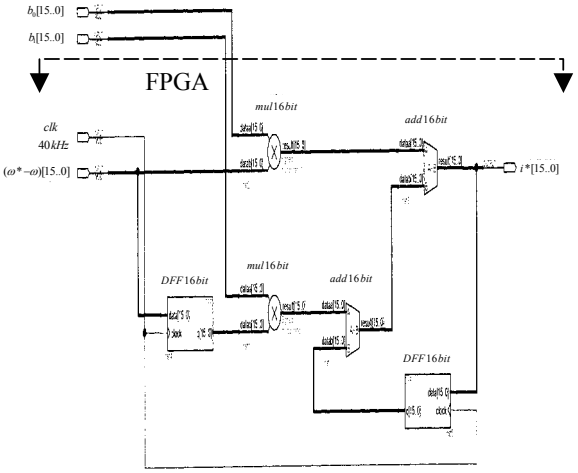

Fig. 8 PI controller Direct form I structure

4. RESULT

If a speed control of K_P and K_I are adjusted to a level of ±1000 rpm, the results will then be shown in Figs. 9~10 as follows:

a) The result of ω^* at 1000 rpm/div
b) The result of ω at 1000 rpm/div
c) The result of i^* at 500 mV/div
d) The result of i at 1 A/div

5.CONCLUSION

The advantages of digital hardware are very high speed and easily adjusted to comply with software. The use of FPGA in Digital Control can be easily adapted to Analog Control.

- Design of PI controller in the format of parallel structure to get P and I work at the same time.
- Design in the format of Direct Form I Structure to use in a format of transfer function.

Those results are not different. Besides FPGA can be a multiplex receiver of ω^* , ω and i . The signal will be compared and further create a driven signal for H-bridge.

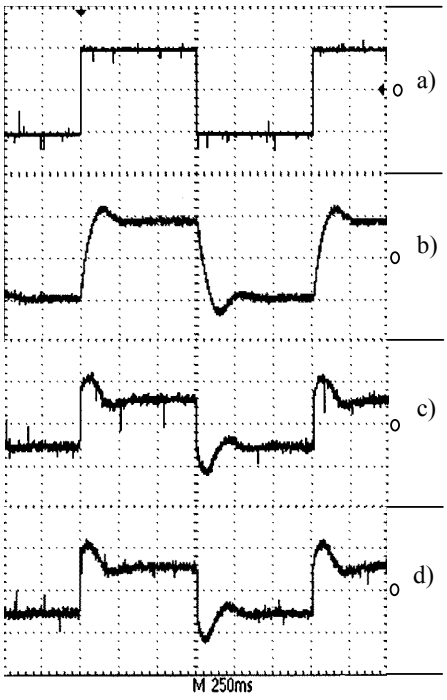

Fig. 9 Speed Control $K_P = 0.000122$ $K_I = 0.004768$

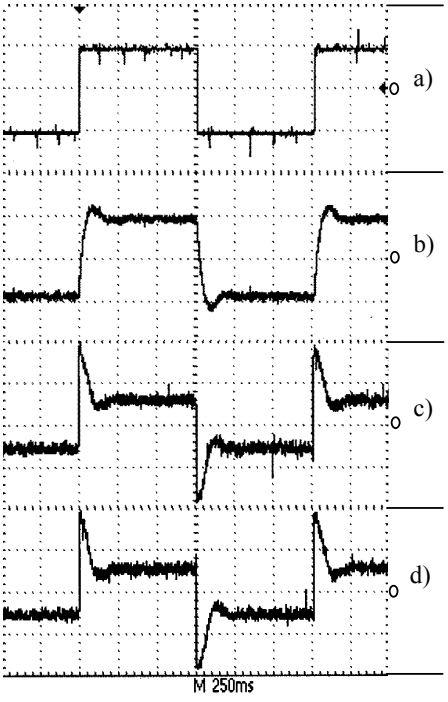

Fig. 10 Speed Control $K_P = 0.000244$ $K_I = 0.009536$

REFERENCES

[1] Sumanth Donthi, and Roger L. Haggard, "A survey of Dynamically reconfigurable FPGA devices," Proceedings of the 35th Southeastern Symposium on System Theory, pp. 422 –426, 2003.

[2] Irfan Ahmed, Implementation of PID and Deadbeat Controllers with the TMS320 Family, Texas Instruments, 1997.

[3] Vadim Utkin, Jurgen Guldner, and Jingxin Shi, Sliding Mode Control in Electromechanical Systems, Taylor & Francis, London, 1999.