# Automatic tune parameter for digital PID controller based on FPGA

**V. Tipsuwanporn, P. Jitnaknan , S. Gulpanich, A. Numsomran and T. Runghimmawan**

*Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang,*
*Bangkok 10520, Thailand. Tel: (66 – 2) 326 – 7347:Ext. 102*
*(E – mail: ktvittay@kmitl.ac.th)*

**Abstract**: Recently technologies have created new principle and theory but the PID control system remains its popularity as the PID controller contains simple structure, including maintenance and parameter adjustment being so simple. The adjust parameter of PID to achieve best response of process which be using time and may be error if user are not expert. Nowadays this problem was solved by develop PID controller which can analysis and auto tune parameter are appropriate with process which used principle of Ziegler – Nichols but it are expensive and designed for each task. Thus, this paper proposes auto tune PID based on FPGA by use principle of Dahlin which maximum overshoot not over 5 percentages and do not fine tuning again. It have performance in control process are neighboring controller in industrial and simple to use. Especially, It can use various process and low price. The auto tune digital PID processor embedded on chip FPGA XC2S50-5tq-144. The digital PID processor was designed by fundamental PID equation which architectures including multiplier, adder, subtracter and some other logic gate. It was verified by control model of temperature control system.

**Keywords**: FPGA, PID,Dahlin.

## 1. INTRODUCTION

Recently technologies have created new principle and theory but the PID control system remains its popularity as the PID controller contains simple structure, including maintenance and parameter adjustment being so simple. The adjust parameter of PID to achieve best response of process which be using time and may be error if user are not expert. As well as nowadays process is faster than formerly. Then this paper propose auto tune parameter of PID based on chip FPGA which very fast in calculate. The auto PID controller was designed by consist of analog to digital 10 bit converter, digital 12 bit to analog converter, digital PID processor and Algorithm of Dahlin which embedded on chip FPGA. The auto tune PID processor will be use algorithm of digital PID-equation, which come from fundamental PID equation and algorithm of Dahlin. First part present theory and method of PID and Dahlin. Next part explains design processor on chip FPGA. Other part will show experiment temperature process and conclusion.

## 2. THEORY

### 2.1 Principle and theory of digital PID controller

PID controller has a fundamental equation [1], [4].

$$V_o(t) = K_p\left[e(t) + \frac{1}{T_i}\int e(t)\,dt + T_d\,\frac{de(t)}{dt}\right] \quad (1)$$

And

$$e(t) = sp(t) - pv(t) \quad (2)$$

When

*Vo(t)* = controller output.
*e(t)* = error.
*st(t)* = set point.
*pv(t)* = process output.
*Kp* = controller gain.
*Ti* = integral time (sec.).
*Td* = derivative time (sec.).

From equation (1), change to digital PID controller by discrete differential equation following.

$$V_o = V_{o_{n-1}} + K_p\left[(e_n - e_{n-1}) + \frac{\Delta T}{T_i}e_n + \frac{T_d}{\Delta T}(e_n - 2e_{n-1} + e_{n-2})\right] \quad (3)$$

When

$\Delta T$ = The sampling period
$V_{o_{n-1}}$ = Controller output at the *n*th sampling instant.
$e_n$ = error at the *n*th sampling instant.

Define $K_i = \frac{K_p \Delta T}{T_i}$

$K_d = \frac{K_p T_d}{\Delta T}$

So that digital PID equation show below.

$$V_o = V_{o_{n-1}} + (K_p + K_i + K_d)e_n - (K_p + 2K_d)e_{n-1} + K_d e_{n-2} \quad (4)$$

### 2.2 Process Characteristics Analysis

Transfer function of the process used for characteristic analysis will be in form of a process called First- Order Lag Plus Dead Time (FOPDT), that is,

$$G(S) = \frac{Ke^{-t_0 s}}{\tau s + 1}$$

When $\tau$ = process time constant

The testing of the process characteristic can be done by unit step input signal [$m(t)$] into the process. The response obtained in regardless of disturbance signal is S-shaped as shown in Fig.1. This method can use to test with second or higher-order process with damping Ratio equal to or higher than 1.

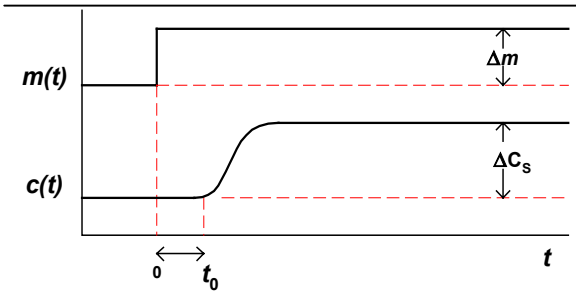


Fig.1. Process reaction curve or open-loop step response.

With the step change of $m(t)$, the output response of the FOPDT process is

$$\Delta c(t) = K\Delta mu(t-t_0)\left[1-e^{-(t-t_0)/\tau}\right] \quad (5)$$

At the steady-state,

$$\Delta c_s = \lim_{t\to\infty}\Delta c(t) = K\Delta m \quad (6)$$

The steady-state gain of the process can be obtained from Eq.(6) as

$$K = \frac{\Delta c_s}{\Delta m} \quad (7)$$

Dead time of the process ($t_0$) is derived from checking time from the beginning until there is a response about 3%,while the time constant of $\tau$ is obtained from a calculation by replacing time $t_1$and $t_2$ in Eq.(3) by setting

$$t_1 = t_0 + \frac{\tau}{3}, t_2 = t_0 + \tau \quad (8)$$

Obtain

$$\Delta c_1 = \Delta c(t_0 + \frac{\tau}{3}) = 0.283K\Delta m = 0.283\Delta c_s$$
$$\Delta c_2 = \Delta c(t_0 + \tau) = 0.632K\Delta m = 0.632\Delta c_s$$

So, $$\tau = \frac{3}{2}(t_2 - t_1) \quad (9)$$

**2.3 PID controller Parameter Synthesis**

To consider parameter synthesis of PID controller, it is made from Close loop control principle as stated in Fig.2.

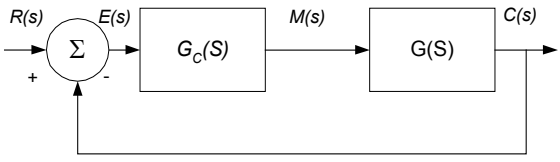


Fig.2. Block diagram for PID controller synthesis.

Theoretically, the most suitable response to feed back control system is the control system which provides the response in form of Fist Order Lag, but dead time of this control system remains negative, making this controller becomes unreal. So, it is necessary to consider the control system, which provides First Order Lag response with dead time $t_0$ as in Eq.(10).

$$G_c(s) = \frac{\tau}{K(\tau_c + t_0)}\left[1 + \frac{1}{\tau s}\right] \quad (10)$$

Which is the PI controller that has value.

$$Kp = \frac{\tau}{K(\tau_c + \tau_0)}, T_i = \tau \text{ and } T_i = \tau \quad (11)$$

When is the PID parameter controller is synthesized by Dahlin method [1] and parameter is

$$Kp = \frac{\tau}{K(\tau_c + \tau_0)}, T_i = \tau \text{ and } T_d = \frac{t_0}{2} \quad (12)$$

When $\tau_c$ = the time constant of the close-loop response

With the process used for PID control, it should have $t_0$ more than τ/4 and $\tau_c$ should be similar $t_0$ in changing set point value to create overshoot not over 5%

**2.3 Extrapolation**

Extrapolation is an estimation of future data by analyzing data obtained from various samplings. A suitable method of numerical analysis is Newton's Divided-Difference Extrapolating Polynomial, in which this paper use to calculate $\Delta c_s$ advance. The value obtained from this calculation method has a slight error, by using equation

$$\begin{aligned} F(x) = {} & f(x_0) + (x-x_0)f[x_1, x_0] + \\ & (x-x_0)(x-x_1)f[x_2, x_1, x_0] + \ldots + \\ & (x-x_0)(x-x_1)\ldots(x-x_{n-1})f[x_n, x_{n-1}, \ldots, x_0] \end{aligned} \quad (13)$$

when

$$f[x_1, x_0] = \frac{f(x_1) - f(x_0)}{x_1 - x_0}$$

$$f[x_n, x_{n-1}, \ldots, x_0] = \frac{f[x_n, \ldots, x_1] - f[x_{n-1}, \ldots, x_0]}{x_n - x_o}$$

$x_n$ = data from each sampling
$f(x)$ = value from extrapolation

user is able to select suitable size of the sampling period. In this paper uses 3 sampling data, that is $x_0$ , $x_1$ and $x_2$ to calculate future data $x_3$ and $x_4$ that shown the tendency of process response. If $x_4 > x_3$ then it will calculate $x_4$ and $x_5$ again from sampling data $x_1$ ,$x_2$ ,$x_3$ until future data $x_n \geq x_{n+1}$ because the response result becomes stable. Once the data is obtained, that is $x_n = \Delta c_s$ , controller will analyze data and figure out parameter from the test.

## 3. DESIGN

**3.1 PID processor**

The digital PID processor embedded on chip FPGA which use algorithm from digital PID controller equation. Fig. 3. show block diagram which will be define variable SP and PV have size 10 bit, $K_p$, $K_i$ and $K_d$, have size 8 bit and $V_o$ has size 12 bit.

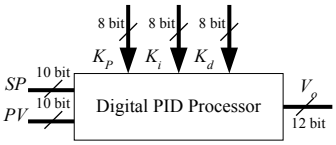


Fig. 3. The block diagram of digital PID processor.

An internal digital PID processor to consist of 3 process show in fig. 4. Process 1, 2 and 3 are share operator in order to reduce number gate of FPGA. Thus all operator are compose 3 input 20 bit full adder, 2 input 10 bit full adder, both 2 input 10 bit multipliers which show state diagrams in fig. 5. To work each process defined by state machine which relate to clock signal.

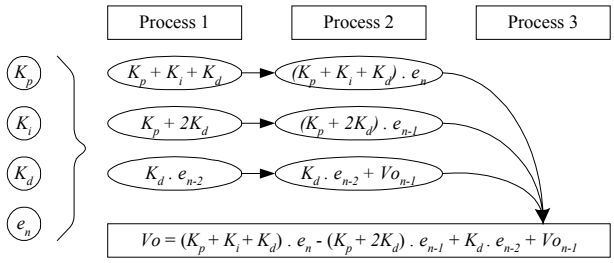


Fig. 4. The process within digital PID processor.

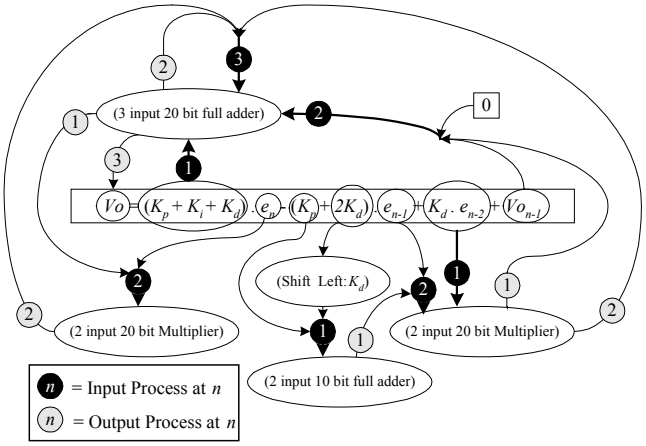


Fig. 5. State diagrams for share operator within PID processor.

### 3.2 Auto tune (Dahlin) on FPGA

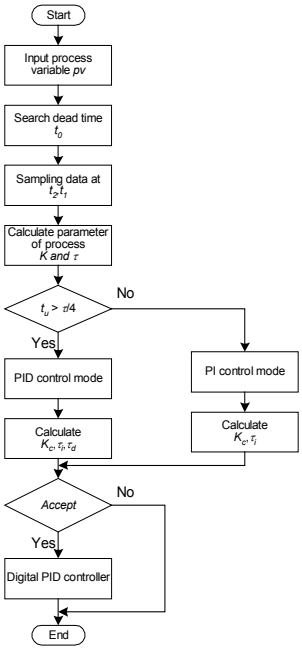


Fig. 6 Flowchart for calculate parameter.

In analyzing characteristic of the process there is a test by unit step signal into the process. The dead time value of process can also be obtained from this test. Once the resulting response becomes stable, take $\Delta c_s$ to calculate steady – state gain and time constant of the process. Since the test of analyzing the $\Delta c_s$ takes long time until response becomes stable therefore in this paper the numerical analysis is used to estimate value of $\Delta c_s$ by comparing data from sampling while the unit step input signal during the test. Once the data is obtained that $K$, $\tau$ and $t_0$ carry to calculate into digital PID processor. The step for calculate show in Fig. 6.

## 4. EXPERIMENTAL RESULT

### 4.1 Simulation PID processor result

The application program ModelSimXE are used to simulate digital PID processor for verify this processor. The result of simulation when set point is unit step and fix parameter of PID, manipulate variable (MV) are change relate to theory of PID

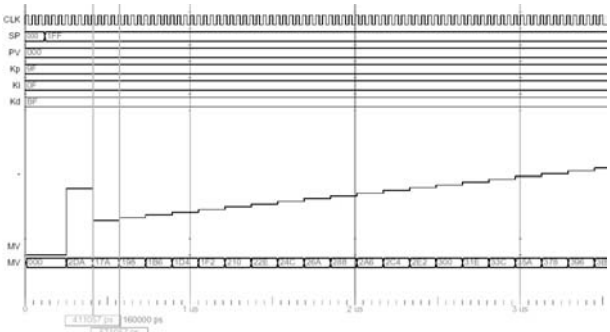


Fig. 7 Result of simulation PID processor.

### 4.2 Implementation PID controller result

The experiment will be use temperature process system which consist of temperature sensor, retransmission signal, auto tune PID controller, heater and phase control. Fig. 8. show diagram of temperature control system which controlling temperature within oven will be control phase input of heater by controller will be send control signal is 4 – 20 *mA* to phase control. Fig. 9. show temperature process system.

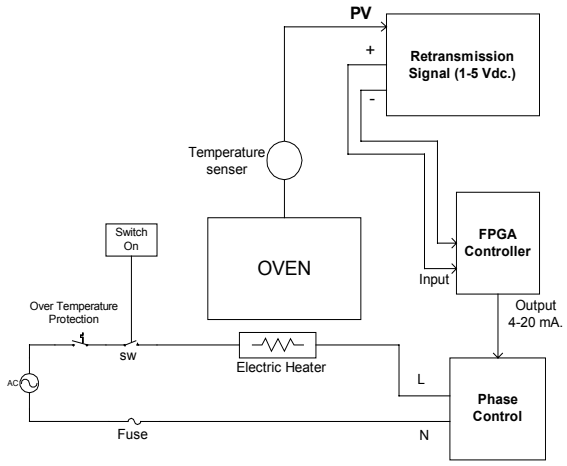


Fig. 8. The diagram of temperature process system.

Fig. 9. The temperature process system.

Figs. 10 and 11 show the experimental result of process which process not overshoot but steady state time about 25 seconds. When step are change not effect to controlling.

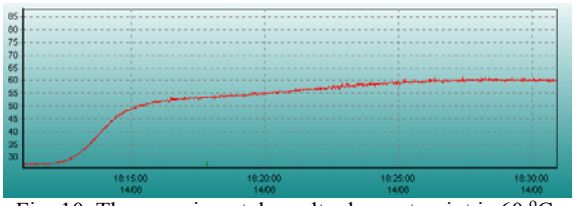

Fig. 10. The experimental result when set point is 60 $^{o}$C.

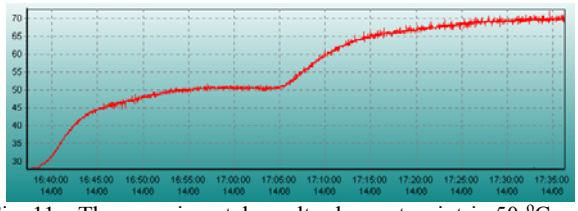

Fig. 11. The experimental result when set point is 50 $^{o}$C and then change set point to 70$^{o}$C.

## 5. CONCLUSIONS

PID controller development by applying FPGA as the PID controller that can analyze and automatically tune the appropriate parameter of the controller and takes less time while avoid any error or damage that may occur due to insufficient skill of user. This method is very accurate and provides a good process response. According to experimental results of temperature control process, it is found that a Self-Tuning PID controller can operate very effectively and accurately and save expenses with easier works. In addition, the result obtains is good.

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