LOW DIRECT-PATH SHORT CIRCUIT CURRENT OF THE CMOS DIGITAL DRIVER CIRCUIT

Jirawath Parnklang Ampaul Manasaprom Nut Laowanichpong

Department of Electronics,
Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang
Charlongkrung Road, Ladkrabang, Bangkok, Thailand, 10520
E-mail: kpjirawa@kmitl.ac.th

Abstract An idea to redce the direct-path short circuit current of the CMOS digital integrated circuit is present. The sample circuit model of the CMOS digital circuit is the CMOS current-control digital output driver circuit, which are also suitable for the low voltage supply integrated circuits as the simple digital inverter, are present in this title. The circuit consists of active MOS load as the current control source, which construct from the saturated n-channel and p-channel MOSFET and the general CMOS inverter circuits. The saturated MOSFET bias can control the output current and the frequency response of the circuit. The experimental results show that lower short circuit current control can make the lower frequency response of the circuit.

Keywords: Electronics Circuit, Signal Processing

1.INTRODUCTION

In recent years, the designers have been putting increasing effort into reducing the supply voltage and power consumption of digital and analogue and mixed integrated circuits and system. This.trend towards lower operation voltages has been brought about by a number of factors. Firstly, there is a need to reduce power dissipation in modern digital systems. Complete systems can be implemented on modern high-density integrated circuits. As chip components get closer together, the problem of heat dissipation increases. And break-down voltage between components on a chip reduces as geometry get smaller. Secondly, the use of battery-operated portable electronics and wireless systems is increasing. Examples are cellular phones, portable PCs and wireless terminals. All these benefit from lower power and low weight requirements. Thirdly, low-power solutions are spreading into other fields of application, such as filters, audio signal processing and EMI and EMC component system. In particular, non-invasive sensors are being fully integrated on chip.

Finally, there is considerable scientific interest in exploring the technological and physical limits of integrated devices. These factors fall into two main categories: the increasing demand for logn-life portable equipment and the technological limits of VLSI circuit. As for the portable applications, low power requirement usually implies a sacrifice in terms of speed and/or dynamic range, while high speed and high integration density are the basic aim of VLSI research.

We know that the best way to reduce the power dissipation in VLSI digital circuits is to decrease the supply voltage. A decrease in supply voltage is necessary because the electrical field within the chip has to be maintained at an acceptable level. But in this title if the supply voltage cannot be reducing this technique will help you to reduce the power consumption of the CMOS circuits.

2. CIRCUIT DESCRIPTION

Figure 1 shows the CMOS output digital driver circuit concept, which is composed of the fundamental segment of digital CMOS inverter circuit, and the bias current source circuits segment. In the fundamental segment, there are PMOS and NMOS devices (MN1, MP1) with the supply voltage V_{DD}. The current source use as the short circuit control when both of the transistor MN1 and MP1 is operated in saturate mode, which occur when the circuit is in the transition from high logic level to low logic level.

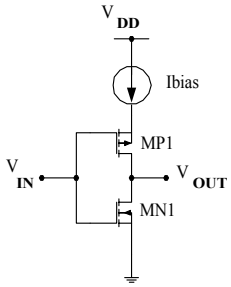


Figure 1. The current source CMOS output digital driver circuit

The output driver circuit threshold voltage [5][6] $V_{th} = V_{in} = V_{out}$ occurs when all of the transistors are saturated such that

$$V_{th} = \frac{V_{Tn} + \sqrt{\beta_p / \beta_n}\left(V_{DD} - \left|V_{Tp}\right|\right)}{\left(1 + \sqrt{\beta_p / \beta_n}\right)} \qquad (1)$$

Where β_n and β_p is the devices transconductance parameter of the NMOS and PMOS transistors respectively.

The objective of the current source is to control the maximum switching current I_{max} of the switching output. If the maximum switching current is limited to I_{max}, then for a given load capacitance C_{Load} the output-switching transient [7] is limited by

$$\tau = \frac{C_{Load} V_{DD}}{I_{\max}} \tag{2}$$

For the current controlled output digital driver circuit shown in figure 1, the charging and discharging current are limited by the bias current ans the saturate current ov the MN1 and MP1. Here, the rise and fall times are limited to

$$\tau_{rise} = \frac{C_{Load} V_{DD}}{I_{bias}} \tag{3}$$

And

$$\tau_{fall} = \frac{C_{Load} V_{DD}}{I_{MN1}} \tag{4}$$

The increase in output transient time and the realization of low level output voltage for given output sink current when output voltage is low are major limitation in using current controlled output driver. In addition, the switching speed of a fully current controlled output driver is always less than or equal to the switching speed of an equivalent current unregulated output digital driver circuit. From this concept, the implemented circuit with dual current source control is shown in figure 2.

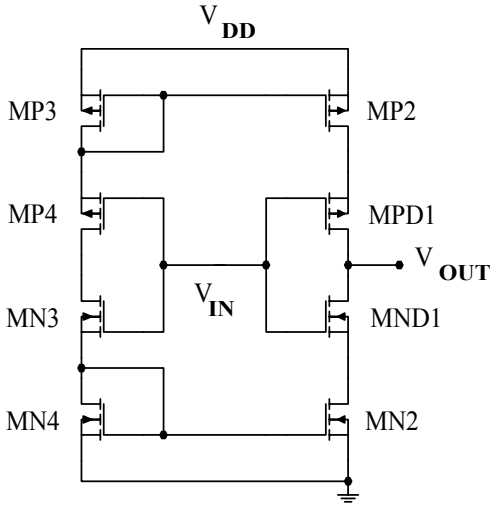


Figure 2 The implemented current control digital driver circuit

The circuit topology is such that the gates of the two transistors (MND1 and MPD1) are connected to form the input of the circuit with

$$V_{in} = 2V_{GSn} = V_{DD} - 2V_{SGp} \tag{5}$$

While the drain of the MN1 is tied to the current source MN2 which control the current form the current miller MN3 that we design it to be the current amplifier. The W/L of the MN3 is smaller as the design rule can,.and also the drain of the MP1 is tied to the current source MP2 which also control the current concept as the MN2 and MN3, giving the output voltage of

$$V_{out} = V_{DSMN1} + V_{DSMN2} = V_{DD} - V_{SDMP1} - V_{SDMP2} \tag{6}$$

To construct the voltage transfer characteristic for the output driver circuit, start with input voltages $V_{in}<V_{Tn}$. Since the MN1 is in cutoff, $I_{Dn} = I_{Dp} = 0$. However, the MP1 has an inversion layer established since V_{SGMP1} is large and the currents from MP1 and MP2, which flow through the output node, are controlled by the MP2. The output voltage is thus

$$V_{out} = V_{OH} = V_{DD} - V_{MP2} - V_{MP2} \approx V_{DD} \tag{7}$$

When the input voltages $V_{in}<V_{Tp}$, the MP1 is in cutoff, $I_{Dn} = I_{Dp} = 0$. However, the MN1 has an inversion layer established since V_{SGn} is large and the current from MN1 which flow from the output node are controlled by the MN2. The output voltage is thus

$$V_{out} = V_{OL} = V_{DSMN1} + V_{DSMN2} \approx 0 \tag{8}$$

Now, the current controlled output digital driver circuit with dual current source control shown in figure 2, the charging and discharging current are limited by the bias current and the current and the MN1 and MP1 which operate as a switch. Here, the rise and fall times are both limited to

$$\tau_{rise,fall} = \frac{C_{Load} V_{DD}}{I_{DS(sat)MN2,MP2}} \tag{9}$$

There are three major sources of power dissipation in digital CMOS circuits, which are summarized in the following equation:

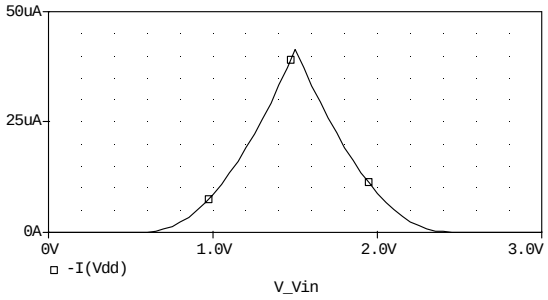
$$P_{total} = p_t \left(C_L \cdot V \cdot V_{dd} \cdot f_{clk} \right) + I_{sc} \cdot V_{dd} + I_{leakage} \cdot V_{dd} \tag{10}$$

The first term represents the switching component of power, where C_L is the loading capacitance, f_{clk} is the clock frequency, and p_t is the probability that a power-consuming transition occurs (the activity factor). In most cases, the voltage swing V is the same as the supply voltage V_{dd} ; however, in some logic circuits, such as in single-gate pass-transistor implementations, the voltage swing on some internal nodes may be slightly less [6]. The second term is due to the direct-path short circuit current I_{sc}, which arises when both the NMOS and PMOS transistors (the conventional driver) are simultaneously active, conducting, current directly from supply to ground. For This low power consumption digital driver circuit, all of the transistors are saturated being on at the same time while the input switches such that short circuit current of low power driver circuit less than the conventional driver circuit. So that power dissipation of low power driver circuit will less than the conventional driver, as is shown in figure 3 for the implemented circuit and figure 4 for the conventional CMOS digital driver circuit. Finally, leakage current $I_{leakage}$, which can arise from substrate injection and subthreshold effects, is primarily determined by fabrication technology considerations

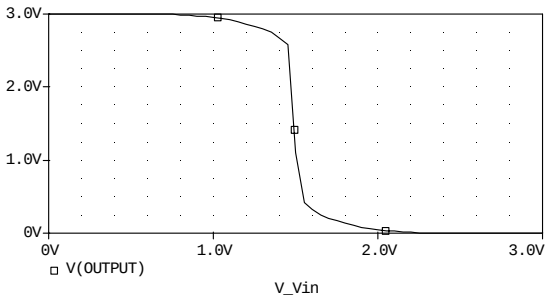
We also evaluated (through experimental measurements and SPICE simulations) the DC input-output characteristics of both conventional output driver circuit and the circuit in figure 2., which are plotted using the Voltage-Transfer Curve (VTC) shown in figure 3 and figure 4. This is simply a plot of V_{out} as a function of V_{in}. The inversion operation is seen directly from the curve: when V_{in} is small, V_{out} is large, and vice-versa.

III. RESULTS AND DISSCUSION

To verify the implemented circuit concept, Pspice program is used for all of the simulation. The level 49 MOSFET model of the Spice is used. Some useful parameters of the entire MOS device are the threshold voltage of both PMOS and NMOS is absolute 0.6 volt and the device transconductance of the driver PMOS (MPD1) is equal to the driver NMOS (MND1). The current gain of the current mirror is 4. The supply voltage of the circuit is 3 volts and the input sweep voltage is from 0 to 3 volts. The simulation results of the direct-path short circuit current of the basic digital inverter and the designed output driver circuit, and also the voltage transfer characteristics, which are shown in figure 3 and 4 respectively. The figure show that the direct-path maximum short circuit current (I_{SC}) of the conventional digital driver circuit is 41.5 μA. and the implemented circuit I_{SC} is 5.9 μA.

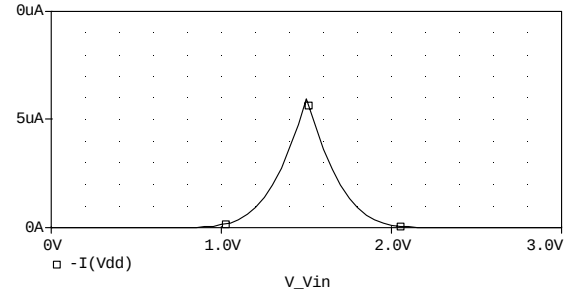


(a) I_{SC}

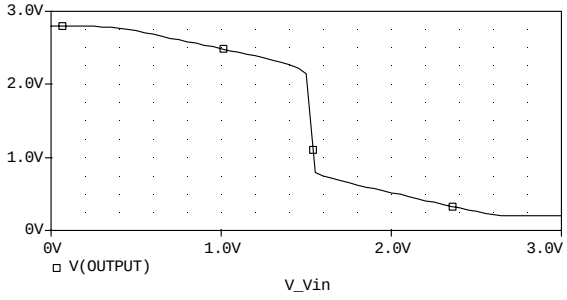


(b) VTC

Figure 3. The direct-path short circuit current (I_{SC}) of the conventional digital driver circuit



(a) I_{SC}



(b) VTC

Figure 4. The direct-path short circuit current (I_{SC}) of the implemented digital driver circuit

The frequency response of the both CMOS output driver circuit at 3V-supply voltage was measured in figure 5 and figure 6. It –3dB bandwidth of the conventional driver was about 146MHz and the –3dB bandwidth of the conventional driver was about 42 kHz.

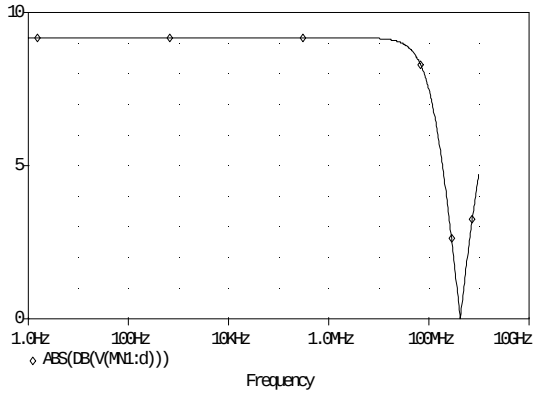


Figure. 5. The gain response of the conventional CMOS digital output driver circuit

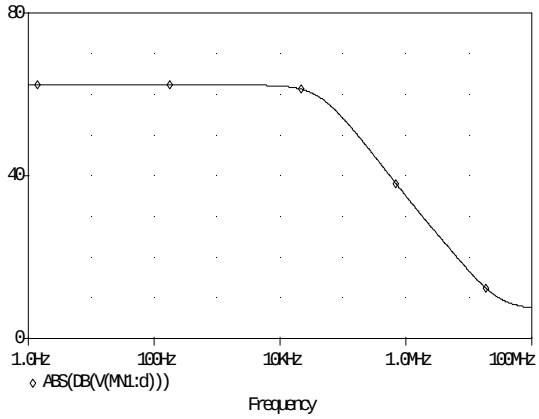


Figure. 6. The gain response of the implemented CMOS digital output driver circuit

IV. SUMMARY

An idea to reduce the direct-path short circuit current of the CMOS digital integrated circuit is present The CMOS output digital driver circuits using positive and negative bias current have been proposed as the sample in this paper. Simulation results are given to show the useful of the proposed circuit. The propose idea show that the maximum short circuit current of the sample circuit can be reduce 1000 time compare with the conventional output digital driver circuit although the frequency response of the circuit, which is depend on this current, is also decrease. Frequency response of the circuit shows that the proposed CMOS current control output digital driver circuits will be useful for low power consumption application.

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