An Analog Maximum, Median, and Minimum Circuit in Current-mode

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Abstract: In this paper, the CMOS integrated circuit technique for implementing current-mode maximum and minimum operations scheme is described. The maximum and minimum operations are incorporated into the same scheme with parallel processing. Using this scheme as the basic unit, an analog three-input maximum, median, and minimum circuit is designed. The performance of the proposed circuit shows a very sharp transfer characteristic and high accuracy. The proposed circuit achieves a high-speed operation, which is suitable for real-time systems. The PSPICE simulation results demonstrating the characteristic of the proposed circuit are included.

Keywords: maximum and minimum operations, three-input median circuit, current-mode circuits, CMOS-based circuit

1. INTRODUCTION

Conventionally, the maximum, median, and minimum circuits can be implemented in either digital or analog form [1-10]. The analog maximum, median, and minimum operations are often needed in some real-time applications of analog signal processing such as image processing and fuzzy applications [3-10]. In recent years, much attention is on the CMOS-based maximum, median, and minimum circuits in current-mode [3-10]. Because of the current-controlled current sources have much higher bandwidth in comparison to those of the voltage-controlled active elements. The current sources can drive small resistive and capacitive loads up to very high frequencies without sacrificing its stability [11]. The most reported realization of the maximum and minimum operations so far have been implemented either maximum or minimum operation. When incorporating the maximum and minimum operations into the same circuit, the advantages will be gained [7-8]. The three-input maximum, median, and minimum circuits have been introduced [9-10]. The approach in literature [9] is based on voltage-mode signal processing while the approach in literature [10] generates accumulated error as a result of using the two-input maximum and minimum cell to implement the three-input maximum, median, and minimum circuit. To reduce the accumulated error, the three-input maximum and minimum operations are integrated into the same scheme is presented in this paper. Using this CMOS-based scheme as the basic unit, the median operation is designed. The proposed maximum, median, and minimum circuit can be operated under the single supply voltage. The resulting performances of the proposed circuit have high accuracy and wide-band capability.

2. CIRCUIT DESCRIPTION

From basically design of the proposed circuit, the transistors are all matched and operated in their saturation regions. The drain current of NMOS transistor operated in saturation region is expressed as [12]

$$i_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(v_{GS} - V_T\right)^2 = K\left(v_{GS} - V_T\right)^2 \quad (1)$$

where K, v_{GS}, and V_T are the device transconductance parameter, the gate-source voltage, and the threshold voltage, respectively.

2.1 Three-input maximum operation scheme

The scheme of three-input maximum operation [13] is shown in Fig. 1. The implementation of this scheme is based on the shared gate-source voltage corresponding to the saturation value imposed by the maximum input current. Each maximum cell for one input signal is comprised of three NMOS transistors, M_{j1}, M_{j2}, and M_{j3}. The transistor M_b and the bias current source I_B generate a bias voltage V_B to provide the pre-bias transistors M_{j1}-M_{j3}. The diode connected transistor M_a and the transistor M_c form as the unity gain positive current mirror to capture the maximum current to output node. The maximum operation of the scheme Fig. 1 can be explained as follow.

Suppose that there is only one maximum input current among the three positive input currents, and the maximum current is i_1, which can be stated as

$$i_1 = \max\left(i_1, i_2, i_3\right) \quad (2)$$

The drain-source voltages v_1, v_2, v_3 of the transistors M_{11}, M_{21}, M_{31} established by the input currents i_1, i_2, i_3, respectively. The input voltage v_1 is established by the maximum input current i_1, hence the voltage v_1 is the maximum voltage. The gates of transistor M_{11}, M_{21}, M_{31}, and M_a are connected together. Then their gate-source voltages can be given by

$$v_{GS11} = v_{GS21} = v_{GS31} = v_a \quad (3)$$

Based on Eqs. (1)~(3), the transistors M_{11}, M_{21}, M_{31}, and M_a have the same drain current as

$$i_{D11} = i_{D21} = i_{D31} = i_{Da} = i_1 \quad (4)$$

In saturation, the current i_{D21} flows through the transistor M_{21} increasing the gate-source voltage of the transistor M_{21}, which effects the transistor M_{22} to cutoff. Similarly, The flow of i_{D31} through the transistor M_{31} causes the transistor M_{32} to cutoff. Therefore the drain currents i_{D22} and i_{D32} can be given by

$$i_{D22} = i_{D32} = 0 \quad (5)$$

Considering at node v_a, the drain current i_{Da} can be expressed as

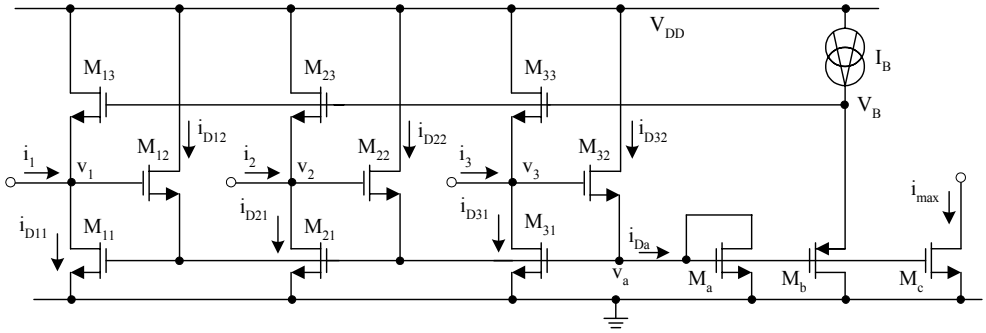


Fig. 1 Three-input maximum operation scheme

$$i_{Da} = i_{D12} + i_{D22} + i_{D32} \tag{6}$$

Substituting Eq. (5) into Eq. (6), we obtain

$$i_{Da} = i_{D12} = i_1 \tag{7}$$

The current i_{Da} is mirrored into output node by the current mirror M_a and M_c. Then the maximum output current i_{max} can be given by

$$i_{\max} = i_1 = \max\left(i_1, i_2, i_3\right) \tag{8}$$

2.2 Incorporated three-input maximum and minimum operations scheme

Fig. 2 shows the incorporated maximum and minimum operations scheme for three input currents, which based on the use of the maximum scheme in Fig. 1. For one input signal, the cell consists of three NMOS transistors, M_{j1}-M_{j3}, and two PMOS transistors, M_{j4}-M_{j5}. The transistors M_a, M_c, and M_d function as the unity-gain positive current mirror. The transistors M_e and M_f function as the unity-gain negative current mirror. The maximum operation scheme in Fig. 2 can be discussed as section 2.1, the minimum operation can be explained as follow.

Suppose that all input currents are positive and the maximum and minimum currents are i_1 and i_3, respectively, which can be stated as

$$i_1 = \max\left(i_1, i_2, i_3\right) \quad \text{and} \quad i_3 = \min\left(i_1, i_2, i_3\right) \tag{9}$$

The drain-source voltage v_1 is established by the maximum input current i_1, thus the voltage v_1 is the maximum voltage. The matched NMOS transistors M_{11}, M_{21}, M_{31} and M_a have the same gate-source voltage v_1, so, in saturation, they should also have the same drain current as

$$i_{D11} = i_{D21} = i_{D31} = i_{Da} = i_1 \tag{10}$$

Considering at each input node, the input current i_j can be written as

$$i_{Dj4} = i_{Dj1} - i_j \tag{11}$$

Based on the Eq. (10) and Eq. (11), the drain current i_{Dj4} of transistor M_{j4} can be given by

$$i_{D14} = 0,\ i_{D24} = i_1 - i_2,\ \text{and}\ i_{D34} = i_1 - i_3 \tag{12}$$

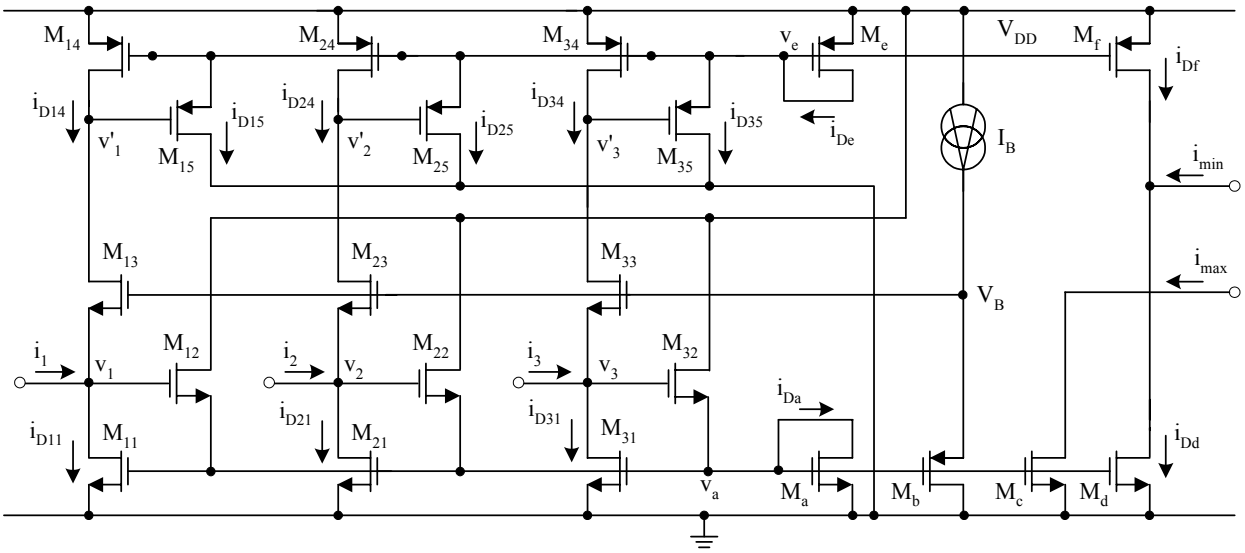


Fig. 2 Incorporated three-input maximum and minimum operations scheme

Based on the shared gate-source voltage corresponding to the saturation value imposed by the maximum current. The source-drain voltage v'_3 is established by the maximum differential current i_1-i_3, thus the voltage v'_3 is the maximum voltage effecting the transistors M_{15} and M_{25} to cutoff. Therefore, the drain currents i_{D15} and i_{D25} can be given by

$$i_{D15} = i_{D25} = 0 \tag{13}$$

At node v_e, the drain current i_{De} can be written as

$$i_{De} = i_{D15} + i_{D25} + i_{D35} = i_1 - i_3 \tag{14}$$

Substituting Eq.(13) into Eq.(14), the drain current i_{De} can be rewritten as

$$i_{De} = i_{D35} = i_{D34} = i_1 - i_3 \tag{15}$$

The unity gain current mirrors M_a,M_d and M_e,M_f reflect the drain currents i_{Da} and i_{De} to minimum output node, respectively. Thus the minimum output current can be stated as

$$i_{\min} = i_{Df} - i_{Dg} = i_{Da} - i_{De} \tag{16}$$

Substituting Eq.(10) and Eq. (15) into Eq.(16), we obtain

$$i_{\min} = i_1 - (i_1 - i_3) = i_3 = \min(i_1, i_2, i_3) \tag{17}$$

It is clearly seen that the maximum and minimum operations for three input currents are incorporated into the same scheme with parallel processing.

2.3 The proposed scheme

Using the incorporated maximum and minimum operations scheme and the current mirrors as the basic unit, the three-input maximum, median, and minimum circuit is designed. In Fig. 3, the transistors M_{P1}-M_{P3} form as the dual-output negative current mirror with the unity current gain (CM1). The input current i_{in}, and the output currents i_{out1} and i_{out2} flow out from the circuit. The input current i_{in} flows into the circuit while the output currents] i_{out1} and i_{out2} flow through the output nodes. The relation between the input current i_{in} and the output currents i_{out1} and i_{out2} can be expressed as

$$i_{in} = i_{out1} = i_{out2} \tag{18}$$

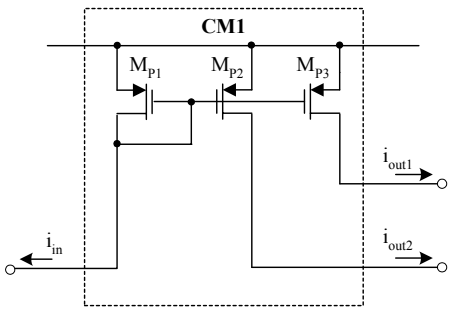


Fig. 3 The dual-output negative current mirror (current gain = 1)

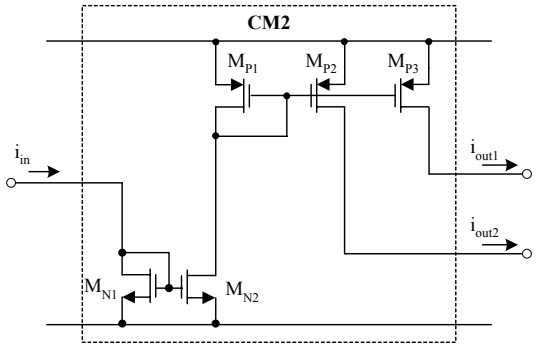


Fig. 4 The dual-output current mirror (current gain = 1)

Fig. 4 shows the circuit diagram of the dual-output current mirror with the unity current gain (CM2). The relation between the input current i_{in} and the output currents i_{out1} and i_{out2} can be also expressed as Eq. (18).

The median operation can be realized as shown in Fig. 5. The output current for the median value i_{med} is equal to

$$i_{med} = (i_1 + i_2 + i_3) - (i_{\max} + i_{\min}) \tag{19}$$

3. SIMULATION RESULTS

To verify the performances of the proposed circuit, the circuit in Fig. 3 has been simulated with the PSPICE analog simulation program. The BSIM MOS model of the 0.5μm CMOS process was used for the circuit simulation. The proposed circuit simulations, the dimension W/L of the devices used are 10μm/1μm, the bias current source I_B is set to 25μA. The supply voltage V_{DD} is equal to 5V. The simulated transient-responses of the proposed circuit are shown in Fig. 6, where the input currents i_1, i_2, and i_3 are 100kHz sinusoidal wave with 80μA, 100μA, and 60μA peak amplitude and 110°, 0°, and 240° phase shift, respectively. From the results, the errors for maximum, median, and minimum operations are about 0.02%, 0.37%, 0.25% of full-scale value (100μA), respectively. It is evident that the proposed circuit function correctly and provides excellent performances.

4. CONCLUSION

A current-mode circuit configuration for realizing the three-input maximum, median, and minimum operators has been presented. The proposed circuit is based on the use of the incorporated maximum and minimum operations in the same scheme and the current mirrors. The proposed circuit has a simple structure and can be directly fabricated in a standard CMOS process. The PSPICE simulation results have been used to verify the performances of the proposed circuit and have been demonstrated to agree very well with the theoretical predictions.

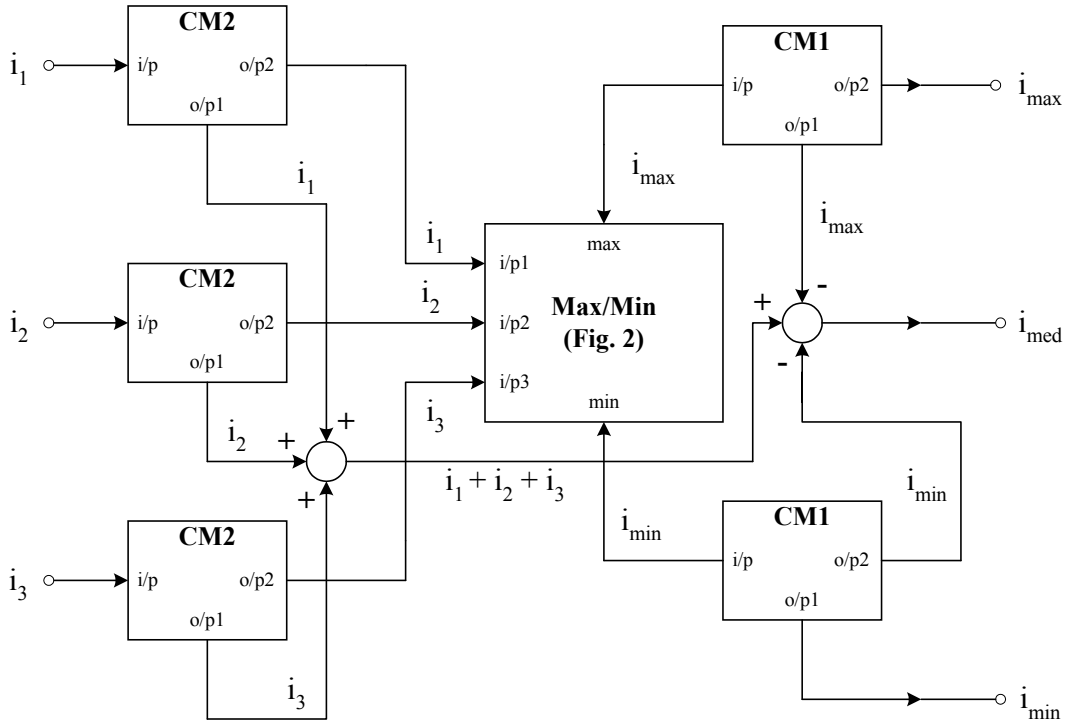
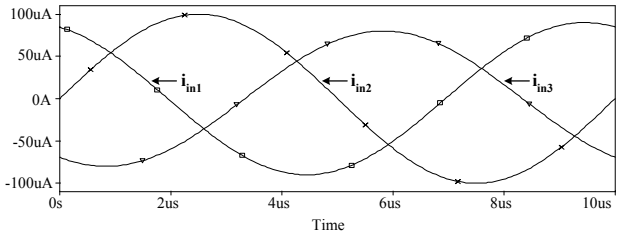
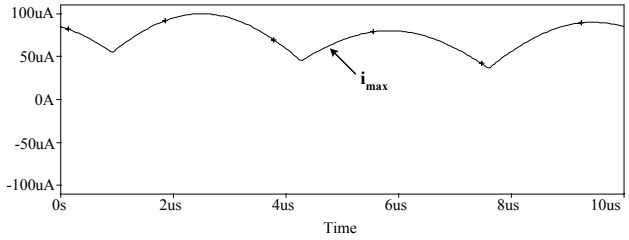


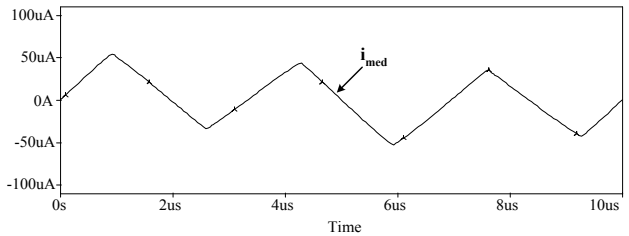
Fig. 5 Block diagram of the proposed circuit



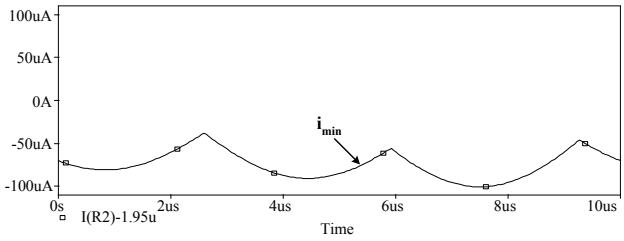
(a) Sinusoidal input signal currents



(b) Maximum output current, i_{max}



(c) Median output current, i_{med}



(d) Minimum output current, i_{min}

Fig. 7 Simulated transient response

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