A Low-voltage CMOS CCII

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Abstract: A CMOS second generation current conveyor, which can be operated from a low-voltage power supply, is presented in this article. The proposed circuit is simple, small in size and suitable for implementing in standard CMOS process. It provides the resistance at port X lower than 3.5Ω. The bandwidth of the transfer characteristic extends beyond 326MHz. PSPICE simulation results demonstrating the characteristics of the proposed circuit are included.

Keywords: CCII, Voltage follower

1. INTRODUCTION

The second generation current conveyor (CCII) is a very versatile building block for current mode analog signal processing. It can be used as element in many applications such as an instrumentation amplifier, a analog signal conditioner, a current measuring device in a digital measurement of current, probe for a digital voltmeter and a digital-to-analog converter that can be provide current source output [1-3]. The analog current mode circuit designs become increasingly important and attractive. Due to the current mode circuit have a wider bandwidth than the voltage mode circuit. The current mode circuit can drive small resistive and capacitive loads up to very high frequencies without sacrificing its stability.

One fundamental approach to realize the second generation current conveyor is based on the bipolar transistor. In recent years, there has been strong motivation to develop a novel CMOS circuit which can perform an analog function. This is due to the rapid progress in CMOS technology which made it possible to manufacture complex and flexible chips. The low power and low voltage issue has been increased important in VLSI application. The demand of portable and battery-powered equipment are much attention in the present to the future. Thus, the current conveyor circuits realizable in integrated technology, especially in CMOS technology, have attracted considerable attention. An implementation of CMOS technology is presented in [4] seems to be the most suitable. Unfortunately, it includes a class AB behavior which require the supply voltage higher than 3V. Thus, it is unacceptable in CMOS applications that the supply voltage should be trend lower than 3V. Recently, a low supply voltage CCII operated at ± 1.5V is presented in [5]. However, it has the resistance at port X higher than 150Ω that causes the large transfer error between port Y and X. The purpose of this article is to propose a low voltage CMOS second generation current conveyor that has the low resistance at the current input node and wide bandwidth.

2. CIRCUIT DESCRIPTION

Basically, a CCII is a three–port device derived by interconnecting the voltage and the current follower that the relationship can be given by

$$\begin{bmatrix} i_y \\ V_y \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ \pm k & 0 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ V_x \\ V_z \end{bmatrix} \quad (1)$$

where k denoted the current gain and it is usually set to equal one. From Eq. (1), the current at port Y is equal zero. The voltage at port Y is accurately transferred to port X. The current at port Z is a replica of the current at port X. The cases of $i_z = (+k)*(i_x)$ and $i_z = (-k)*(i_x)$ will be referred to as the positive current conveyor (CCII+) and the negative current conveyor (CCII-), respectively. It can be further inferred that the differential terminal resistance at port Y and Z must be high, while the differential terminal resistance at port Y and X must be low.

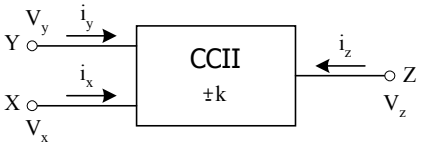

Fig. 1 Second generation current conveyor

Figure 2 shows the voltage follower circuit that the relationship between the voltage at port Y and port X can be written by

$$V_y = V_{GS1} - V_{GS2} + V_x \quad (2)$$

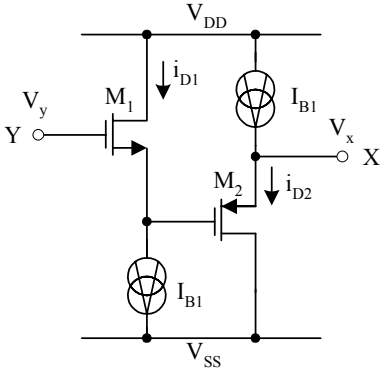

Fig. 2 The voltage follower circuit

Both of transistors are operated in their saturation regions. The drain current of transistor operated in saturation region is expressed as

$$i_D = \frac{\mu C_{OX} W}{2L}(V_{GS} - V_T)^2 = K(V_{GS} - V_T)^2 \quad (3)$$

where K, V_{GS} and V_T are the device transconductance parameter, the gate-to-source voltage and the threshold voltage, respectively.

In the BSIM MOS model of the 0.5μm CMOS process, K of NMOS (K_n) is larger than K of PMOS (K_p) about 3.9. Hence, we design the ratio of channel widths and lengths (W/L) of M_2 larger than M_1 about 3.9 and the drain current of M_1 and M_2 are equals that can be written as

$$K_n = 3.9K_p \quad (4)$$

$$i_{D1} = i_{D2} = I_{B1} \quad (5)$$

The gate-to-source voltage of transistors M_1 and M_2 are equal or

$$V_{GS1} = V_{GS2} \quad (6)$$

Then port X voltage is forced to equal that of port Y,

$$V_x = V_y \quad (7)$$

The resistance at port X can be given by

$$r_X \approx \frac{1}{g_{m2}} \quad (8)$$

where g_{mi} is the transconductance at M_i. If $g_{m2} = 170 \times 10^{-6}$ AV^{-1}, then r_x obtains

$$r_x \approx 5.33\ k\Omega \quad (9)$$

It can be seen that the resistance at port X is rather large. In order to reduce this resistance, the transistor M_3 and the current source are included as shown in figure 3. The transistor M_3 form the negative feedback loop. The current source I_{B2} can be written as

$$I_{B2} = I_{B1} + i_x + i_{D3} \quad (10)$$

Hence, the circuit in figure 3 has the resistance at port X that can be expressed as

$$r_x \approx \frac{1}{g_{m2} g_{m3} r_{I1}} \quad (11)$$

where r_{I1} is the resistance at the current source I_{B1}. If $g_{m2} = 1.19 \times 10^{-4}$ AV^{-1}, $g_{m3} = 4.81 \times 10^{-4}$ AV^{-1} and $r_{I1} = 5$ MΩ, Then r_x in figure 3 can be obtained

$$r_x \approx 3.5\ \Omega \quad (12)$$

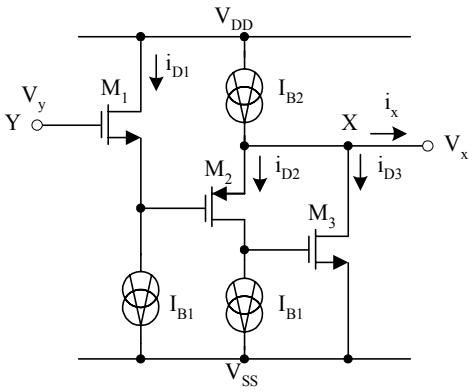

Fig. 3 The proposed circuit to reduce the resistance at port X

The proposed CMOS-based CCII+ circuit is shown in figure 4. The transistors are all match and operated in their saturation regions. The transistors M_1 and M_2 function a voltage follower which accurately transfer the voltage at port Y to port X. The transistor M_3 is used to reduce the resistance at port X. If $V_y > 0$ and R_x is a given resistance connected at port X, the signal current $i_x = V_y/R_x$ will flow out at port X. The transistor M_4 and the current source I_{B3} are used to duplicate the current at port X (i_x) to port Z (i_z) that can be explained as followed.

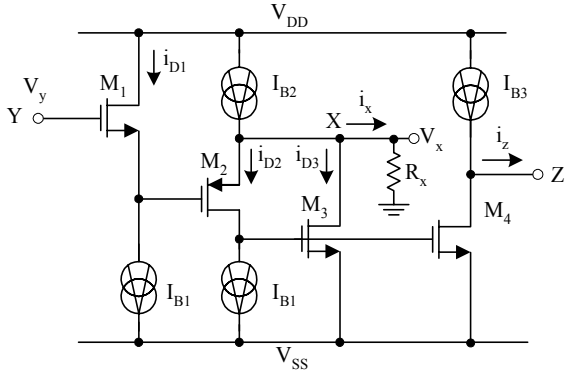

Fig. 4 The proposed CCII+ circuit

At port X, the drain current of the transistor M_3 can be given by

$$i_{D3} = I_{B2} - i_{D2} - i_x \quad (13)$$

Based on the Eq.(1), the gate-to-source voltage of the transistors M_3 and M_4 are equal, so the drain current of the transistor M_3 is equal to the drain current of the transistor M_4. Substituting this result and the Eq.(5) into Eq.(13), the drain current M_3 can be written as

$$i_{D3} = i_{D4} = I_{B2} - I_{B1} - i_x \quad (14)$$

The current flowing out at port Z is simply expressed as

$$i_z = I_{B3} - i_{D4} \quad (15)$$

Substituting Eq.(14) into Eq.(15), we have

$$i_z = I_{B3} - I_{B2} + I_{B1} + i_x \quad (16)$$

If $I_{B3} = I_{B2} - I_{B1}$, the current at port Z (i_z) can be given by

$$i_z = i_x \quad (17)$$

It is clearly seen that the current i_z is in the same direction as the current i_x. Therefore, the circuit in figure 4 that realizes CCII+ and this case k = +1.

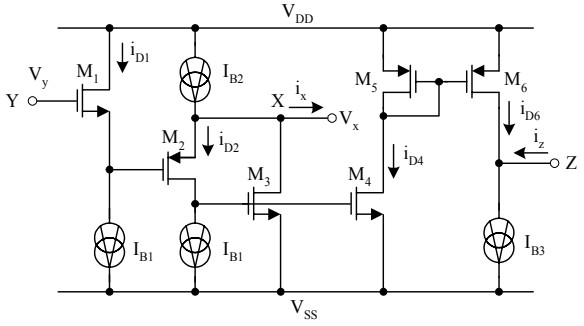

Fig. 5 The proposed CCII- circuit

Figure 5 shows CCII-, which is directly adapted from the circuit in figure 4. In this circuit, the transistors M_5 and M_6 are the current mirror that reflect the drain current of the transistor M_4 (i_{D4}) to port Z. Then the difference of i_{D6} and I_{B3} is the current i_z that flow in the opposite direction of the current i_x. It can be expressed as

$$i_z = -i_x \quad (18)$$

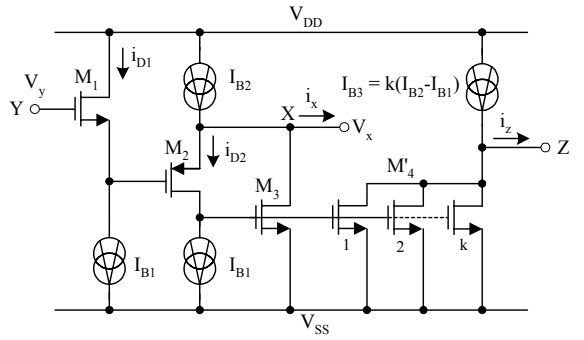

Fig. 6 The CCII+ with the current gain k

In practice, the usefulness of the current conveyor can be further extended if the current transfer ratio is not restricted only to the case of k = ±1 [6]. Figure 6 shows the current conveyor, which is modified from the circuit in figure 4 for the current gain equal to +k. The current gain k is achieved by replacing the transistor M_4 by a multiple transistor M_4', in which k transistors are connected in parallel. It should be noted that the current source I_{B3} is now set to $k(I_{B2}-I_{B1})$. Alternatively, the current gain k can be set through the transistor geometry by designing the ratio of channel width and length (W/L) of the transistor M_4.

It can be seen clearly from the above explanation that the three transistors are stacked in the path of the transistors M_1, M_2 and M_3 in figure 6. Then the power supply voltage can be down to ±1.5V.

3. SIMULATION RESULTS

The performances of the proposed circuit were studied by using PSPICE analog simulation program. The BSIM MOS model of the 0.5μm CMOS process was used in the circuit simulation. The ratio of channel width and length (W/L) of the devices are shown in Table 1. The supply voltage $V_{DD} = -V_{SS} = 1.5V$. The current source I_{B1}, I_{B2} and I_{B3} are set to 10μA, 60μA and 50μA, respectively. Figure 7 shows the simulation results of the transfer characteristic between V_y and V_x.

Table 1 The ratio of channel widths and lengths

Device	W/L(μm)
M_1	8/1
M_2	31.5/1
M_3,M_4	32/1

The voltage swing at port X is limited by the gate-to-source voltage V_{GS3} of transistor M_3. Figure 8 shows the plot of V_x against frequency, which has the bandwidth beyond 326MHz. The transfer characteristic between i_x and i_z is shown in figure 9. It should be noted that the dynamic range is limited by the current source I_{B3}. The frequency characteristic of the current transfer i_z is shown in figure 10. The bandwidth extends beyond 310MHz.

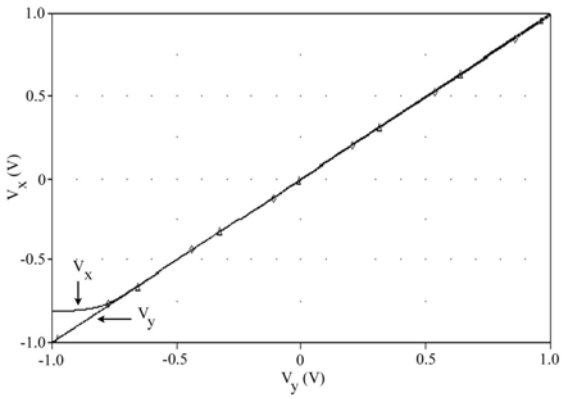

Fig. 7 The transfer characteristic between V_x and V_y

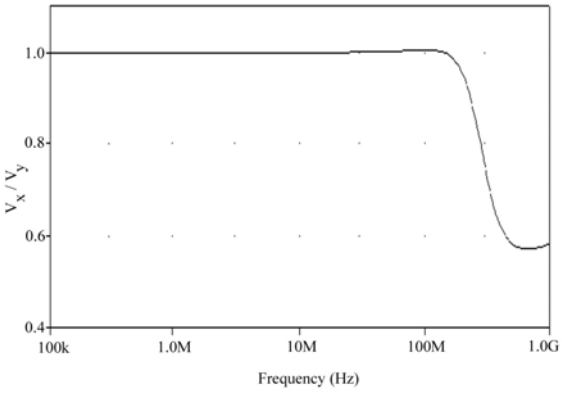

Fig. 8 The frequency characteristic of the voltage transfer

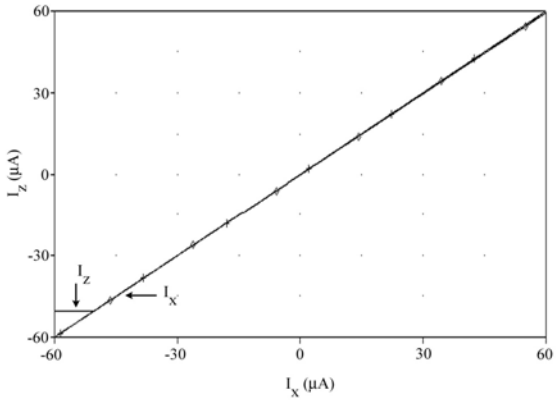

Fig. 9 The transfer characteristic between i_z and i_x

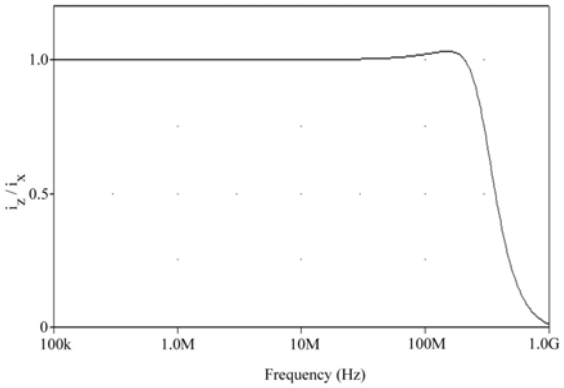

Fig. 10 The frequency characteristic of the current transfer

4. CONCLUSION

This paper describes a low-voltage and low resistance at port X of CMOS CCII. The circuit configuration is simple and small in size. The realization method is suitable for fabrication using standard CMOS process. The transfer characteristic and frequency response of the proposed circuit are included.

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