Four Quadrant CMOS Current Differentiated Circuit

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Abstract: In this literature, the CMOS current mode fout quadrant differentiator circuit is proposed. The implementation is base on an appropriate input stage that converts the input current into a compressed voltage at the input capacitor (C_{gs}) of the CMOS driver circuit. This input voltage use as the control output current which flow to the output node by passing through a MOS active load and use it as the feedback voltage to the input node. Simulation results with level 49 CMOS model of MOSIS are given to demonstrate the correct operation of the proposed configuration. But the gain of the circuit is too low so the output differentiate current also low. The proposed differentiator is expected to find several applications in analog signal processing system.

Keyword: CMOS circuit, Signal Processing

1. Introduction

A current mode differentiator is a circuit which develops an output voltage that is substantially in proportion to the rate of change of theinput current. This type of circuit substracts over time. The type of wave on its input current and the frequency of that signal determine the output current. This is because both the shape and the frequency of a signal affects how fast the wave's current is changing. Whether the frequency is consider "high" or "low" is base on the time constant which, in turn, is base on the differentiator's RC value. [1][2] The differentiators's output current increases as the frequency increases. As a result, the current differentiator has the frequency response of a high pass filter.

Differentiator circuit for continuour signals as opposed to sampled signals are well known and may comprise marely a series capacitor and shunt resistor of the resistor may form a feedback path for an operational amplifier. Neither form is particularly convenient for implementation in integrated form, i.e. as a part of an integrated circuit. The circuit idea is shown in figure 1.

The circuit to the right shows an amplifier connected as a differentiator. Since the input circuit element is a capacitor, this circuit will only experience input current in response to changes in input voltage — the faster and larger the change in input voltage which cause by the input current into R1, the greater the input current, therefore the greater the output voltage in response and also the greater output current to the load.
Since the output voltage will reflect the rate of change of the input, this circuit will indeed perform differentiation.

The "d/dt" notation indicates differentiation with respect to time. If you're not familiar with differential calculus, don't worry about it here; you won't need it for these pages.

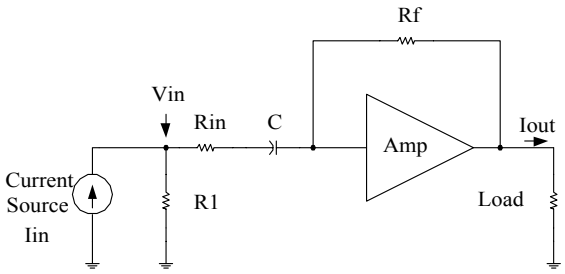

Figure 1. Current differentiator circuit idea

The op-amp differentiator [3] is not used in any analog computer application, and indeed not generally. The basic reason for this is that high-frequency noise signals will not be suppressed by this circuit; rather they will be amplified far beyond the amplification of the desired signal.

In some applications, it may be possible to add a series input resistor, as shown in the schematic diagram to the right. This limits the high frequency gain of the circuit to the ratio R_f/R_1. The low frequency gain is still set by R_f and C, as before. The cutoff frequency, where these two effects meet, is determined by R_1 and C, according to the expression: $f_{CO} = \frac{1}{2} R_1 C$

Higher-frequency signals are still amplified more than low-frequency signals, so any noise present in the circuit will still be amplified more than the desired signal. If an application can

suppress such noise and doesn't require higher-frequency components, this modified circuit may serve the need. In other cases, if differentiation is absolutely required, a passive RC circuit is generally used instead, and the inevitable signal losses compensated later.

2. Circuit Description

In this literature, an implement of simple CMOS transistor differentiator is proposed as shown in figure 2. For this proposes, we considered the following requirements: the input current into compressed voltage at the capacitor node and simultaneously the availability of the capacitor's current as the drain current of a MOS transistor. In order to achieve the above requirements an appropriate input stage is presented.[4]

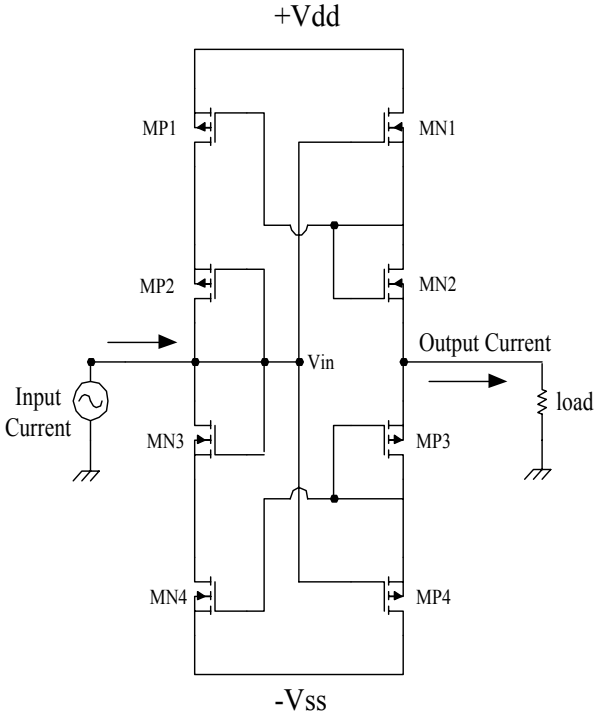

Figure 2. The implemented CMOS differentiator Circuit

The input current is convert to the input voltage by MN3 and MP2. This voltage is used to control the drain current of MP4 and MN1. When this current flow through the MP3 and MN2 it cause the voltage V_{DS} and use it as the feedback voltage to the input node. The current transfer function of the circuit is shown in equation 1.

$$I_{Out} = \left[\frac{R_{dsMP2} \cdot R_{dsMN3}}{R_{dsMP2} + R_{dsMN3}}\right]\left[\frac{C_{gsMP2} \cdot C_{gsMN3}}{C_{gsMP2} + C_{gsMN3}}\right]\frac{dI_{IN}}{dt} K \quad (1)$$

where K is the gain or loss of the circuit as shown in equation 2

$$\frac{\left[\begin{array}{l} g_{mMN1} g_{mMP3}\left[\begin{array}{l}(g_{mMP4} + s(C_{gsMN2} + C_{gsMP2}))\\ (g_{mMP4} + s(C_{gsMP4} + C_{gsMN2}))\end{array}\right] + \\ g_{mMP2} g_{mMP3} g_{mMN1}\left[g_{mMN3} + s(C_{gsMP2})\right]\end{array}\right]}{\left[\begin{array}{l}(g_{mMP2} + g_{mMN1})(g_{mMN3} + s(C_{gsMN2} + C_{gsMP4}))(g_{mMN4} + \\ (C_{gsMN1} + C_{gsMN2}))(g_{mMN3} + s(C_{gsMP3} + C_{gsMP4})) + g_{mMN3}\end{array}\right]} \quad (2)$$

From equation 1 the circuit can differentiate the input current with the time constant that depend on the input capacitor of the driver MOS and the parallel input resistor of the saturate MOS. But the gain of the circuit from equation 2 is too low because of the g_m or device transconductance parameter of the MOS is lower than the channel resistor.

3. Simulation results

Spice circuit simulation program is used as the tool. The level 49 AMI 0.5 μm.model of MOSIS Integrated Circuit Fabrication Service is used. Some special parameter of the MOSFET model is shown in table 1.[5][6]

Table 1 Some special electrical parameter of the MOS model

Parameter	NMOS	PMOS
Vth	0.76 V	-0.93V
Gamma	0.5 $V^{1/2}$	0.58 $V^{1/2}$
K'	55.5uA/V^2	-18.3 uA/V^2
Low field mobiility	462 cm^2/V.s	152 cm^2/V.s
CGSO	2.67E-10	3.71E-10
CGBO	1 E-10	1 E-10

We set the input current signal to be pure sine wave, triangle with flat top and square wave. The output current signal that flow through the load resistor is shown in figure 3.

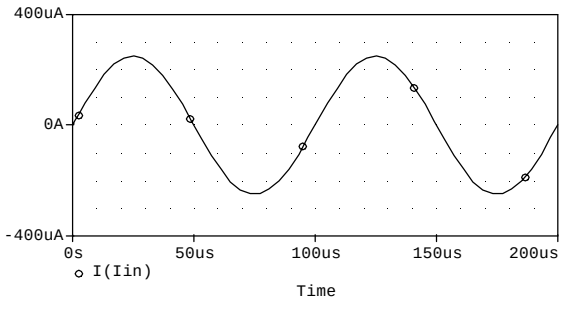

Figure 3A The input sine current with 250 μA_{PP}

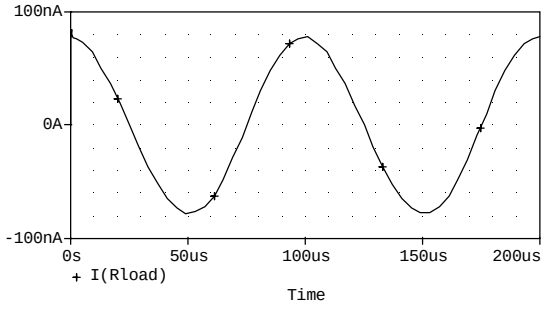

Figure 3B The output current of the sine current Input

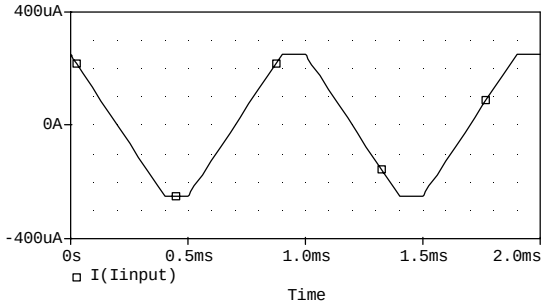

Figure 3C The input current triangle with flat top

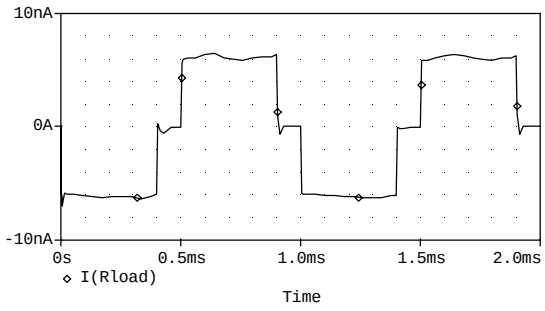

Figure 3D The output current of the input current of 3C

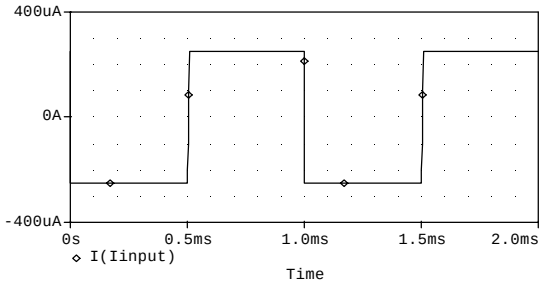

Figure 3E The input square wave current

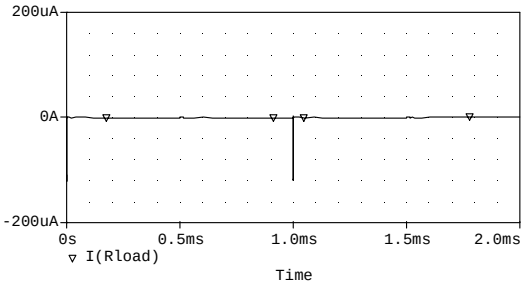

Figure 3F The output current of figure 3E

The peak current of the input current signal of each input is 250 μA_{PP} but the output current that flow through the load resistor is too low. This is the effect from the gain of the circuit

From the experimental results the output current is the differentiate value of the input current From figure 3F and 3D the high frequency of the triangle and square wave can pass the circuit to the output node this confirm that the circuit also act as the high pass filter

4. Conclusion

A current mode CMOS differentator circuit is present. The output current of the circuit can differentiate the input current. The gain of the circuit is too low, so the output differentiate current value is not the correct value. It need to improve the output current value by adjust the MOS parameters in the equation 2.

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