A high-speed algorithmic ADC based on Maximum Circuit

Amphawan Chaikla, Tattaya Pukkalanun, Vanchai Riewruja,
Chaleompun Wangwiwattana, and Ruedee Masuchun

Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang, Ladkrabang, Bangkok, Thailand
(Tel: +66-2-739-2406-7; E-mail: vanchai@cs.eng.kmitl.ac.th)

Abstract: This paper presents a high-speed algorithmic analog-to-digital converter (ADC), which is based on gray coding. The realization method makes use of a two-input maximum circuit to provide a high-speed operation and a low-distortion in the transfer characteristic. The proposed ADC based on the CMOS integrated circuit technique is simple and suitable for implementing a high-resolution ADC. The performances of the proposed circuit were studied using the PSPICE analog simulation program. The simulation-results verifying the circuit performances are agreed with the expected values.

Keywords: gray code ADC, algorithmic ADC, maximum circuit, CMOS-based circuit

1. INTRODUCTION

An analog-to-digital converter (ADC) is an important circuit building block in a mixed analog-digital system. It can be used as a component in many applications such as radar systems, TV and video systems, digital telephony, computerized control systems, and instrumentation systems. Since ADC is a small part of the whole system, it should be simple and small in size. Moreover, low-power consumption and high-speed performance become necessary. For high-speed ADC, the parallel conversion method offers the highest speed performance. However, the parallel conversion ADC has a circuit complexity and spends a large portion of the chip area. In recent years, the demand of high performance, portable and battery-powered equipment arises causing a strong motivation to implement both analog and digital circuit on the same chip using a standard CMOS process. The studies have shown that among the existing ADCs, the algorithmic ADC offers the advantages of both the circuit performance and smaller size of chip area [1]-[4]. In addition, the algorithmic ADC starts its conversion from the most significant bit (MSB) and continues its action successively bit by bit. Thus, the N-bit resolution of an algorithmic ADC can be simply realized by cascading of N-bit cells. There are two techniques to implement an algorithmic ADC, one is binary coding and the other is gray coding. For binary coding, the conversion technique requires the subtract function to generate a sawtooth-like waveform for a linearly increasing input signal. The current mode binary code algorithmic ADC has been also proposed in literature [1]-[2]. The configuration of these approaches is simple and can be realized with a minimum chip area. However, two major limitations of the binary code algorithmic ADC are determined. Firstly, the accumulation of a signal error, occurred during the bit generation, deteriorates the accuracy of the ADC and limits the resolution of the ADC. Secondly, the finite bandwidth of the subtract-function circuit causes the distortion on the subtracted signal due to the broad frequency spectrum of the sawtooth-like waveform. Therefore, a high-speed performance of the ADC is limited. To minimize the disadvantages of such ADC, an algorithmic ADC based on gray coding technique has been introduced [3]-[4]. The transfer characteristic of gray code algorithmic conversion is triangular-like waveform. The advantage of gray code algorithmic ADC is that the accumulated error is smaller than that of a binary code one [4]. The realization of a MOS gray code algorithmic ADC can be implemented using current mirrors, current comparators [5], and the analog switches [3].

However, the accuracy and the conversion speed of this ADC are yet limited by the delay, caused by the current mirror operated in class B, and the distortion, caused by the overlap operation of the analog switches.

The purpose of this paper is to propose a CMOS circuit technique for the realization of an algorithmic ADC. The technique is based on gray coding which utilizes the maximum circuit to achieve a high-speed operation and high-accuracy. Consequently, the proposed ADC is suitable for realization a high resolution ADC.

2. CIRCUIT DESCRIPTION

2.1 Principle of gray code ADC

An algorithmic analog-to-digital conversion technique based on gray coding can be described by the flow chart shown in Fig. 1(a), where I_{ref} is a reference signal and i_{in} is an analog input signal, which has a value between zero and the reference I_{ref}. The input signal i_{in} is amplified by a factor of two to generate a signal $2i_{in}$. The $2i_{in}$ signal is compared with the reference I_{ref}. If $2i_{in}$ is less than I_{ref}, a digital output D_o is set to low and $2i_{in}$ becomes the analog output signal. Otherwise, the digital output D_o is set to high and the analog output signal is then generated by subtracting the $2i_{in}$ from $2I_{ref}$. This analog output signal can fed either back to the input or onto a following identical cell to generate another bit of resolution. Consequently, the transfer characteristic of the gray code algorithmic analog-to-digital conversion is a triangular-like waveform for continually increasing the input signal as shown in Fig. 1(b). It should be noted that the algorithmic ADC starts its conversion from the most significant bit (MSB) and continues its action successively bit by bit.

2.2 Two-input maximum circuit

Fig. 2 shows the circuit diagram of two-input maximum operation [6]. The implementation of this circuit is based on the shared gate-source voltage corresponding to the saturation value imposed by the maximum input current. The transistors M_6-M_8 and M_{11}-M_{13} form as the maximum selector. The transistor M_{15} and the bias current I_{bias} provide the bias voltage V_{bias} approximately equal to $3V_T$, where V_T is the threshold voltage M_6-M_8, and M_{11}-M_{13} are forced to the edge of conduction to minimize the crossover distortion. The diode connected transistor M_{14} and the transistor M_{16} form as the unity gain current mirror to capture the maximum current i_{max} to output node. The operation of maximum circuit in Fig. 2 can be explained as follow.
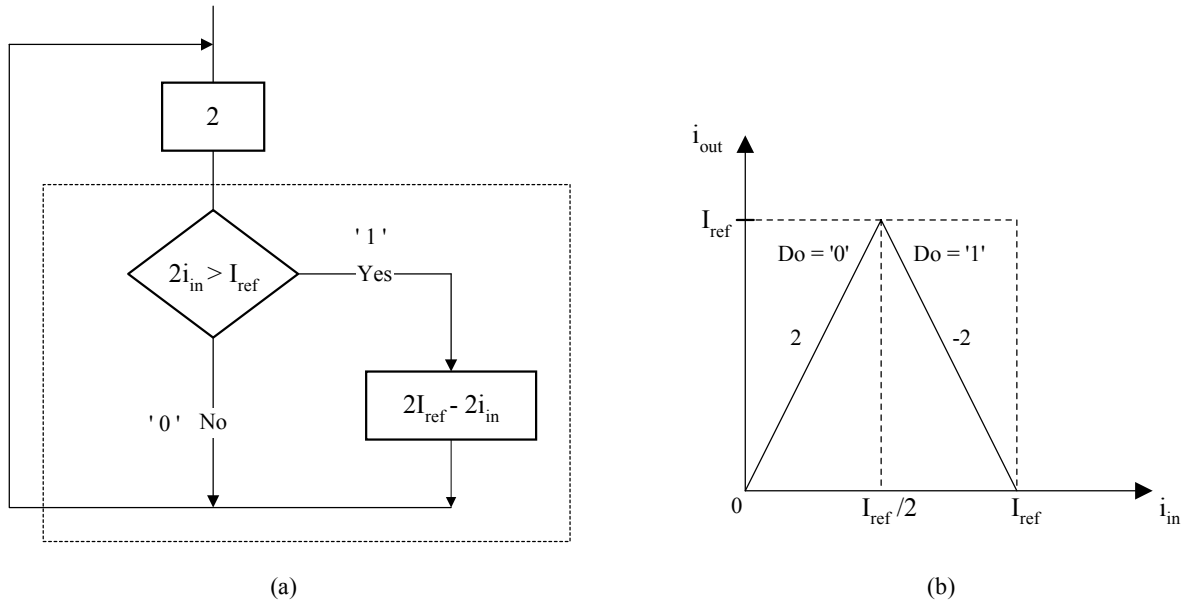
(a)

(b)

Fig. 1 Principle of gray code algorithmic conversion
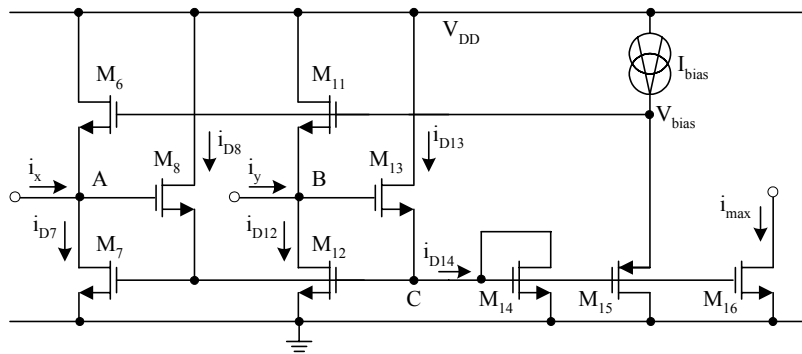(a) flow chart
(b) transfer characteristic

Fig. 2 The two-input maximum circuit

The transistors are all matched and operated in their saturation regions. The drain current of NMOS transistor operated in saturation region is expressed as [7]

$$i_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (v_{GS} - V_T)^2 = K (v_{GS} - V_T)^2 \qquad (1)$$

where K, v_{GS}, and V_T are the device transconductance parameter, the gate-source voltage, and the threshold voltage, respectively.

Suppose that the current i_x is grater than the current i_y ($i_x > i_y$), which can be stated as

$$i_x = \max(i_x, i_y) \qquad (2)$$

The voltages at node A and node B are established by the currents i_x and i_y, respectively. Thus the voltage v_A is also greater than the voltage v_B. The gates of transistor M_7, M_{12}, and M_{14} are connected together. Then, their gate-source voltages can be given by

$$v_{GS7} = v_{GS12} = v_{GS14} \qquad (3)$$

Based on Eqs. (1)~(3), the transistors M_7, M_{12}, and M_{14} have the same drain current as

$$i_{D7} = i_{D12} = i_{D14} = i_x \qquad (4)$$

In saturation, the current i_{D12} flows through the transistor M_{12} increasing the gate-source voltage of the transistor M_{12}, which effects the transistor M_{13} to cutoff. Therefore the drain currents i_{D13} can be stated as

$$i_{D13} = 0 \qquad (5)$$

Considering at node C, the drain current i_{D14} can be written as

$$i_{D14} = i_{D8} + i_{D13} \qquad (6)$$

Substituting Eq. (5) into Eq. (6), the drain current i_{D14} can be rewritten as

$$i_{D14} = i_{D8} = i_{D7} = i_x \tag{7}$$

The current i_{D14} is mirrored into maximum output node by the current mirror M_{14} and M_{16}. Then the current i_{max} can be given by

$$i_{max} = i_{D14} = i_x = \max\left(i_x, i_y\right) \tag{8}$$

The above discussion verifies the maximum operation of the circuit in Fig. 2.

2.3 The proposed ADC

The proposed one-bit cell gray-code algorithmic ADC circuit is shown in Fig. 3. The decision block inside the dashed line frame in Fig. 1(a) is replaced by the two-input maximum circuit, the reference current I_{ref}, and the current mirrors M_4-M_5, M_9-M_{10}, M_{17}-M_{18}, as shown in Fig. 3. The transistors M_1-M_3 form a dual-output negative current mirror with the current gain equal to two. The transistors M_{19}-M_{24} function as a current comparator [5] used to compare the current i_{D19} with the current i_{D20} to generate the digital output. Consider the circuit in Fig. 3, the currents i_{in} and I_{ref} are the input signal and the reference current, respectively. The operation of the proposed circuit can be explained as follow.

The input signal current i_{in} is multiplied by a factor of two using the current mirror M_1-M_3, where the channel width of transistors M_2 and M_3 are twice compared to transistor M_1's. The two-input maximum circuit generates the analog output signal i_{out} and the digital output signal V_{out} at node F and node I, respectively according to compare the new signal current $2i_{in}$ with the current I_{ref}. From the maximum operation, the current i_{max} can be stated as

$$i_{max} = \begin{cases} I_{ref} & ; 2i_{in} < I_{ref} \\ 2i_{in} & ; 2i_{in} \geq I_{ref} \end{cases} \tag{9}$$

The current i_{D8} is mirrored to node D using the unity-gain current mirror M_9-M_{10}. Thus, the current i_a can be given by

$$i_a = i_{D10} - i_{D13} = i_{D8} - i_{D13} \tag{10}$$

Considering at node E, the current i_{D17} can be expressed as

$$i_{D17} = i_{max} - I_{ref} \tag{11}$$

The unity-gain current mirror M_4-M_5 and the double-gain current mirror M_{17}-M_{18} reflect the current $2i_{in}$ and i_{D17} to node F, respectively. Thus, the output current i_{out} can be written as

$$i_{out} = i_{D5} - i_{D18} = 2i_{in} - 2i_{D17} \tag{12}$$

Substituting Eq.(11) into Eq.(12), we obtain

$$i_{out} = 2i_{in} - 2\left(i_{max} - I_{ref}\right) \tag{13}$$

Substituting Eq.(9) into Eq.(13), the analog output current i_{out} can be rewritten as

$$i_{out} = \begin{cases} 2i_{in} & ; 2i_{in} < I_{ref} \\ 2I_{ref} - 2i_{in} & ; 2i_{in} \geq I_{ref} \end{cases} \tag{14}$$
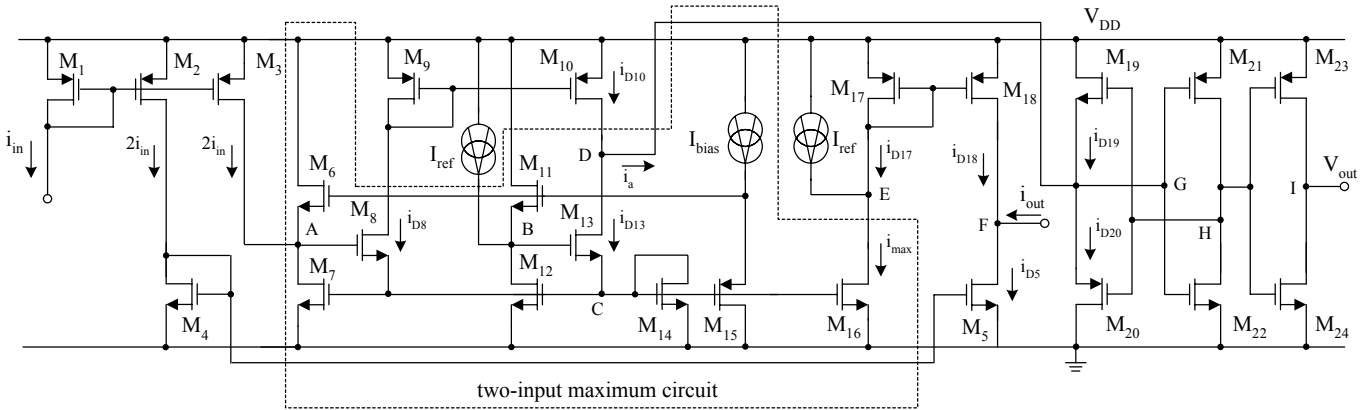

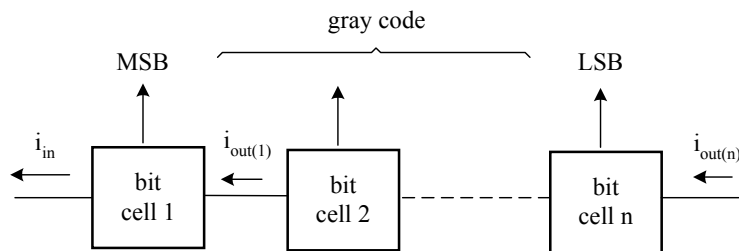Fig. 3 The proposed one-bit cell Gray ADC

Fig. 4 The N-bit resolution ADC

Consequently, if $2i_{in} < I_{ref}$, the current i_a is equal to the current $-i_{D13}$ or $-I_{ref}$ and flows through the current comparator M_{19}-M_{24}. The current i_{D19} is equal to the reference current I_{ref} and the current i_{D20} is zero. Then the output voltage V_{out} of the current comparator is set to low. For the case of $2i_{in} \geq I_{ref}$, the currents i_{D19} and i_{D20} are forced to be zero and $2i_{in}$, respectively. Thus the output voltage V_{out} goes high.

For the N-bit resolution, the N proposed circuits are cascaded with the analog output of one circuit connecting to the analog input of the following circuit as shown in Fig. 4.

3. SIMULATION RESULTS

The performances of the proposed circuit were observed through the use of PSPICE analog simulation program. The BSIM MOS model of the 0.5μm CMOS process was used for the circuit simulation. The ratios of the channel width and length (W/L) of the devices used are shown in Table 1. The reference current I_{ref}, and the bias current I_{bias} are set to 50μA and 10μA, respectively. The supply voltage V_{DD} is set to 3.3V. Fig. 5 shows the DC transfer characteristic of the proposed circuit and the digital output voltage for the input

signal current, which is varied from 0 to 50μA. It is apparent that the circuit exhibits low distortion of the transfer characteristic. The frequency response of the circuit is shown in Fig. 6. It should be noted that a bandwidth of approximately 165MHz is observed. A four-bit resolution ADC formed by cascading four proposed circuits was used to verify the conversion performance. Fig. 7 shows the output waveform that monitored from the analog output of the least significant (LSB), or from the fourth bit cell of the four-bit ADC. It is evident that the circuit operates with high accuracy over the entire dynamic range.

Table 1 Dimensions of the MOS Transistors

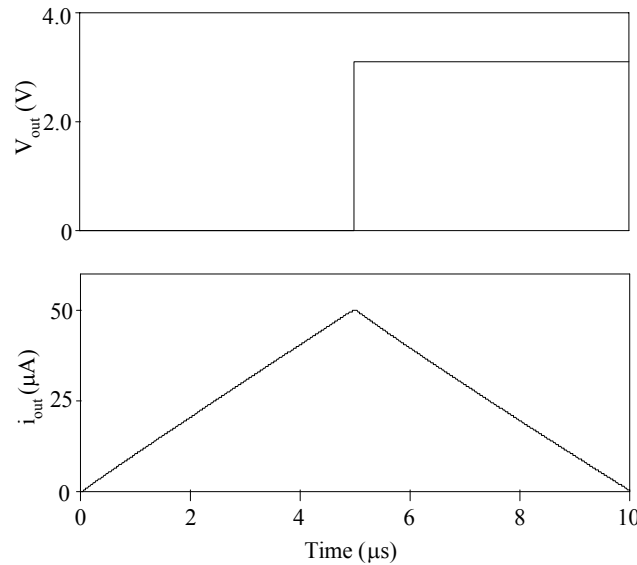| Transistors	W(μm)/L(μm)
M_2, M_3, M_4, M_5, M_{18}	20/1
M_1, M_8, M_{13}, M_{17}	10/1
M_6, M_7, M_{11}, M_{12}, M_{14}, M_{16}	4/1
M_9, M_{10}, M_{21}, M_{22}, M_{23}, M_{24}	2/1
M_{15}, M_{19}, M_{20}	1.2/0.5

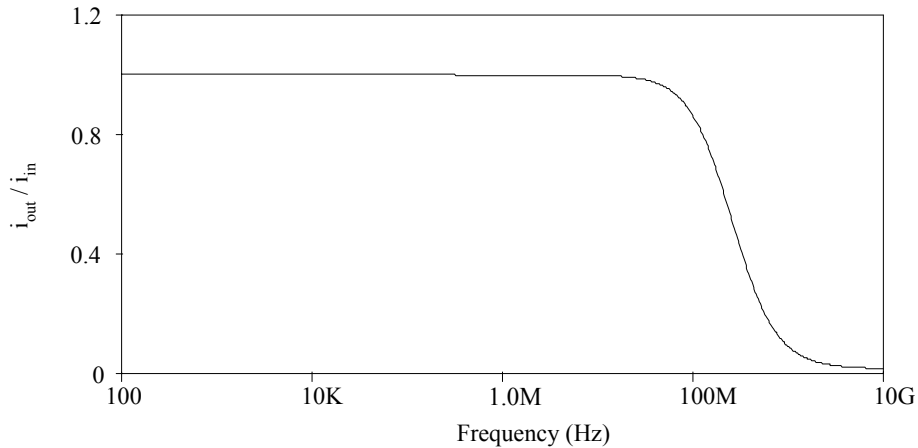Fig. 5 DC transfer characteristic and digital output
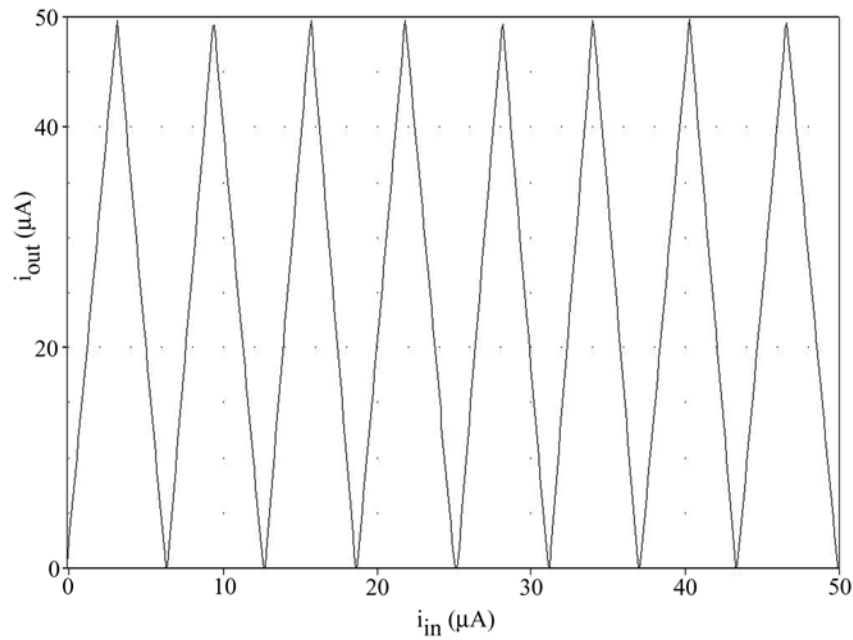

Fig. 6 Frequency Response

Fig. 7 Analog output of the fourth bit cell

4. CONCLUSION

This paper describes a CMOS integrated circuit technique for realizing an algorithmic analog to digital converter using the current-mode two-input maximum circuit. The DC transfer characteristic of the proposed ADC shows a good linearity and low distortion over an entire dynamic range. The proposed ADC is simple and suitable for realization a high resolution ADC. An N-bit resolution ADC can be achieved by cascading of N proposed circuits. PSPICE simulation results validating the circuit performances are agreed with the proposed technique.

REFERENCE

[1] K. Anuntahirunrat, W. Surakampontorn, and V. Riewruja, "One-bit algorithmic A/D based on nonlinear circuit", *Proc.RESTECS'96 KMITL*, pp. E81-E87, 1996.

[2] N Nairn, D.G., and Salama, C.A.T., "Algorithmic analogue/digital convertor based on current mirrors", *Electronics Letters*, Vol. 24, No.8, pp.471-472, April 1988.

[3] P.O. Pouliquen, K.A. Boahen, and A.G.Andreou, "A Gray-code Mos Current-mode analog-to-digital converter design", *IEEE International Symposium on Circuit and Syst.*, Vol.4, pp.1924-1927, 1991.

[4] S. Signell, B. Jonsson, H. Stetrom, and T. Nianxiong, "New A/D Converter Architectures Based on Gray Coding", *Proceedings of 1997 IEEE International Symposium on Circuits and Systems, 1997. ISCAS '97*, Vol.1, pp.413-416, 1997.

[5] D.A. Freitas, and K.W. Current, "CMOS current comparator circuit", *Electronics letters*, Vol.19, pp. 695-697, 1983.

[6] C. Pojanasuwanchai, C. Wangwiwattana, A. Chaikla, V. Riewruja, and P. Julsereewong, "Fuzzy Multiple-Input Maximum Circuit in Current-mode", *SICE Annual Conference in Fukui*, Japan, pp. 571-575, 2003.

[7] Paul R. Gray, and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuit*, charter 1, John Wiley &Sons, Inc., 1993.