A Current-mode Multiple-Input Minimum Circuit For Fuzzy Logic Controllers

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Abstract: This paper presents a current-mode multiple-input minimum circuit. The proposed circuit can be implemented by applying De Morgan's law. The circuit diagram is simple and modular. It operates using a single 2.5V supply and has very low dissipation. The realization method is suitable for fabrication using CMOS technology and all transistors are operated in their saturation region. The performances of this proposed circuit were studied using the PSPICE analog simulation program. The simulation results show the approval of this circuit that it has adequate basic performances for a real-time fuzzy controller and a fuzzy computer.

Keywords: current-mode circuit, minimum circuit, CMOS-based circuit, fuzzy logic controller

1. INTRODUCTION

The applications of fuzzy logic and fuzzy algorithm in real-time systems are accepting much attention [1]. In recent years, the demand of the real time systems in term of high-speed operation, high-efficiency performance, and lower power consumption arises causing a strong motivation to implement fuzzy based hardware. In literature, the hardware implementation of fuzzy systems can be categorized into the digital approach [2] and the analog approach [3-5]. The digital approach is superior to the analog approach in accuracy, extension, and ease of design. On the other hand, the analog circuits have higher speed and lower power consumption than their digital counterparts. The most significant fuzzy logic functions for realizing fuzzy systems are the maximum and minimum circuits. For fuzzy systems employing, these two functions are used in many applications [3-5]. In the past, the realization of maximum and minimum functions in analog circuit form have been implemented using either a second generation current conveyor (CCII) [3] or an operational transconductance amplifier (OTA) [4] as a basic active circuit element. These approaches require diode function as an electronic switch to eliminate undesirable signal to provide maximum and minimum operations. However, the high-speed performance of these approaches is limited by the delay caused by the transition between "on" and "off" state of diodes. The dynamic range of the OTA-based maximum and minimum circuits are also limited by the input stage of an OTA. Other approaches are based on the use of CMOS circuit technique to perform maximum and minimum functions [5, 8-10].

For implementing a fuzzy logic controller or fuzzy processor by employing maximum and minimum functions, the multiple input maximum and minimum circuits are needed [6-7]. The problems of using the binary tree structure based on the two-input maximum and minimum circuit [8] to implement the multiple input maximum and minimum circuits are accumulated errors and low operation speed. To minimize these disadvantages, the one-stage multiple-input maximum and minimum circuits have been proposed in literature [9-10]. The disadvantage of these approaches is the change between the saturation and non-saturation region of the operation regions in MOS transistors that causes the distortion on the output signal and limits the operating speed.

In this paper, the current-mode multiple-input minimum circuit based on De Morgan's law [11] is proposed. The proposed circuit can be implemented using an n-input maximum circuit and n+1 complement circuits. Where n is the number of current input signals. The proposed circuit operates using a single 2.5V supply and provides high accuracy and high-speed. Simulation results supporting the characteristics of the proposed n-input minimum circuit are also included.

2. CIRCUIT DESCRIPTION

From basically design of the proposed circuit, the transistors are all matched and operated in their saturation regions. The drain current of NMOS transistor operated in saturation region is expressed as [12]

$$i_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(v_{GS} - V_T\right)^2 = K\left(v_{GS} - V_T\right)^2 \quad (1)$$

where K, v_{GS}, and V_T are the device transconductance parameter, the gate-source voltage, and the threshold voltage, respectively.

2.1 Principle of minimum operation

The minimum operation is related to the maximum operation by De Morgan's law as [11]

$$\min\left(i_1, i_2, ..., i_n\right) = \overline{\max\left(\bar{i}_1, \bar{i}_2, ..., \bar{i}_n\right)} \quad (2)$$

where $\bar{\bullet}$ is the fuzzy complement operation.

Consequently, the minimum operation can be implemented using the maximum operation and the fuzzy complement operation. The fuzzy complement operation can be expressed as

$$\bar{i}_j = I_R - i_j \quad (3)$$

where I_R is the reference current corresponding to fuzzy-grad 1. As Eq. (2) indicated in, the minimum output current i_{min} can be written as

$$i_{\min} = I_R - i_{\max} \quad (4)$$

According to Eq. (3) and Eq. (4), the complement circuits can be implemented using the current mirrors.

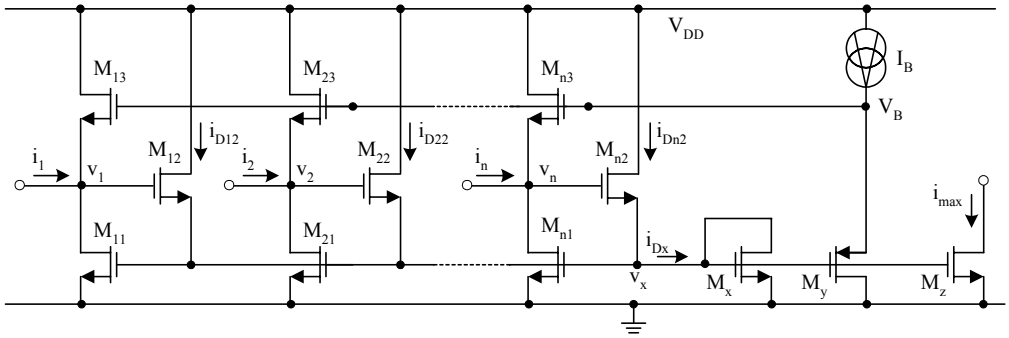


Fig. 1 The multiple-input maximum circuit

2.2 Multiple-input maximum circuit

The current-mode n-input maximum circuit [13] with a very sharp corner in the transfer characteristic is shown in Fig. 1. The transistors are all matched and operated in their saturation region. Each maximum cell for one input variable is composed of three transistors, M_{j1}, M_{j2}, and M_{j3}. The transistors M_{j1} and M_{j2} function as the current maximum selector. The transistor M_y and the bias current source I_B provide the bias voltage V_B approximately equal to $3V_T$, where V_T is the threshold voltage of the transistor. Therefore, the transistors M_{j1}-M_{j3} are forced to the edge of conduction to minimize the crossover distortion. The transistor M_x acts as the diode. The transistor M_z is connected to capture the maximum current to output node. The maximum operation of this circuit, based on the shared gate-to-source voltage corresponding to the saturation value imposed by the maximum input current, can be discussed as follow.

Suppose that there is only one maximum input current among i_1, i_2,…, i_n, and the current i_1 is the largest current, which can be stated as

$$i_1 = \max\left(i_1, i_2, \ldots, i_n\right) \tag{5}$$

The drain-source voltages v_1, v_2,…, v_n of the transistors M_{11}, M_{21},…, M_{n1} established by the input currents i_1, i_2,…, i_n, respectively. The drain-source voltage v_1 is established by the maximum input current i_1, thus the voltage v_1 is the maximum voltage. The gates of transistor M_{11}, M_{21},…, M_{n1}, and M_x are connected together. Then their gate-source voltages can be given by

$$v_{GS11} = v_{GS21} = \ldots = v_{GSn1} = v_x \tag{6}$$

Based on Eq. (1) and Eqs. (5)~(6), the transistors M_{11}, M_{21},…, M_{n1}, and M_x have the same drain current as

$$i_{D11} = i_{D21} = \ldots = i_{Dn1} = i_{Dx} = i_1 \tag{7}$$

In saturation, the current i_{D21} flows through the transistor M_{21} increasing the gate-source voltage of the transistor M_{21}, which effects the transistor M_{22} to cutoff. Similarly, The flow of i_{Dj1} through the transistor M_{j1} causes the transistor M_{j2} to cutoff. Therefore the drain currents i_{22}, i_{32},…, and i_{n2} can be given by

$$i_{D22} = i_{D32} = \ldots = i_{Dn2} = 0 \tag{8}$$

Considering at node v_x, the drain current i_{Dx} can be expressed as

$$i_{Dx} = i_{D12} + i_{D22} + \ldots + i_{Dn2} \tag{9}$$

Substituting Eq. (8) into Eq. (9), we obtain

$$i_{Dx} = i_{D12} = i_1 \tag{10}$$

The current i_{Dx} is mirrored into output node by the current mirror M_x and M_z. Then the maximum output current i_{max} can be given by

$$i_{\max} = i_1 = \max\left(i_1, i_2, \ldots, i_n\right) \tag{11}$$

The above discussion supports the maximum operation of the multiple current signals.

2.3 The proposed circuit

Fig. 2 shows the proposed current-mode multiple-input minimum circuit, which consists of the n-input maximum circuit and the complement circuits. The transistors are all matched and operated in their saturation region. Each simple minimum cell for one input variable is composed of five transistors, M_{j1}-M_{j5}, and the reference current source I_R. The transistors M_{j1}-M_{j3} function as the maximum cell. The transistors M_{j4}-M_{j5} form as the unity gain current mirror, which reflects each input current i_j to the complementation node v_j. The drain current of transistor M_{j5} can be written as

$$i_{Dj5} = i_j \tag{12}$$

Considering at complementation node v_j the input current of each maximum cell $\overline{i_j}$ can be expressed as

$$\overline{i_j} = I_R - i_j \tag{13}$$

At output node, the minimum output current i_{min} of the proposed circuit can be given by

$$i_{\min} = I_R - i_{\max} \tag{14}$$

It should be noted that the proposed circuit in Fig. 2 has De Morgan's law-based minimum operation as defined in section 2.1.

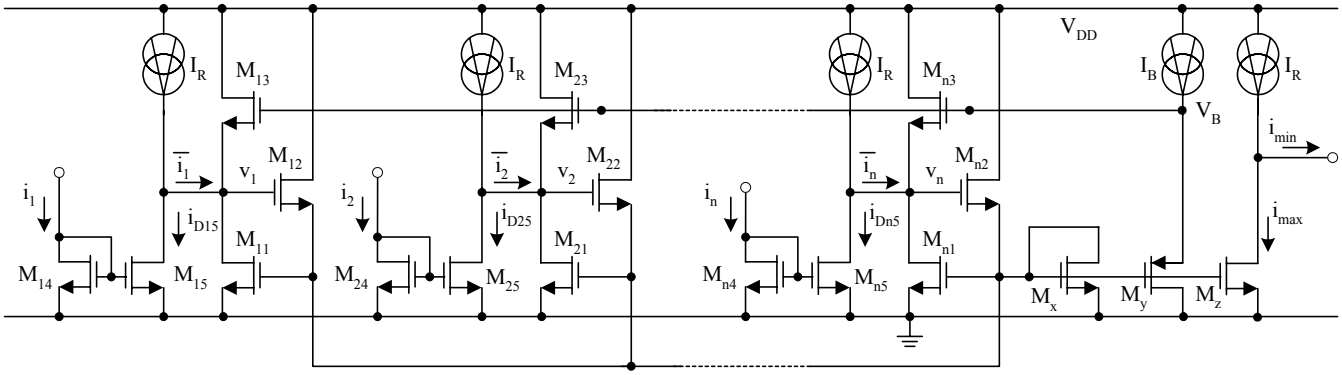


Fig. 2 The proposed multiple-input minimum circuit

3. SIMULATION RESULTS

The performances of the proposed circuit as shown in Fig. 2. were observed using PSPICE analog simulation program. The BSIM MOS model of the 0.5μm CMOS process was used for the circuit simulation. The dimensions W/L of the devices used in the proposed circuit are shown in Table 1. The bias current I_B and the reference current I_R were set to 10μA and 50μA, respectively. The single supply voltage V_{DD} used was 2.5V.

Table 1 Dimensions of the MOS Transistors

Transistor	W (μm)	L (μm)
M_{i2}, M_{i3}, M_y	5	1
M_{i1}, M_x,M_z	5	2

Fig. 3 shows the transient response of the proposed one-input circuit for the input current i_{in}. Where the input current i_{in} was varied from 0μA to 120μA. The reference current I_R was set to 100μA. The dynamic range of the proposed circuit is 100μA. The results show that the transfer characteristic of the proposed circuit is linear over an entire dynamic range. Fig. 4 and Fig. 5 show the simulated transient response of the proposed three-input and five-input minimum circuits, respectively. The triangular input currents are 50μA peak amplitude and 10μs time period. The results show that the output of the proposed circuit is almost consistent with the ideal case's. The maximum error is about 0.134% of full scale value (50μA).

To estimate the propagation delay of the proposed three-input minimum circuit, the transient performance of minimum operations were observed. The simulation results are given in Fig. 6, where the input current i_{in1} were the step-down function currents, and the input currents i_{in2}, i_{in3} were fixed at zero. The simulation curves in Fig. 6 show the results when the current i_{in1} were the step function currents from 10μA to 0μA, 20μA to 0μA, 30μA to 0μA, and 40μA to 0μA, respectively. It can be seen that the propagation delay of the minimum operation of the proposed circuit is about 7ns. It is evident that the proposed circuit has correct function and good performances.

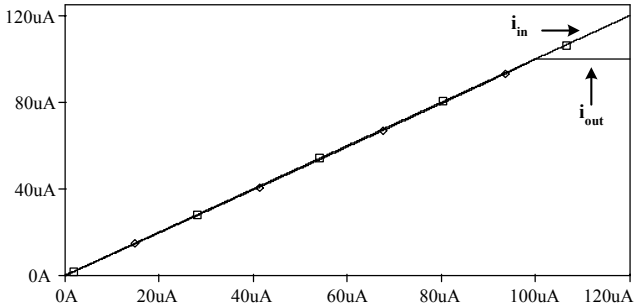
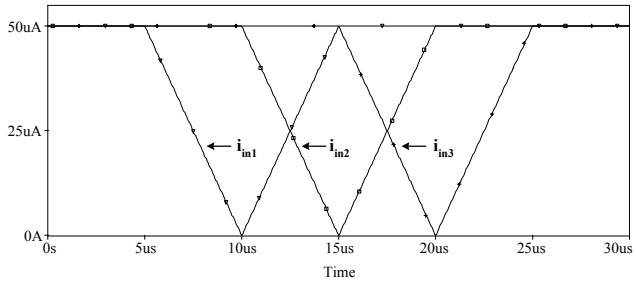
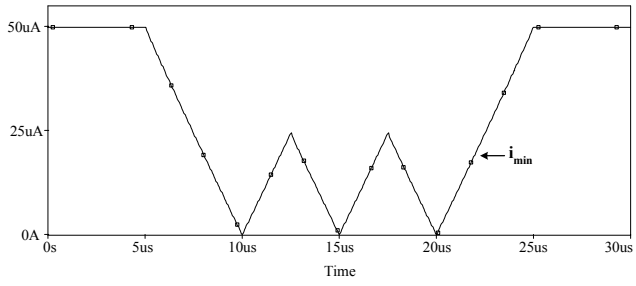


Fig. 3 Transient response of the one-input minimum circuit for the input current i_{in}.

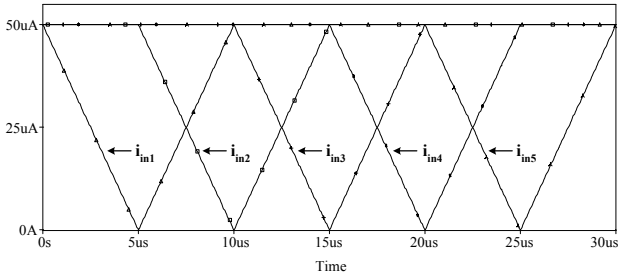


(a)

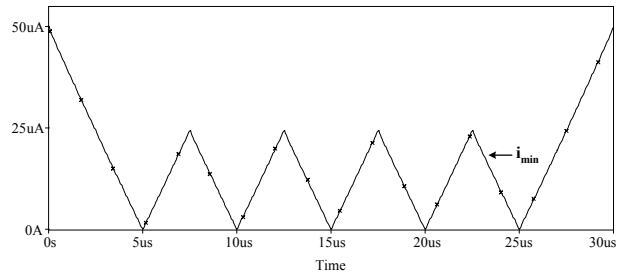


(b)

Fig. 4 Transient response of the three-input minimum circuit
(a) three triangular input currents
(b) the minimum output current



(a)



(b)

Fig. 5 Transient response of the five-input minimum circuit
(a) five triangular input currents
(b) the minimum output current

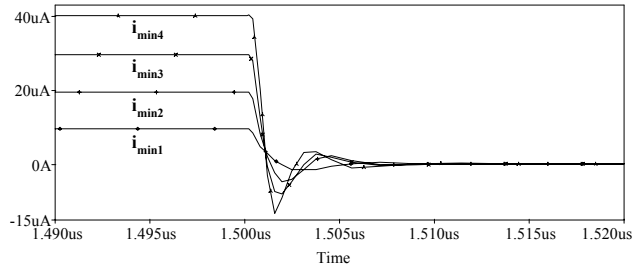


Fig. 6 Step responses of minimum operation

4. CONCLUSION

Based on De Morgan's law, the minimum operation is described. Using this technique, the CMOS-based multiple-input minimum circuit for fuzzy logic controller has been proposed. The proposed circuit was designed with 5n+3 transistors, where n is the number of inputs. This structure is simple and modular, so it can be easily expanded to meet the requirement of the number of multiple-input signals. Under single 2.5V supply voltage, the dynamic range of the proposed circuit can achieve up to 100μA and the propagation delay is about 7ns. The maximum error is about 0.134**%** of full scale current. From these simulation results it can be concluded that this proposed circuit, has sufficient basic performances suitable for a real-time fuzzy controller and a fuzzy computer.

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