Development of a Low Temperature Doping Technique for Application in Poly-Si TFT on Plastic Substrates*

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Abstract

A low temperature doping technique has been studied for application in poly-Si TFT's on plastic substrates. Heavily-doped amorphous silicon layers were deposited on poly-Si and the dopant atoms were driven in by subsequent excimer laser annealing. The entire process was carried out under a substrate temperature of 120°C, and a sheet resistance as low as 300 Ω/sq. was obtained.

1. Introduction

Flat panel display (FPD) devices constructed on flexible backplanes find a wide range of potential applications including wearable display, electronic paper, curved-surface displays. Plastic sheets, such as Poly-Ether-Sulfone (PES), are primary candidates for such a backplane owing to their flexibility, durability, and good light transmittance. However, most of these plastic materials have relatively poor thermal resistance, and the process temperature must be kept below the glass transition temperature of the plastics, usually under 150°C.

Especially, in the conventional poly-Si TFT process, not only the crystallization of the amorphous phase but also the dopant incorporation by ion shower and subsequent annealing steps for activation need a temperature as high as 400°C. Therefore, a novel doping and activation technique with a minimal thermal budget must be developed. In addition, since the ion shower technique requires a metal layer to mask out the area not to be doped, a new technique is desired, which can be performed with a standard photo-resist is desired.

Gosain *et al.* attempted to expose the poly-Si films in PH_3 plasma and to drive the dopant atoms into the poly-Si layer by excimer laser annealing [1]. They were successful in obtaining a sheet resistance of only a few hundred Ω /sq. In this method, however, the phosphorus atoms may be left all over the substrate and act as a source of contamination during the subsequent processes. Also, it is difficult to remove the dopant atoms in the unwanted area. Doping area control can be made easier if we use an amorphous silicon layer containing appropriate dopant elements. This technique is more advantageous than the dopant plasma method, especially when p-type and n-type transistors need to be built simultaneously on a single substrate.

It can be easily deduced that, the higher the thickness of the dopant layer and the energy of the laser beam, the lower the sheet resistance of the resulting film. However, there also exists an increased chance of explosive evolution of hydrogen in the dopant layer and of non-recoverable damage to the poly-Si film when the dopant layer is thick. So far there is little information on the optimum thickness and laser energy for the dopant layer to achieve sufficiently low sheet resistance.

In this paper, low-temperature deposition parameters of the dopant-rich amorphous silicon are examined. Influence of both the thickness of the dopant layer and the laser energy to the sheet resistance has also been studied.

2. Experimental Procedure

The experimental procedure is illustrated in Figure 1. A 500Å-thick undoped polycrystalline silicon (poly-Si) film was prepared using the standard excimer laser annealing on a Corning 1737® glass substrate. An amorphous silicon layer containing dopant impurities of phosphorus was deposited using the standard PECVD (plasma-enhanced chemical vapor deposition) technique. The dopant layer thickness was varied between 50 Å and 100 Å

The dopant layer was subsequently annealed to activate the dopant atoms. Variation of the sheet resistance of the resulting n-type poly-Si was studied as a function of the annealing energy.

3. Results

The deposition conditions of the a-Si:H dopant layers are summarized in Table I. Dopant layers

* In this study, all the experiments were carried out on glass substrates only, and the possibility of application to the plastic substrates was discussed.

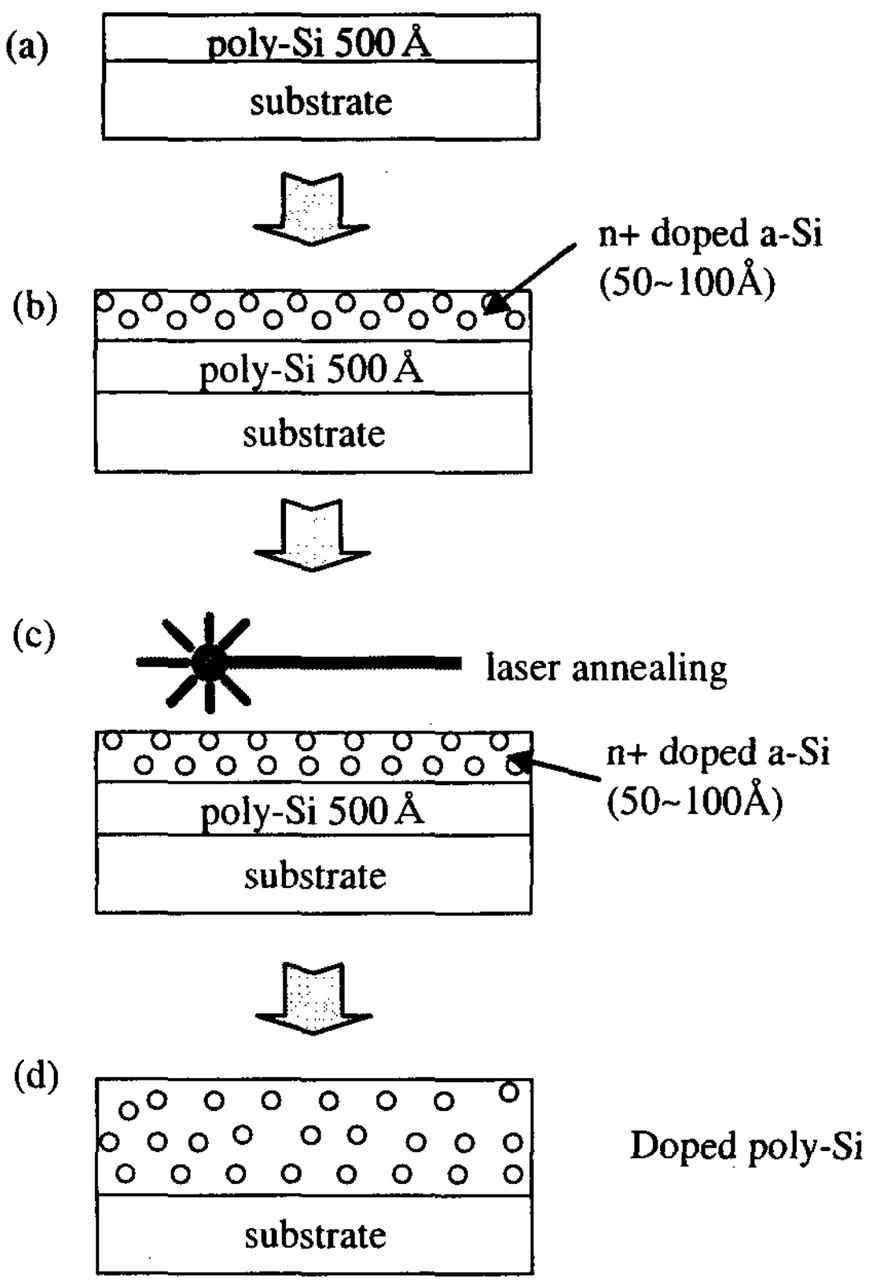

Figure 1. Schematic of the experimental procedure

were successfully deposited at the substrate temperature of 120°C, showing no evidence of columnar growth and of poor adhesion. Gas mixtures of SiH_4 + He and PH_3 + He were used to ensure good film quality for the low-temperature deposition. Helium is believed to be effective in preventing columnar growth and hence densifying the film, as it etches out the weakly-bonded radicals and transfers thermal energy to the mobile radicals on the growing surface [2]. Sample #5 was used for depositing dopant layers in this study.

According to Stutzmann's early work [3], if we neglect the influence of plasma power and temperature, the density of the dopant atoms incorporated in the film can be approximated as follows:

$$N_{solid} \approx (N_{gas})^{0.8} = \left(\frac{[PH_3]}{[SiH_4]+[PH_3]} \right)^{0.8} = 14.7\%$$

If we take 5.0 x 10^{22} cm^{-3} as the atomic density of silicon, the doping density per unit area of the 50 Å-thick layer corresponds to:

$$(5.0\times10^{22})(14.7)(50\times10^{-8}) = 3.7\times10^{17}\,\text{atoms/cm}^2$$

Therefore, with only 50 Å of a dopant layer we can have a sufficient number of dopant atoms available, comparable to that of the ion shower technique.

Figure 2 shows the variation of surface resistivity with the laser energy for samples having the 50Å-thick dopant layer. It is seen that the sheet resistance decreases monotonically with the increase in laser energy. Sheet resistance values lower than 10^{-4} Ω/sq. were obtained at the laser energy density of 390mJ/cm^2. These values are considered to be sufficiently low for n+ contact in poly-Si TFT's.

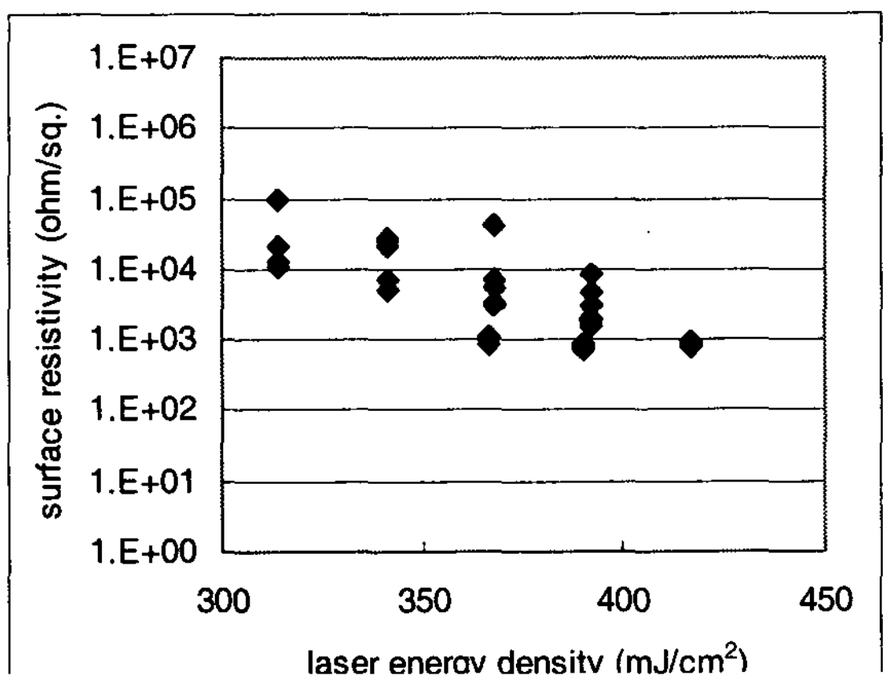

Figure 3 shows the surface resistance for samples having the 100 Å thick dopant layer. A sheet resistance as low as 300 Ω/sq. was obtained at the energy density of 370 mJ/cm^2, but no systematic behavior was found with the variation in the laser energy. Also, most samples were damaged permanently at laser energy densities higher than 400 mJ/cm^2. This result implies that, as the dopant layer becomes thicker, the hydrogen contained in the layer seems to have more adverse effect to the activation of the dopant atoms.

In figures 2 and 3, we can see that the laser energy required to obtain low enough resistivity values

Table I. Deposition parameters for a-Si dopant layers at 120°C

	Gas flow rate (sccm)			RF power (W)	Pressure (torr)	Dep. Rate (Å/sec)
	20%SiH_4/He	H_2	1%PH_3/He			
sample # 1	50	0	20	50	2	6.1
sample # 2	50	50	20	50	2	5.5
sample # 3	50	0	40	50	2	5.5
sample # 4	50	50	40	50	2	5.5
sample # 5	50	0	100	50	2	4.4

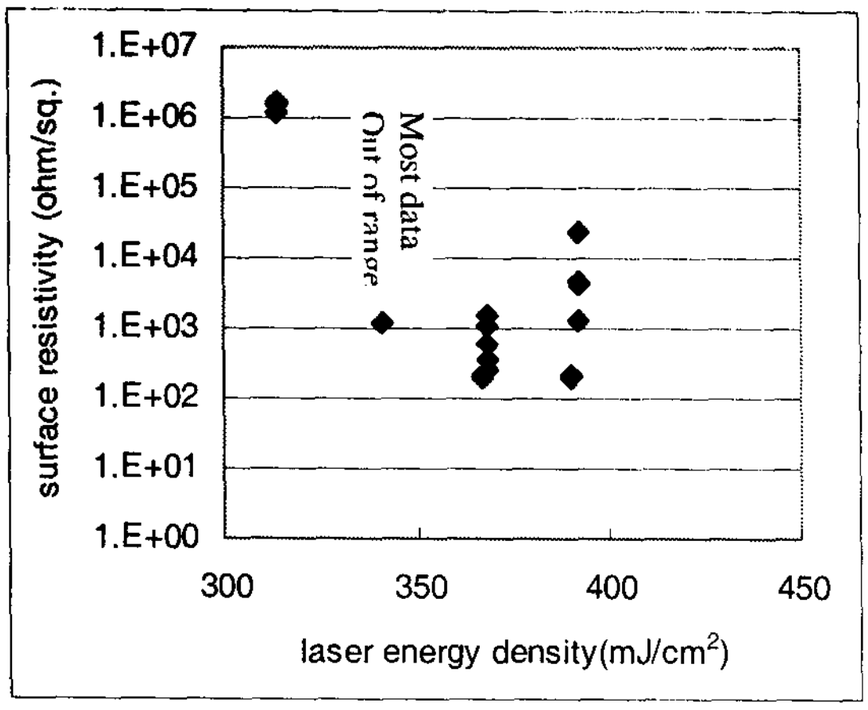

Figure 3. Variation of surface resistivity with laser activation energy for samples having 100Å-thick dopant layer

corresponds to that for melting and recrystallizing the silicon film. This result implies that the laser pulse width might be too short to drive the dopant atoms into the poly Si layer in the solid state, and the silicon must be melted for proper activation. This result also calls for an advanced technique in which crystallization and dopant activation can be achieved in a single pass of laser annealing.

4. Discussion

In addition to the low temperature process capability, one of the biggest advantages of the dopant layer method is the potential of simplifying the TFT fabrication process. We propose several schemes to reduce the number of process steps.

The dopant layer method can be applied to the conventional poly-Si TFT process to carry out laser crystallization and doping at a single step. The process flow is illustrated in Figure 4.

The undoped amorphous silicon (a-Si) precursor layer and a thin, doped a-Si layer are deposited continuously without breaking the vacuum of the PECVD reactor (step a). After proper dehydration, the a-Si layer is patterned using a slit or halftone mask, so that the photo-resist in the undoped channel region is only partially developed (step b). The a-Si layer is then dry-etched to produce the vertical profile as shown in the step c of Figure 4. The consumption of the partially-developed photo-resist delays the etching of the channel layer, and the doped layer can be etched selectively. The photo-resist is stripped out and the a-Si layer is crystallized by the excimer laser (step d). The resulting structure is a pair of highly-doped n+ poly-Si islands with an undoped poly-Si channel layer between them.

Lightly-doped drain (LDD) regions are often desired in poly-Si TFT's to suppress the current leakage due to the hot carriers, although the LDD structure may reduce the on-current as well[4]. We expect that a

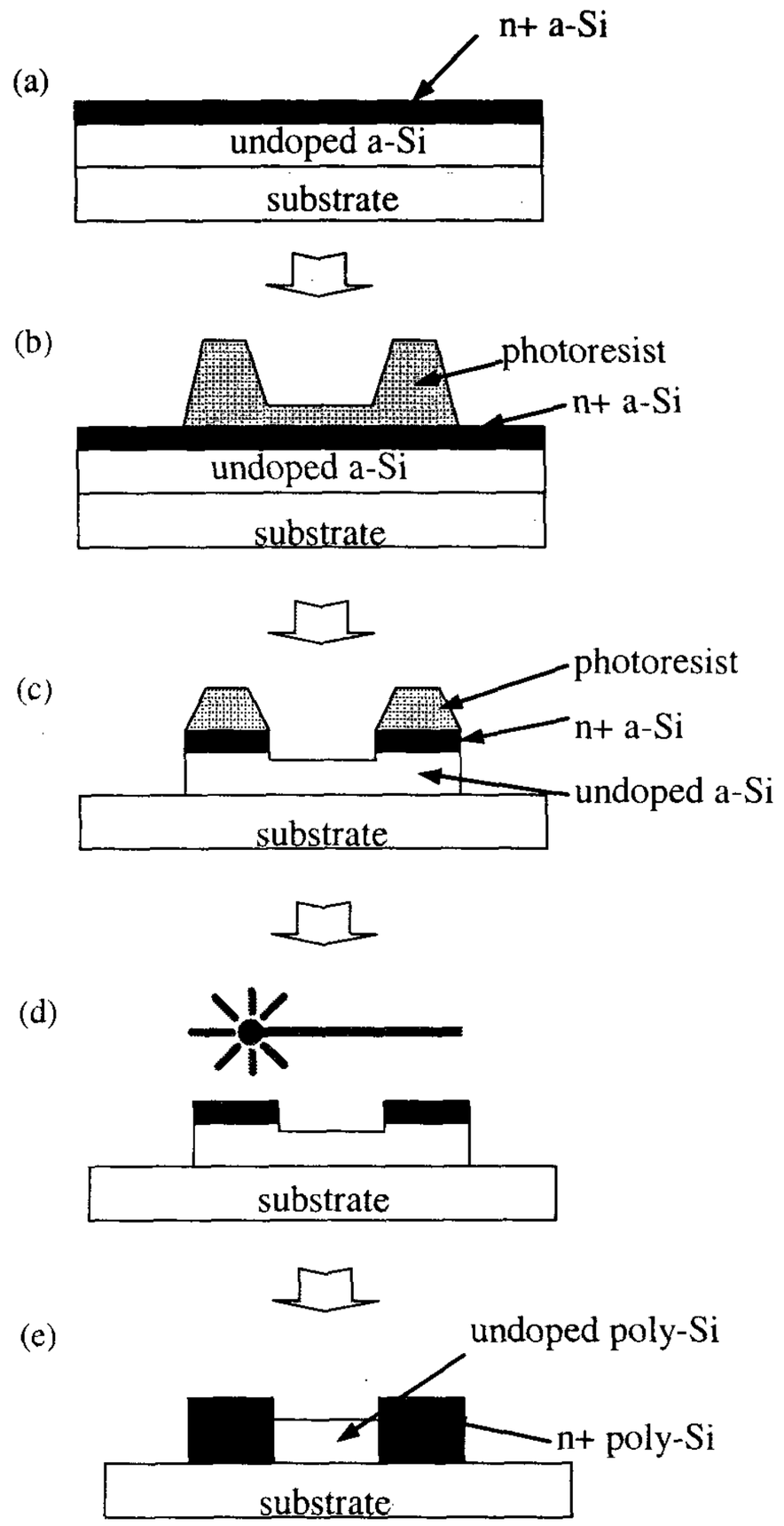

Figure 4. Process flow of the single-step crystallization and doping process: (a) deposition of the double layer of undoped and n+ doped a-Si, (b) second pass of the laser scan with a reduced laser intensity would cause the dopant atoms to diffuse laterally to form a region of a low dopant concentration. However, as the diffusion length would be limited with such a short duration of laser pulses, the dimension of the LDD region formed by lateral diffusion may be insufficient to form an appropriate offset structure with a standard alignment technique.

An alternative way is to form only the LDD and undoped regions during the initial crystallization step, as described in Figure 4. After the entire gate stack is laid down and patterned, the n+ dopant layer is deposited, patterned and annealed as shown in Figure 5. This method would require an additional mask to define the n+ doped contact layer, but the total number of mask will still be less than that of the conventional structure, since the initial LDD formation is carried out simultaneously with the pattering of the channel island.

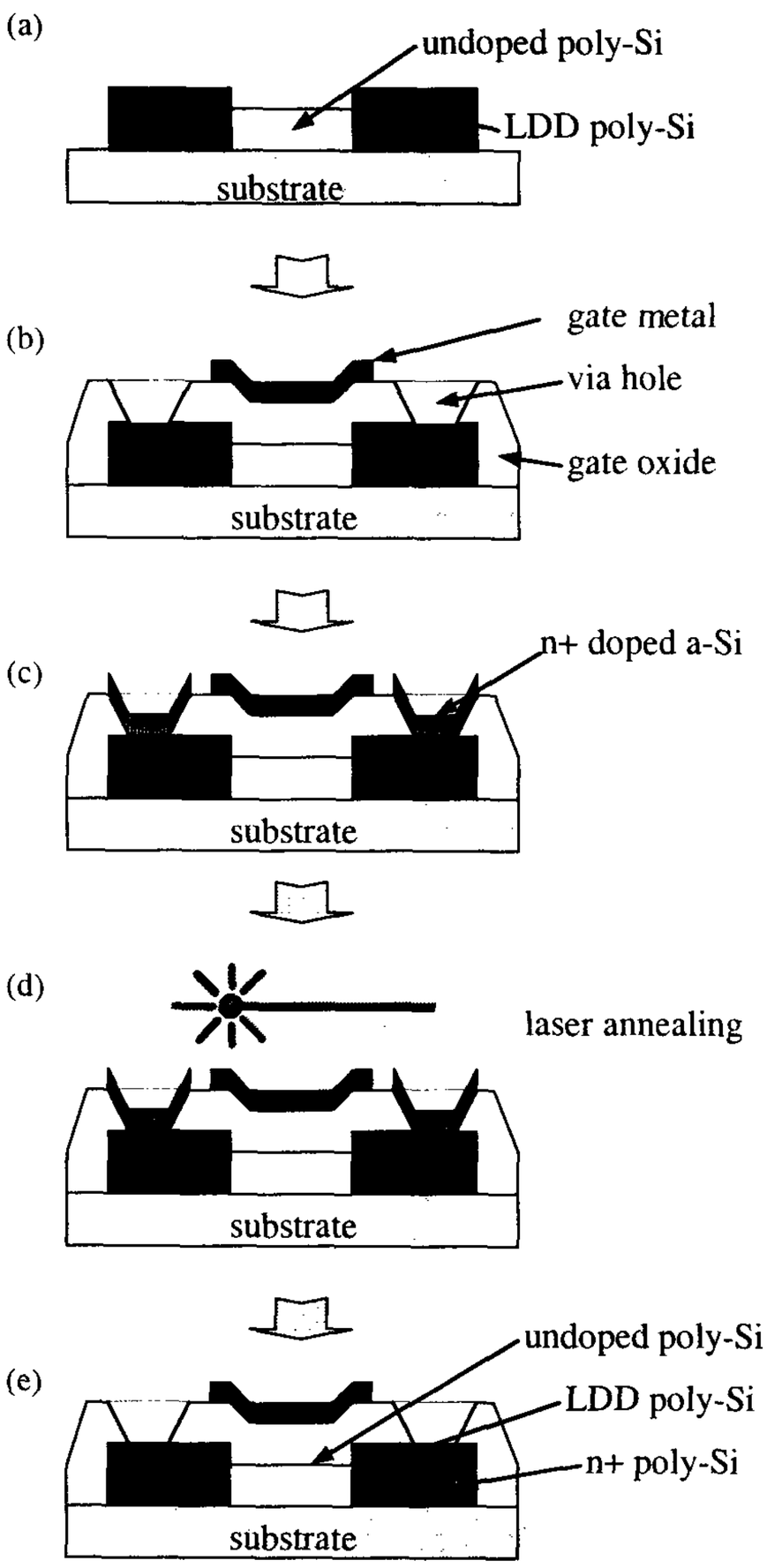

Figure 5. Process flow for LDD formation: (a) crystallization and activation of undoped and LDD layer as described in figure 4, (b) gate stack formation and S-D via hole etch, (c) n+ doped a-Si deposition and patterning, (d) laser annealing for activation, (e) completed LDD/contact structure

We expect that the dopant layer is also advantageous in applications to flexible OLED's. As the importance of the threshold voltage compensation rises in the OLED's, the driving circuitry becomes complicated and often contains both the p- and n-type TFT's. In the conventional ion-shower doping process, the gate metal is used as a masking layer for one type of doping, and an extra metal mask layer is needed for the other type. However, the dopant layer can be patterned with photo-resist only, and dispenses with the deposition and removal of the additional metal layer.

5. Conclusion

A low temperature poly-Si doping process has been studied. Thin layers of amorphous silicon containing phosphorus atoms were successfully deposited on standard poly-Si layers at 120°C. A 50Å-thick dopant layer was calculated to be equivalent to an ion dosage of ~3.7 x 10^{17} cm^{-2}, and a surface resistivity as low as 300 Ω/sq. could be obtained by subsequent laser activation. During the entire process the substrate underwent temperatures no higher than 120°C, and this technique was proven to be applicable to the fabrication of poly-Si TFT's on plastic substrates.

6. Acknowledgement

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7. References

[1] Gosain et al., Jap. J. Appl. Phys. Part2, vol.39 p.L179 (2000)

[2] U.Kroll et al., MRS Symp. Proc., vol.336, p.115 (1994)

[3] Stutzmann, M. et al., Physical Review B, vol.35 11 p.5666 (1987)

[4] Shuichi Rchikoga, Nobuki Ibaraki, Thin Solid Films, vol.383, p.19 (2001)