A New COG Technique Using Solder Bumps for Flat Panel Display

Min-Seok Lee, Un-Byoung Kang and Young-Ho Kim
Div. of Materials Science and Engineering, Hanyang University, Seoul, 133-791, Korea
Tel : 82-2-2290-0405, E-mail : rhsoddl@bcline.com

Abstract

We report a new FCOG (flip chip on glass) technique using solder bumps for display packaging applications. The In and Sn solder bumps of 40 ㎛ pitches were formed on Si and glass substrate. The In and Sn bumps were bonded at 125□ at the pressure of 3 mN/bump. The metallurgical bonding was confirmed using cross-sectional SEM. The contact resistance of the solder joint was 65 mΩ which was much lower than that of the joint made using the conventional ACF bonding technique. We demonstrate that the new COG technique using solder bump to bump direct bonding can be applied to advanced LCDs that lead to require higher quality, better resolution, and lower power consumption.

1. Introduction

Recently, the pitch size and contact area are being decreased in LCD driver IC packaging because of excellent resolution, full color, and small size. The chip on glass (COG) technique is currently being used in a number of products such as high pixel density and small area LCD's. However, the maximum bonding temperature of COG is limited by heat resistance temperatures for the liquid crystal materials and polarizer plate [1]. Therefore, a new reliable and low temperature method should be developed for ultrafine pitch size LCD application. As shown in Fig. 1, many kinds of the conventional COG bonding techniques have been developed: Au bump bonding using anisotropic conductive adhesive (ACA) or anisotropic conductive film (ACF), and bump bonding using isotropic conductive adhesive [2-4].

The COG technique using anisotropic conductive film (ACF) has been only applied because it had some advantages such as low bonding temperature, simple process, and improved environmental compatibility. However, the COG technique using ACF bonding may be limited because the electrical short or open will increase as the resolution of LCD become higher.

We introduce a new COG technique using the solder bump-to-solder bump bonding at the temperature below 150□. In this technique, the different solder bumps were formed on the chip and the glass substrate respectively and metallurgically bonded below the melting temperature of two solder bumps. Using the In/Sn solder system, the test chip and the glass substrate with 40 ㎛ pitch bumps were connected at 125□ which is lower than the melting temperature of either In(157□) or Sn(232□).

This paper describes the bump formation method, the results of experimental bonding and electrical properties.

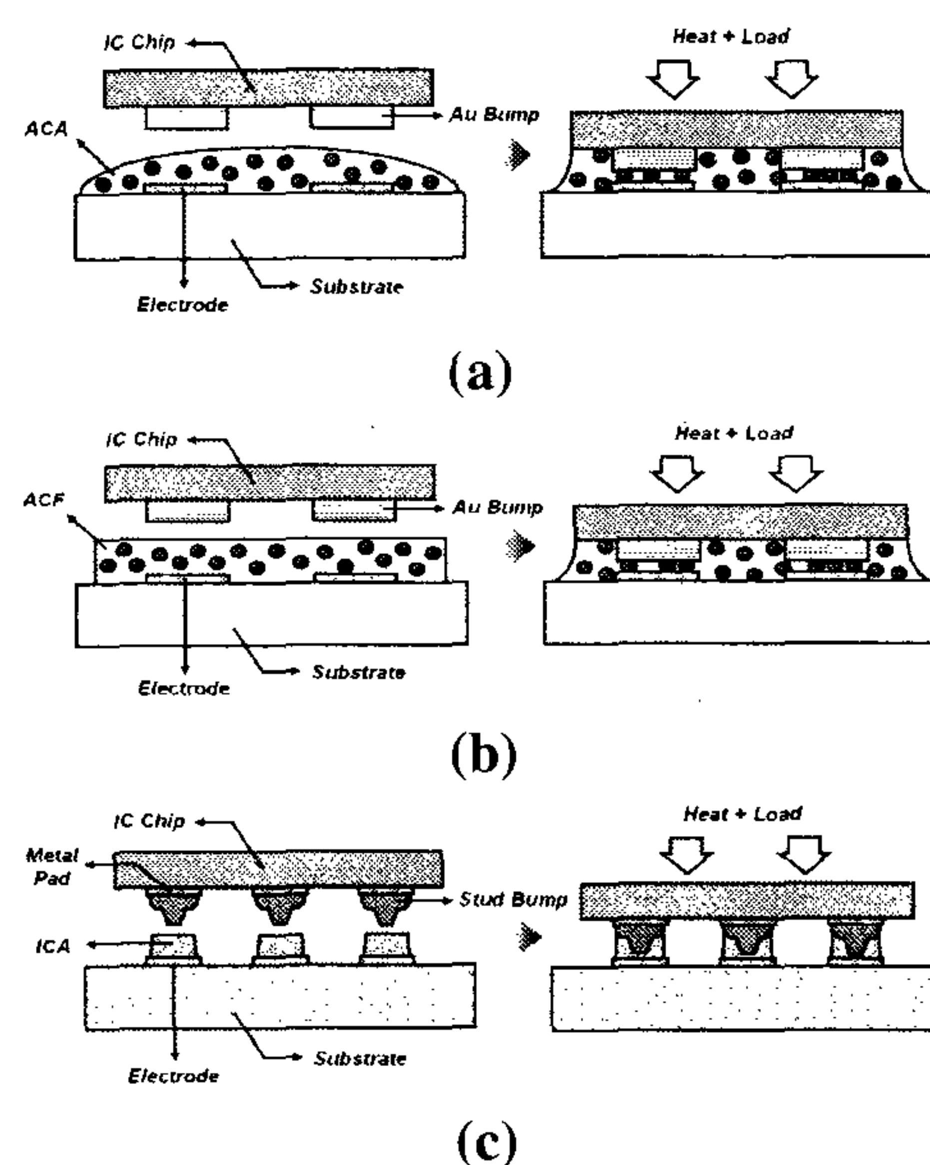

Figure 1. Various COG technologies using (a) ACA, (b) ACF, and (c) ICA

2. Experimental procedure

To investigate the possibility of this method, In and Sn solder of 10 ㎛ was respectively deposited on metal layer without patterning. The In and Sn solder layer were joined using hot plate at 120□ for 1min.

The procedure for fabricating the solder joints with

40 μm pitch is shown in Fig. 2. Au/Cu/Ti thin film was deposited for metal pads using DC magnetron sputtering on Si wafer. The rectangular shaped metal pads of 40 μm pitch were fabricated through the photolithographic process and the wet chemical etching. For electrical test, a metallization which consists of metal pads and conductor of the daisy chain was needed. Ti(0.1 μm)/Au(0.03 μm)/Cu(2 μm)/Ti(0.05 μm) metal layer was deposited for conductor of the daisy chains on SiO_2/Si wafer. The metal pads were fabricated with opening via of Ti through the photolithographic process and the wet chemical etching.

The solder bumps were formed on the metal pads using evaporation method and lifted off process. The thick PR(AZ^R P9260) was used as lift-off mask. In order to keep the good electrical properties, the rectangular solder bumps were formed on the substrate. The dimension of the solder bumps was 25 μm × 50 μm. The In and Sn solder bumps were formed on the test chip and the glass substrate, respectively. Flux was coated on the surface of each bump and then the solder bumps on the chip were aligned to the corresponding solder bumps of glass substrate using flip chip bonder and all solder bumps were jointed simultaneously at 125℃ for 1 min.

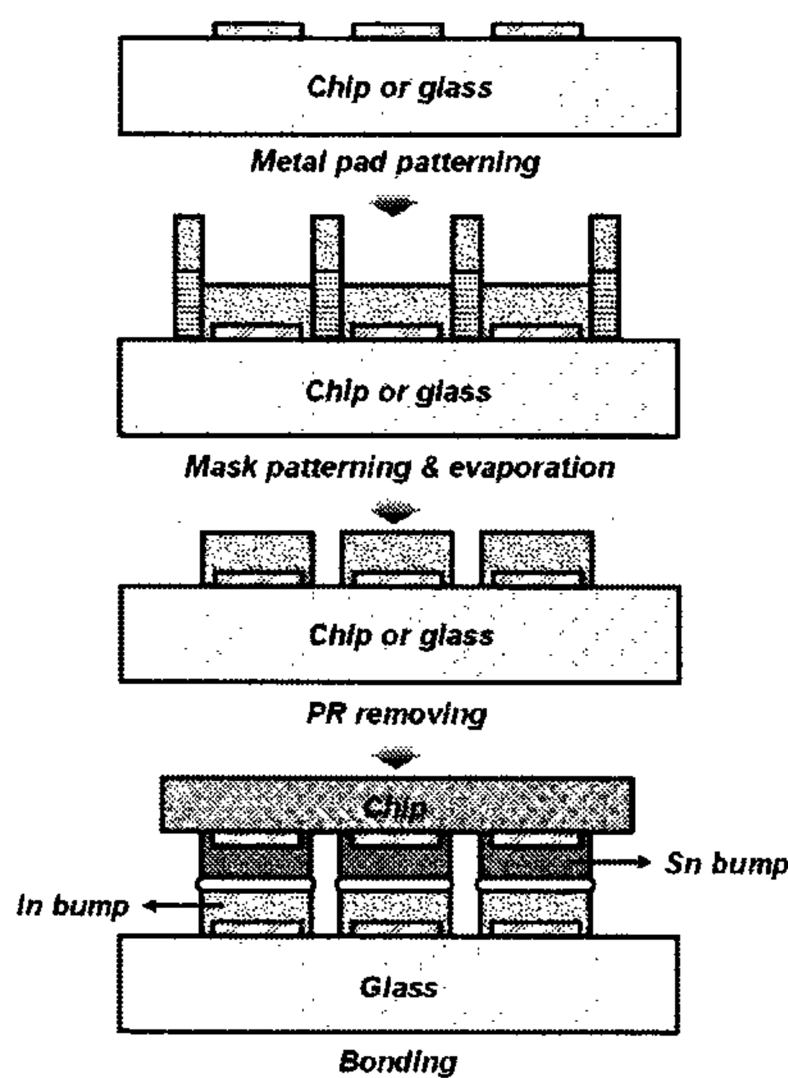

Figure 2. Schematic view of solder joint formation

The load of 2 N per chip was applied during the bonding. Since the test chip and glass substrate had 676 bumps respectively, the load per bump was 3 mN. The contact resistance of the solder joints with daisy chain was measured using four-point probe method.

3. Results and discussion

Figure 3 is the SEM image showing the cross-section of In/Sn solder joint bonded at 120℃ for 1 min. This joint was used without patterning in order to investigate the bondability between In and Sn solder bump at 120℃. The formation mechanism of joint between In and Sn bumps is as follows. When the In and Sn solder are in contact together, the interdiffusion occurs between two solders. As shown in Fig. 4, the melting temperature of In-Sn alloy decreases from that of each solder due to intermixing. Therefore, the In-Sn solder joint may be melted partially and bonded lower the melting temperature of either In(157℃) or Sn(232℃). Actually, it was observed that the joint was successfully made at 120℃.

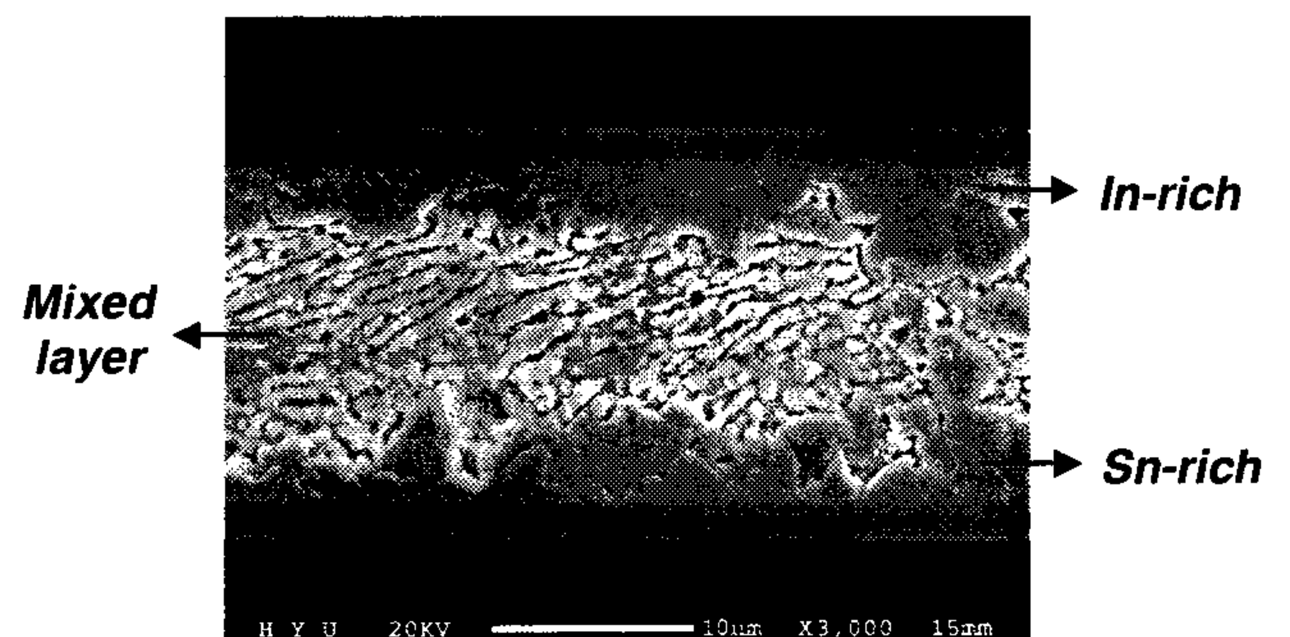

Figure 3. Cross-sectional SEM image of In/Sn solder joint

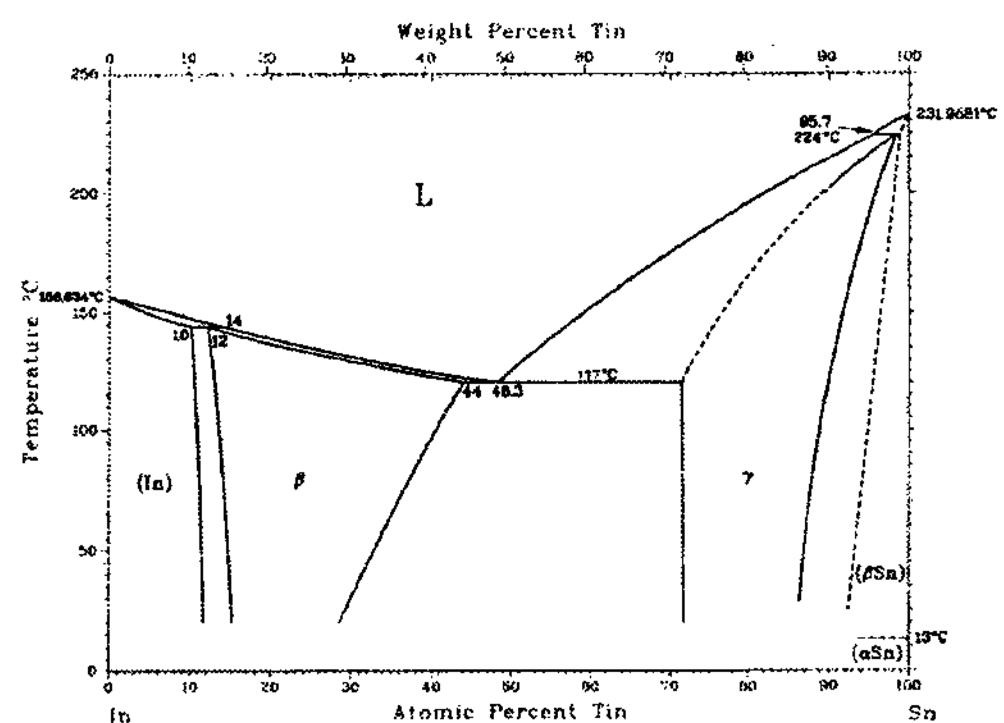

Figure 4. In-Sn phase diagram

Figure 5 is the SEM images showing the metal pads and the In bumps with rectangular shape formed on the metal pads of 40 μm pitch uniformly. The metal pads were designed as 20 μm × 45 μm rectangle to fix solder bumps firmly. The solder bumps were successfully fabricated using evaporation method and

lifted off process and the average height of the solder bumps was 10 ㎛.

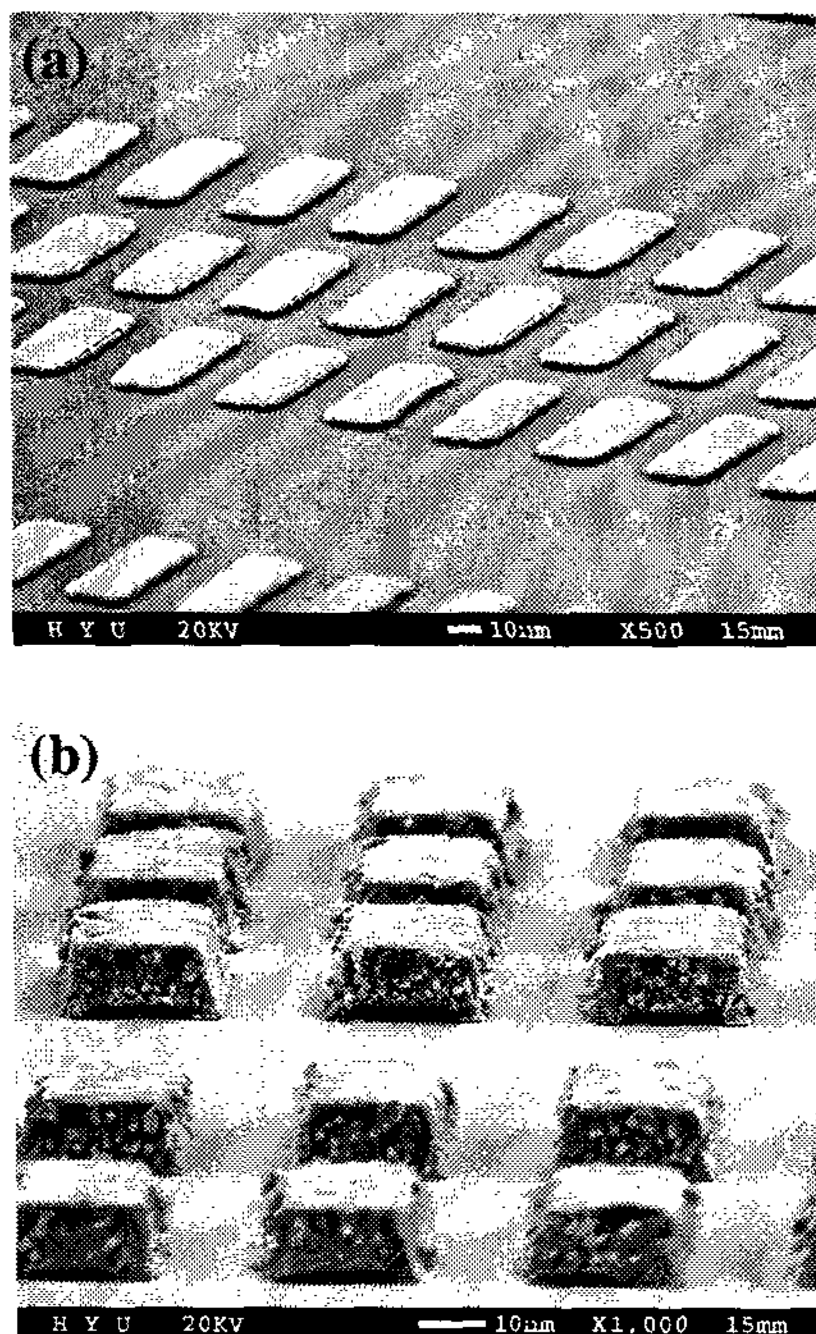

Figure 5. SEM images showing (a) the metal pads and (b) the In solder bumps

Figure 6 is the SEM image of the cross-sectional In/Sn solder joint. This image shows the jointed solder bumps with 40 ㎛ pitch. The solder joints were connected through the metallization between Si and glass substrate. The In/Sn solder bumps were successfully connected under the bonding pressure as low as 3 mN per bump which is much lower than that of COG technique using ACF. Using this technique, the solder joints which have 40 ㎛ pitch was fabricated satisfactorily and the much finer pitch application is likely to be applied.

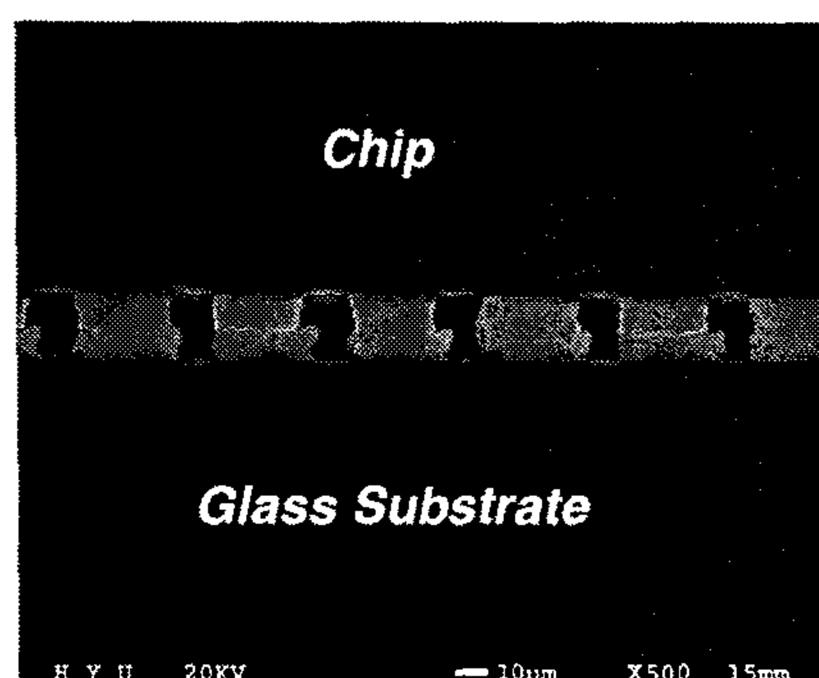

Figure 6. Cross-sectional SEM image of 40 ㎛ pitch In/Sn solder joint

The electrical assessment is done using four-point technique to address the electrical resistance of the daisy chain running through the chip and the glass substrate. Table 1 shows the contact resistance of solder joints. The average of contact resistance per solder joint was 65 mΩ/bump with 204 bumps. This value is lower than that of conventional ACF bonding technique which has hundreds milliohm per bump [5-6].

Table 1. Contact resistance of the joints of In/Sn solder bump

	R_b(mΩ)	Standard deviation(mΩ)
Average	65	17

Based on the results, this COG technique using the metallurgical bonding of the solder bump is applicable to mounting IC for ultrafine pitch applications at low temperature and the low pressure. This technique has the several advantages as compared with the COG technique using ACF in the field of ultrafine pitch LCD driver IC packaging; ultrafine pitch capability, low contact resistance, low bonding pressure, and low material cost.

4. Conclusion

Using the In/Sn solder materials, we developed a new COG technique below melting temperature of solder materials. The solder joint of minimum 40 ㎛ pitch was successfully formed through the metallurgical bonding between In and Sn solder bumps. The average contact resistance per solder joint having a minimum 40 ㎛ pitch was 65 mΩ.

Acknowledgement

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