Thin Film Morphology Pentacene Thin Film Using Low-Pressure Gas Assisted Organic Vapor Deposition(LP-GAOVD)

Seong Deok Ahn , Seung Youl Kang , Yong Eui Lee ,
Chul Am Kim , Meyong Ju Joung and and Kyung Soo Suh
Basic Research Lab. &
ETRI, 161 Gajeong-dong, Yuseong-gu, Daejeon 305-350, Korea
Phone : +82-42-860-1581 , E-mail : lovesky@etri.re.kr

Abstract

We have investigated thin film morphology of pentacene thin films by the process of low-pressure gas assisted organic vapor deposition (LP-GAOVD). Source temperature, inert gas flow rate, substrate temperature and deposition pressure during film deposition is used to vary the growth rate, thin film morphology and the crystalline grain size of pentacene thin films. The electrical properties of pentacene thin films for applications in organic thin film transistor and electrophoretic displays will be discussed.

1. Introduction

In recent years, thin film transistor (TFTs) based on organic materials as active layer have received considerable interest. Organic TFTs offer advantages compared to traditional field-effect transistors, like mechanical flexibility and weight reduction[1-4].

Pentacene, a polyacene, consists of five linear benzene rings and has demonstrated the highest electron and hole mobility of organic small molecules. The material exhibits a strong tendency to form highly ordered films which depend on the growth conditions and the substrate. Pentacene thin film have been fabricated by solution precipitation,[5] organic molecular beam deposition,[6] vacuum thermal evaporation,[7] organic vapor phase deposition,[8] all having compared performance.

In this work, we have grown the pentacene thin film with new deposition technique such as low-pressure gas assisted organic vapor deposition (LP-GAOVD). LP-GAOVD proceeds by evaporation of the molecular source material into a stream of cold inert carrier gas that transports the vapors toward a substrate where condensation of the organic occurs. We characterized the pentacene thin films by means of XRD, AFM , FTIR, and SEM images spectra as a function of the working pressure during the evaporation process.

2. Experimental

As received pentacene, obtained from TCI, is used without additional purification. Si-wafers, thermally oxidized in a dry atmosphere (SiO_2 thickness about 500 nm) are used as a substrate. Nitrogen carrier gas at flow rates ranged from 25 to 130 sccm, while the source material was maintained at 300 °C during pentacene thin film deposition. The pressure in the deposition chamber was varied from 0.1 to 10 Torr, and substrate temperature was maintained at 100 °C. The temperature is measured by chromel-alumel thermocouples.

All transistor was fabricated on Si-wafers using the device structure shown in Fig. 1. WSi and low temperature silicon oxide were used for the gate electrodes and gate dielectric layer, respectively. Gold was used for the source and drain contacts, since its large work function leads to improved carrier injection into the organic material.

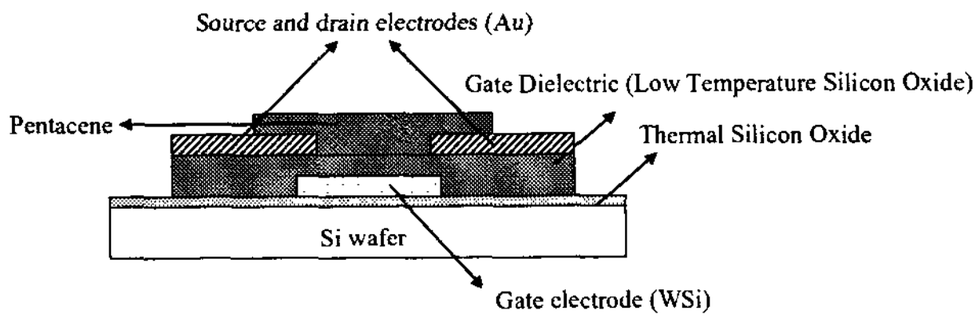

Figure 1. Schematic structure of a pentacene thin film transistor on Si wafer.

3. Results and discussion

Figure 1 shows the morphology of a pentacene thin film on thermal oxide at various deposition pressures. The deposition time was 1 hours. Above 5 Torr, the pentacene thin film is not formed the continuous thin film and below 1 Torr, the pentacene thin film is formed the continuous thin film. We find that the pentacene grain size increase at low deposition

pressures.

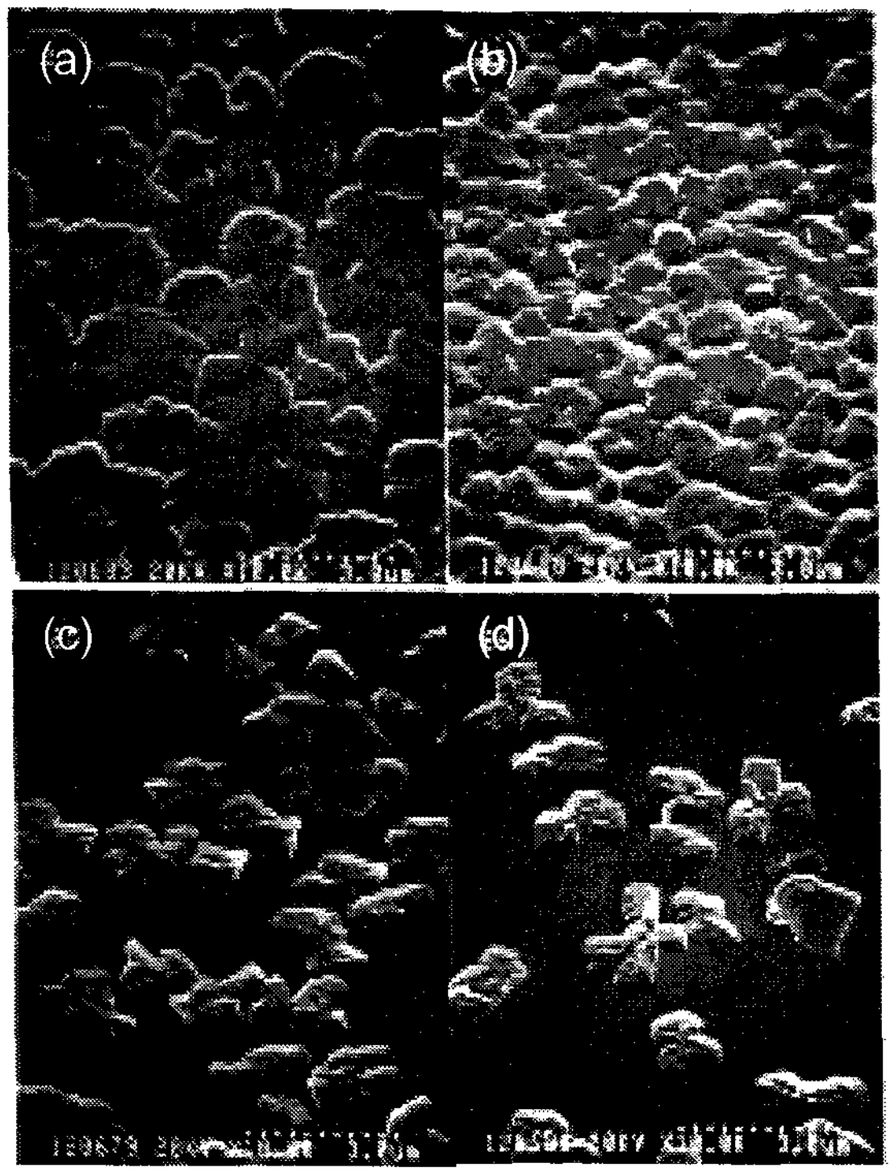

Figure 2. Scanning electron micrographs of pentacene thin films deposited by LP-GAOVD onto thermal oxide at (a) 0.1 Torr, (b) 1 Torr, (c) 5 Torr, and (d) 10 Torr.

Figure 3 shows the XRD pattern of a pentacene thin film on thermal oxide at various deposition pressures. The peaks arise from the well-known bulk and thin film phases of pentacene. The thin film phase has an interplanar spacing of 15.4 Å, while the bulk-phase has an interplanar spacing of 14.5 Å. At 0.1 Torr, the pentacene thin film consists mainly of thin film phase. However, the increase of deposition pressure leads to an increase of the bulk phase. Thus, the composition of the film changes form the thin film to the crystalline bulk phase.

The pentacene used in the present devices behaved as a p-type semiconductor. A typical plot of drain current, I_D, vs drain voltage, V_D at various gate voltages, V_G, is shown in figure 4. The pressure in the deposition chamber and substrate temperature were 0.3 Torr and 100 °C, respectively. When the gate electrode is biased negatively with respect to the source electrode (grounded), pentacene TFTs operate in the accumulation mode and the accumulated charges are holes. For the plots on figure 4, the mobility μ and the threshold voltage V_T were calculated to be 0.003 $cm^2V^{-1}s^{-1}$ and 0.47 V, respectively.

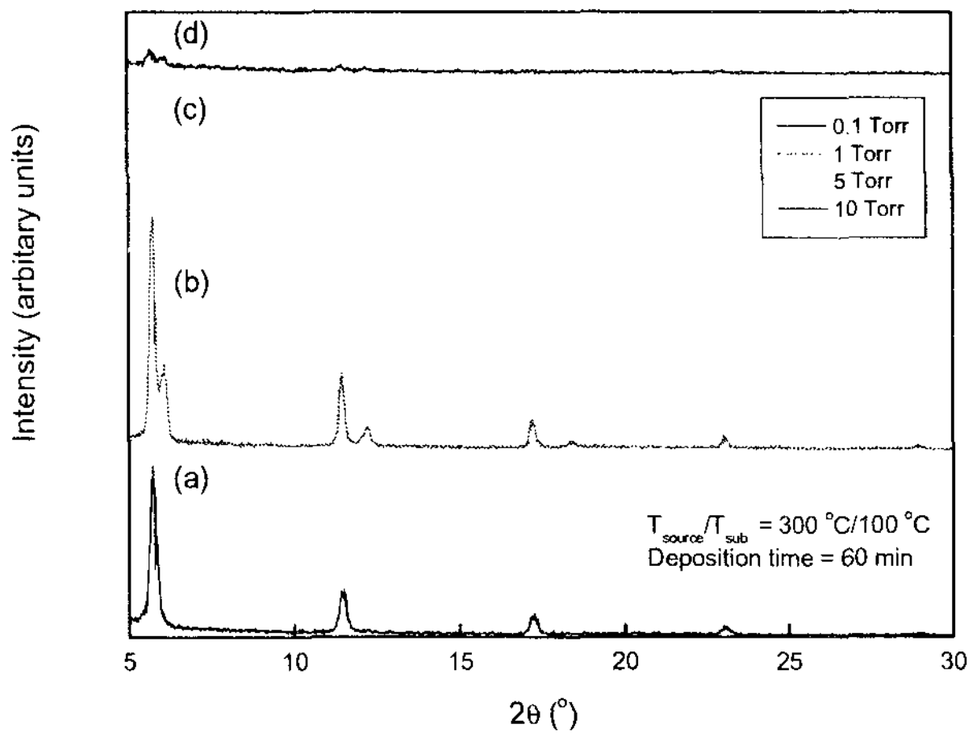

Figure 3. X-ray diffraction pattern of pentacene thin films deposited by LP-GAOVD onto thermal oxide at (a) 0.1 Torr, (b) 1 Torr, (c) 5 Torr, and (d) 10 Torr.

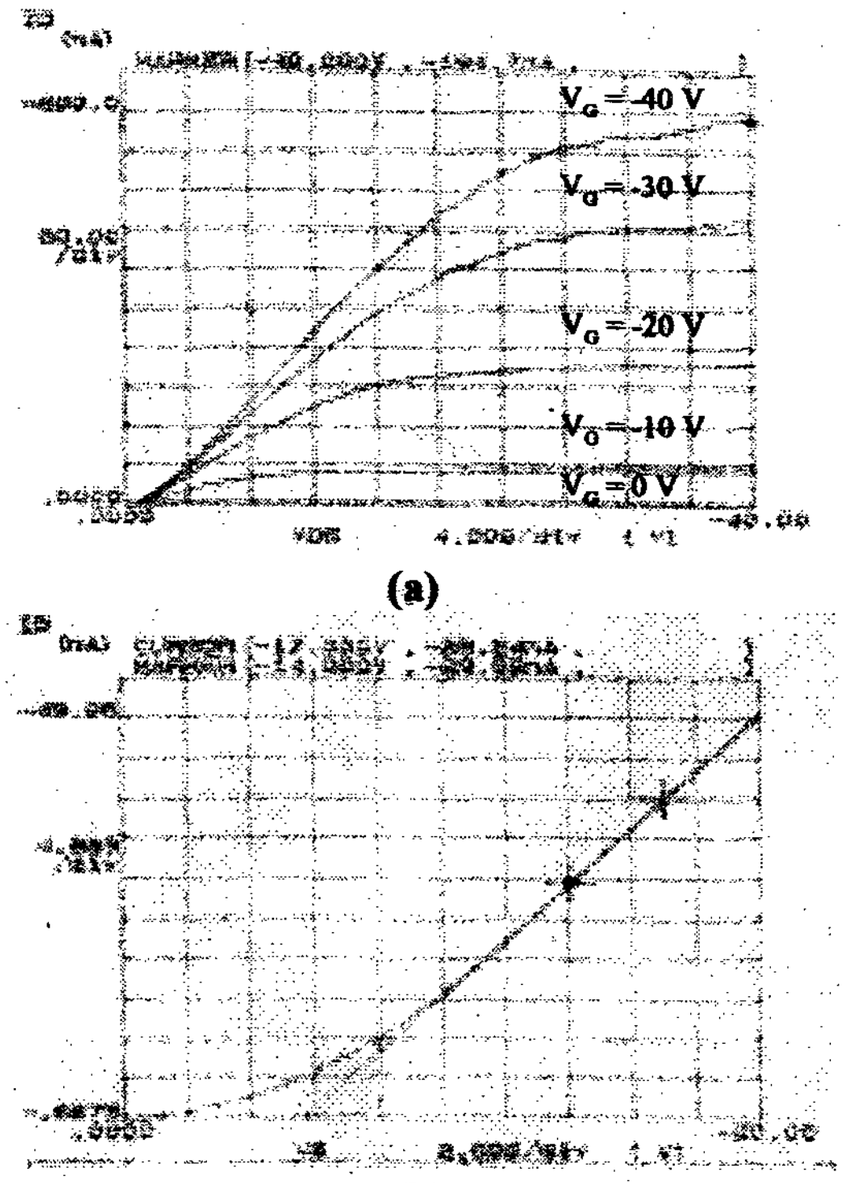

Figure 4. Plot of (a) drain current vs drain voltage at various gate voltage value and (b) drain current vs gate voltage at a constant drain voltage of -10 V (linear region).

4. Conclusion

In this study, we have grown the pentacene thin film with new deposition technique such as LP-GAOVD. Deposition of pentacene thin film using LP-GAOVD process is promising deposition technique. Using this method, the pentacene thin film of the super flat surface is obtained and the mobility and the threshold voltage were 0.003 $cm^2V^{-1}s^{-1}$ and 0.47 V, respectively.

5. Acknowledgements

The authors thank Unitex Co., Ltd for supporting the deposition apparatus and helpful technical assistance. The Korea Ministry of Information and Communications financially supported this work.

6. References

[1] Y.Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, IEEE Trans. Elec. Dev. **44**, 8 (1997).

[2] A. R. Brown, A. Pomp, C. M. Hart, and D. M. de Leeuw, Science, **270**, 972 (1995).

[3] C. D. Dimitrakopoulos, S. Purushotaman, J. Kymissis, A. Callegari, and J. M. Shaw, Science, **283**, 822 (1999).

[4] 3. A. Dodabalapur, J. Laquindanum, H. E. Katz, and Z. Bao, Appl. Phys. Lett. **69**, 4227 (1996).

[5] A. R. Brown, C. P. Jarrett, D. M. de Leeuw, and M. Matters, Synth. Met. **88**, 37 (1997).

[6] C. D. Dimitrakopoulos, A. R. Brown, and A. Pomp, J. Appl. Phys. **80**, 2501 (1996).

[7] D. J. Gundlach, Y. Y. Lin, T. N. Jackson, S. F. Nelson, and D. G. Schlom, IEEE Elec. Dev. Lett. **18**, 87 (1997).

[8] M. Shtein, H. F. Gossenberger, J. B. Benziger, and S. R. Forrest, J. Appl. Phys. **89**, 1470 (2001).