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Influence of wall charge configurations prior to addressing discharge on dynamic margin in AC Plasma Display Panel

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ABSTRACT

We have experimentally investigated the influence of wall charge configurations prior to addressing discharge on dynamic margin in AC plasma display panel. In this experiment, we have analyzed the quantity and polarity of wall charge accumulated on the front and rear dielectrics just prior to the addressing discharge under the conventional driving sequence.

Introduction

The dynamic margin for selective writing discharge occurred at addressing period is one of major factors to determine the display quality and lifetime of device. And we cannot also expect the stable discharge in sustaining period without wide dynamic margin. This dynamic margin has been determined by wall charge configuration, which is formed already prior to the addressing period under a given driving sequence and panel structure. Thus well-adjusted wall charge configuration prior to the addressing period is very important to obtain the wide operation margin and excellent display quality. In this experiment, we have analyzed the quantity and polarity of wall charge accumulated on the front and rear dielectrics prior to the addressing discharge under the well-known driving sequence[1] as shown in Fig. 1. And we have also investigated the relationship between the wall charge configuration and the dynamic margin ranges for full white pattern with 7" test panel.

Experiments and Results

Generally, since the wall charge configuration prior to the addressing discharge is dominantly affected by high voltage reset pulse[2]. For adjusting the wall charge configuration, we have applied the WCAP (Wall Charge Adjusting Pulse) on addressing electrode (Z) as shown in Fig. 1. The WCAP adjusts the discharge strength between sustaining electrode (X) and addressing electrode (Z). And this discharge gives influences on discharge of front electrodes (X and Y). Thus, we can adjust the wall charge configuration with WCAP.

Shown in Fig. 2 is the IR emission emitted from test panel by high voltage reset pulse. Of these two discharges, the former is the bulk write discharge and the latter is the bulk erase by self-erasing method[1-2]. Fig. 3 shows the discharge currents flowed into sustaining electrode (X) as the WCAP varies, when the bulk writing discharge is occurred by high voltage reset pulse, which is applied to X with positive polarity. At the WCAP of 0 V, the discharge response time is very fast for the discharge occurred between X

and Z because of short discharge path relative to X and Y, and also, the discharge of XY is occurred but lately. Thus the positive wall charges are accumulated on the Y and Z electrode. And at the same time, the negative wall charge is strongly formed on X electrode. As the WCAP is increased, the main discharge is occurred with X and Y electrode and the positive wall charges on rear dielectrics with Z electrode are gradually reduced. When the WCAP is 140 V, the discharge currents is about the same as that with floating Z-electrode. Fig 4 shows the discharge currents flowed into X and Z electrodes when the WCAP is 140 V. It is noted that the discharge between front electrodes (X or Y) and Z is not almost occurred, hence the wall charge is little accumulated on the rear dielectrics. At the WCAP much higher than 140 V, the discharges of XY and of YZ are occurred, and the negative wall charges are again formed on the rear dielectrics.

Shown in Fig. 5 is the firing voltage of detecting pulse after self-erasing discharge by high voltage reset pulse versus various WCAP on addressing electrode. The firing voltages of the positive detecting pulse applied on X are always higher than that of positive pulse applied on Y. Therefore, a very small amount of negative wall charge always remains at the X electrode after self-erasing discharge. At the WCAP of 0 V, since the discharge path is obviously divided into XZ and XY[3] relative to that with other WCAP, the wall charges remain much more at the X electrode after self-erase. But in fact, because the quantities of residual wall charge between X and Y electrodes are very small, the firing voltage is dominantly affected by wall charges on rear dielectrics. Therefore, by controlling the wall charges on rear dielectrics we are able to make the firing voltages of detecting pulse applied on X and Y have a same value. Fig. 6 shows the voltages of control pulse applied on Z electrode at the same time with detecting pulse in order to have a same detecting voltage as the WCAP on addressing electrode changes. As we expected, at the WCAP of 140 V, because the wall charge on rear dielectrics is little existing, the voltage of control pulse is only 5 V, whereas, at the WCAP of 0 V with more positive wall charge relatively, the voltage of control pulse is about 30 V.

Fig. 7 shows a panel dynamic margin for full white pattern with driving sequence in Fig. 1 under addressing voltage of 80 V and 90 V, respectively. The range of margin with WCAP of 0 V has been measured to be below 15 V at each addressing voltage, while to be above 30 V for WCAP larger than 70 V. Therefore, as the residual wall charge on front and rear dielectrics increases, the dynamic margin decreases gradually, especially for wall charges between Y and Z of the same positive polarity.

Conclusions

In this experiment, we have analyzed the quantity and polarity of wall charge accumulated on the front and rear dielectrics prior to the addressing discharge under the well-known driving sequences. And we have also investigated the relationship between wall charge configuration and the dynamic margin ranges for full white pattern with 7" test panel. As a result, under a certain wall charge configuration on front and rear dielectrics, especially for the wall charge of same polarity between scan and addressing electrode, the dynamic margin for selective writing discharge occurred at addressing period has been seriously reduced. And it is also found that the wall charge on the rear dielectrics is one of main factors causing the wrong discharge in sustaining period.

Acknowledgements

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References

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[2] Jae-Jun Ko, Young-Guon Kim, etc. "Transition of Space Charge to Wall Charge by Control Pulse after Self-Discharge in AC-Plasma Display Panel", Jpn. J. Appl. Phys. 39(2000), pp. 2825-2828.

[3] Y. Jung, C. G. Ryu, etc. "Influence of Data Voltage on Sustaining Discharge and Luminance Efficiency in AC Plasma Display Panels", 2002 IEEE ICOPS, 5P22.

Figures

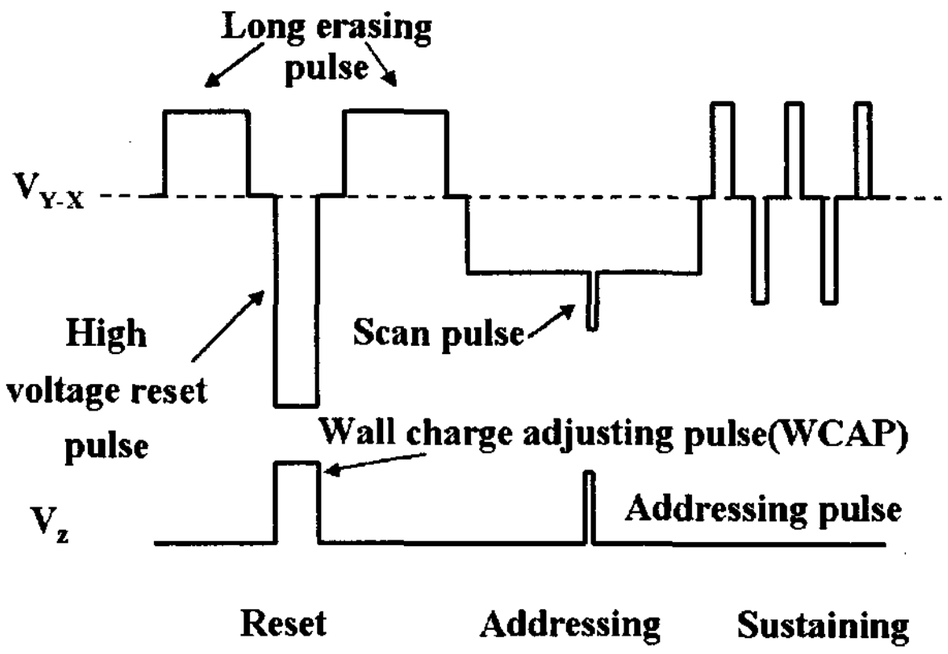

Fig. 1. Driving sequences.

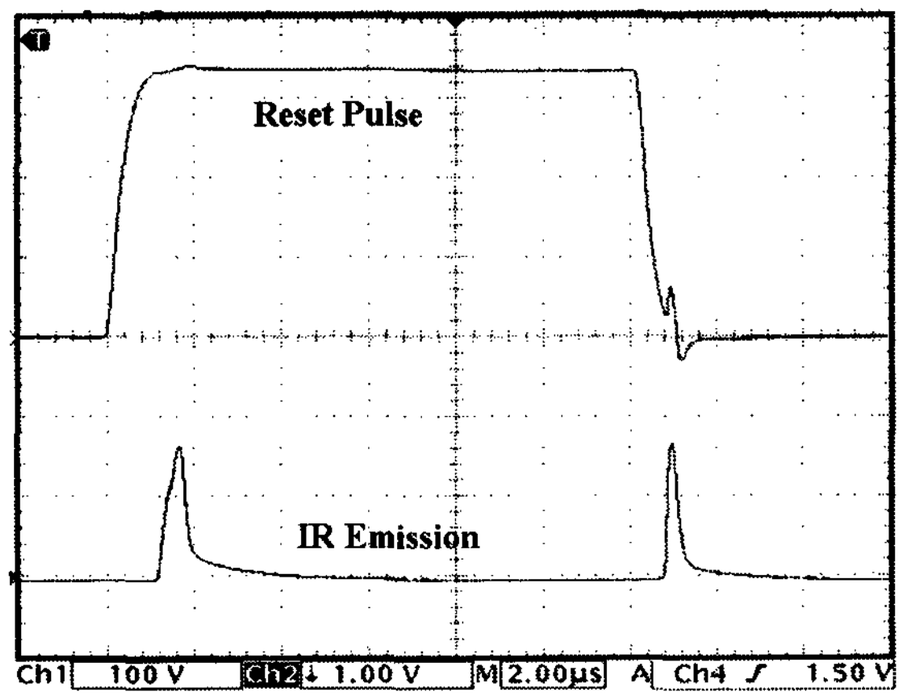

Fig. 2 Reset pulse and IR emission

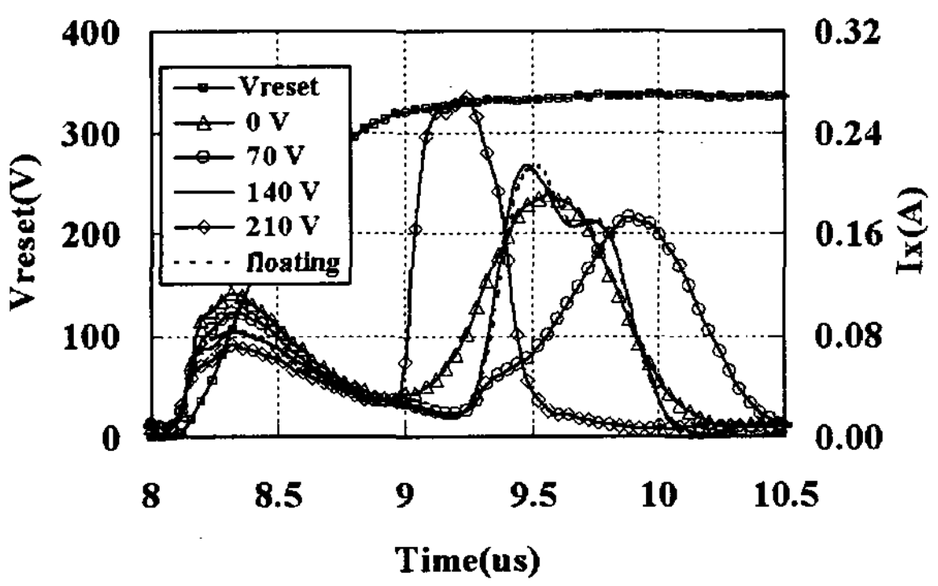

Fig. 3 Discharge currents flowed by bulk write

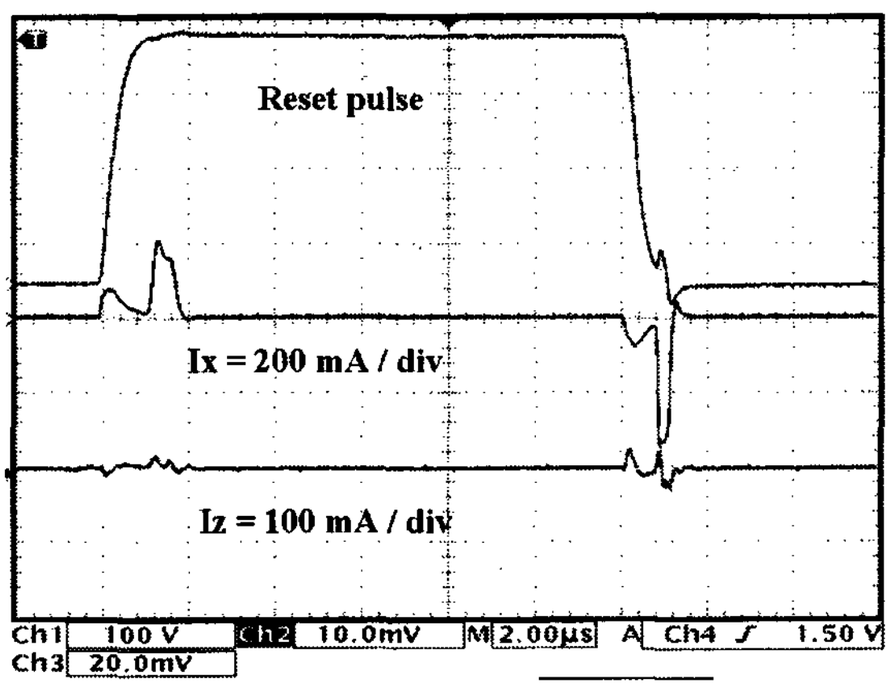

Fig. 4 Discharge Current at WCAP of 140 V.

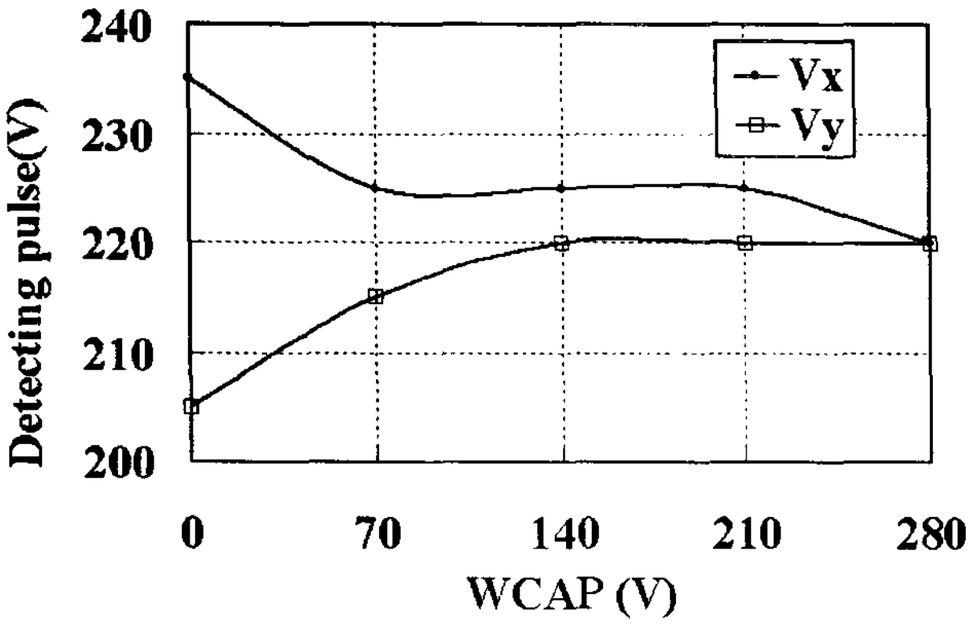

Fig. 5 Firing voltage after self-erase versus WCAP.

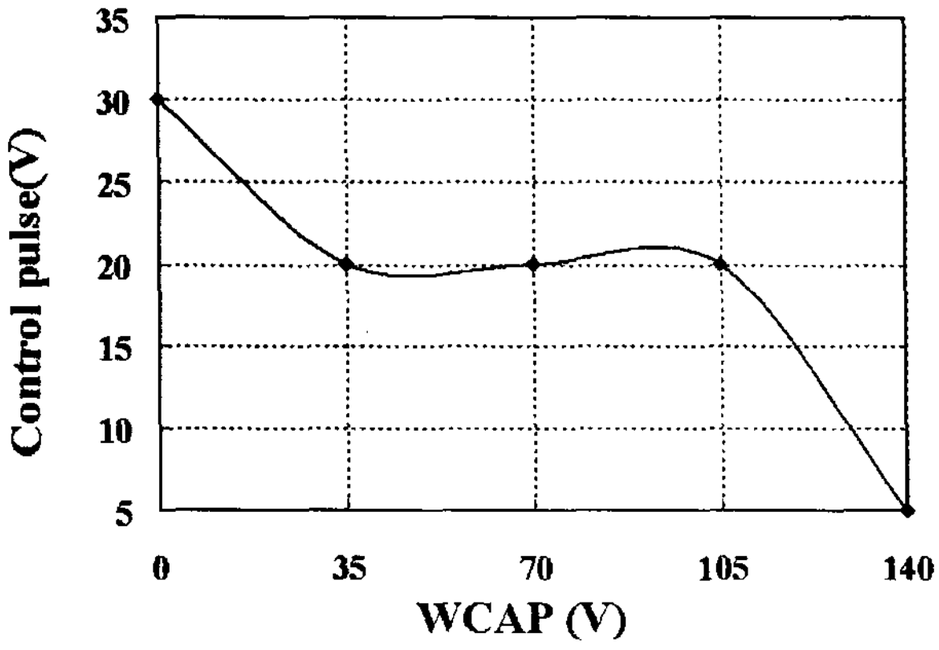

Fig. 6 Control pulse applied on Z electrode versus WCAP.

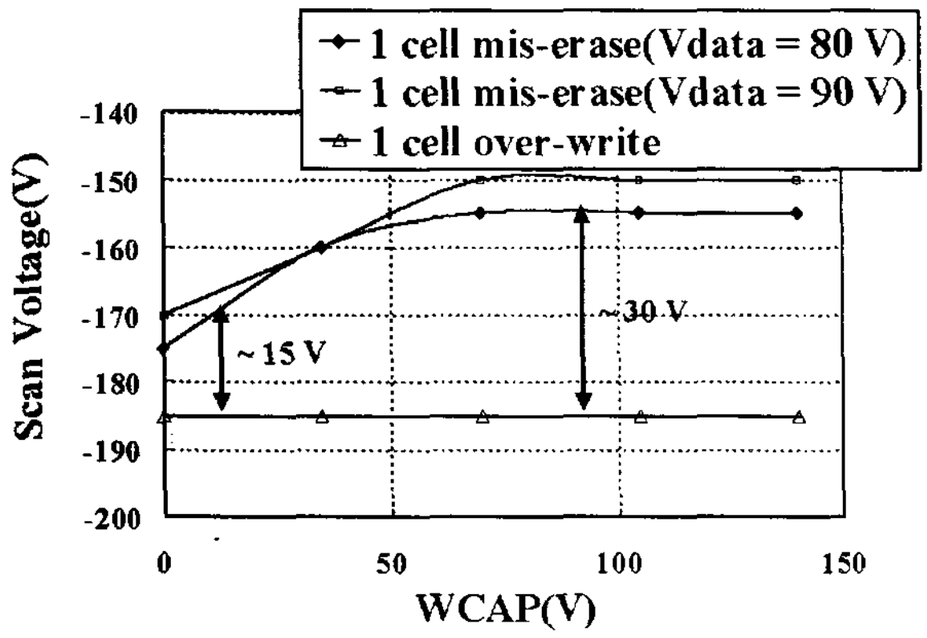

Fig. 7 Dynamic margin