P3.7

New Driving Method for Fast Addressing of AC-Plasma Display Panel

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Abstract

A new driving method is proposed to reduce the address period. The scan time of new driving method overlaps with the next scan time during the discharge lag time. Thus, without reducing the address pulse width and the scan pulse width, the new addressing method can reduce the address period. The results show that the scan time of about 100ns ~ 300ns can be overlapped without the misfiring,.

1. Introduction

An AC Plasma Display Panel (PDP) has many advantages such as its large size, wide viewing angle, and simple structure. However, it also has many defects such as the low luminance efficiency, the low luminance and so on [1-2]. The reason of these problems is very long address period. Due to the long address period, PDP has the low display duty ratio [2-3] so the luminance is low. In order to compensate the low luminance, the high frequency driving can be used. However, the high frequency driving can reduce the luminance efficiency.

Recently, in order to solve these problems, the address driving methods using the priming particles have been introduced [3-4]. However, they need additional electrode and expensive scan driver, and induce the low darkroom contrast ratio. The discharge lag time is one of the factors of the long address period. In this study, the new driving method, that the scan times overlap with the next scan time during the discharge lag time, is proposed to reduce the address period. The new addressing method can reduce the address period without reducing the address pulse width and the scan pulse width.

2 New addressing method

Figure 1 shows the schematic diagram of the voltage waveform and the photo waveform during the address discharge. T_A is the address pulse width and T_D is the discharge lag time. As shown in figure 1, if the pulse is applied to the address electrode, the address discharge is induced after the discharge lag time. Due to the discharge lag time, the address pulse width is increased. In order to decrease the address period, the discharge lag time has to be decreased.

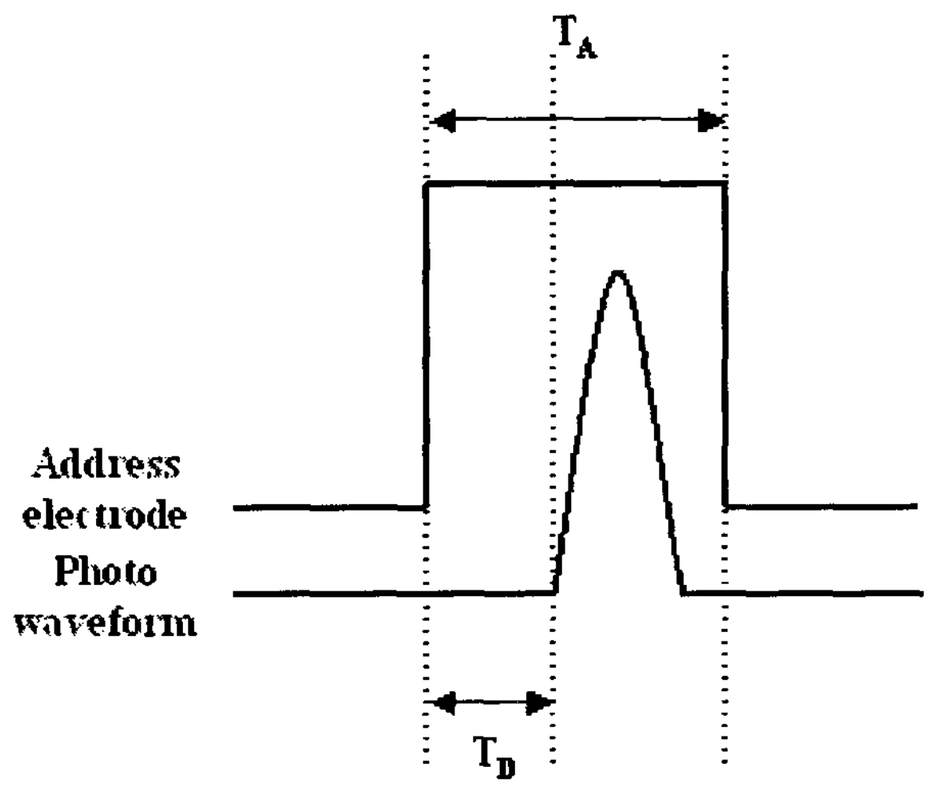

Figure 1. Schematic diagram of the voltage waveform and the photo waveform during the address discharge

Figure 2 shows the schematic diagram of the new addressing method for fast addressing. As shown in figure 2, The characteristic of the new addressing method is that the address pulse and the scan pulse overlap with those of the next scan time. Namely, each one of scan times overlaps with the next scan time during T_O. Then, when PDP has vertical

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resolution of N lines, the new address method can decrease the scan time of $T_O \times (N-1)$. The overlapping time (T_O) must be shorter than the discharge lag time (T_D). If not, the misfiring occurs in the overlapping period. Also, if the address discharge occurs in a line, the misfiring is easily induced in the adjacent line due to priming particles by the address discharge.

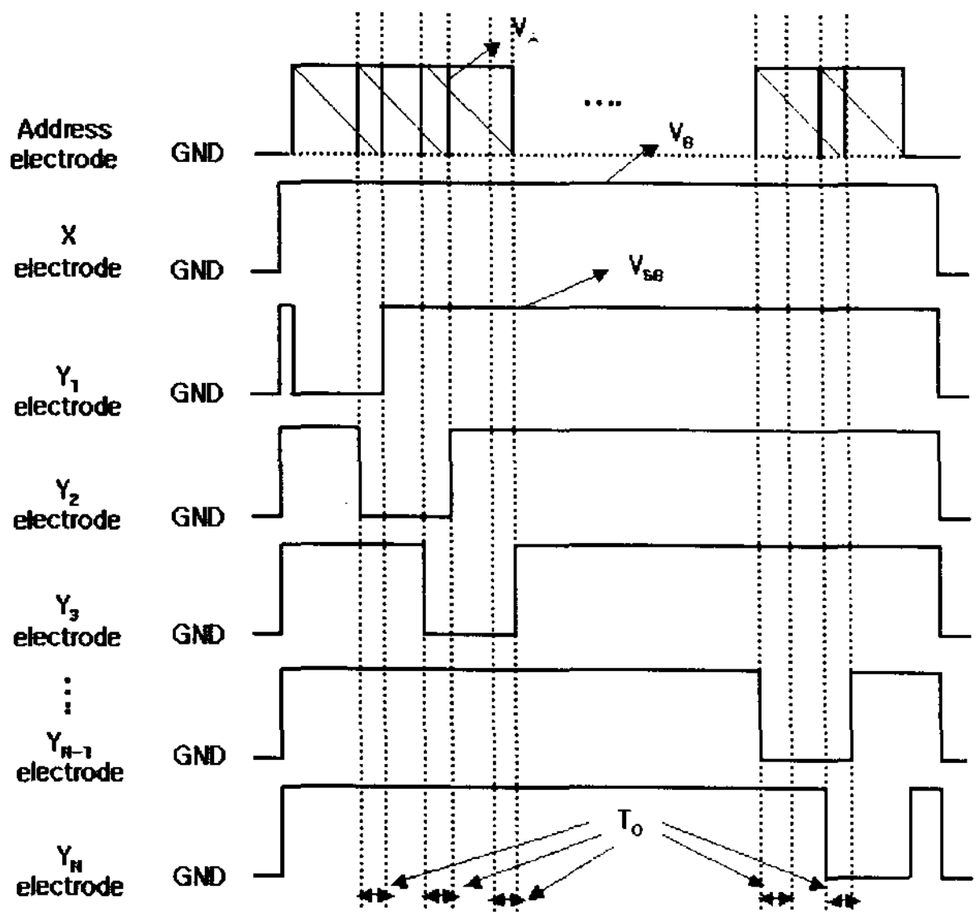

Figure 2. Schematic diagram of the new addressing method for fast addressing

2 Experimental

Figure 3 shows the schematic diagram of the single pixel structure of the AC-PDP used in this study. The single pixel is the minimum unit for full-color display. The panel consists of a front glass plate including ITO electrodes, bus electrodes, dielectric layer, and MgO layer and a rear glass plate including the barrier ribs. The R, G, and B phosphors were deposited between the barrier ribs in the rear glass plate.

The test panel used in this experiment is 7.5 inch diagonal with XGA resolution. The width of ITO electrodes is 275㎛ and the gap distance is 65㎛. The width of bus electrodes is 90㎛. And the height of barrier rib is 130㎛.

Figure 4 shows the schematic diagram of the driving waveform in this study. The one TV-field consists of eight sub-fields and the period of one sub-field is 2㎳. The voltage of V_S, V_W and V_B are designed to 170V, 230V and 170V. The frequency of sustain is 50 . A driving circuit, which is connected with the power supplies, is controlled by pulse generator(Time-98). The voltage waveform is measured by oscilloscope and the photo waveform is measured by a photo detector. Table 1 shows the specifications of the photo detector.

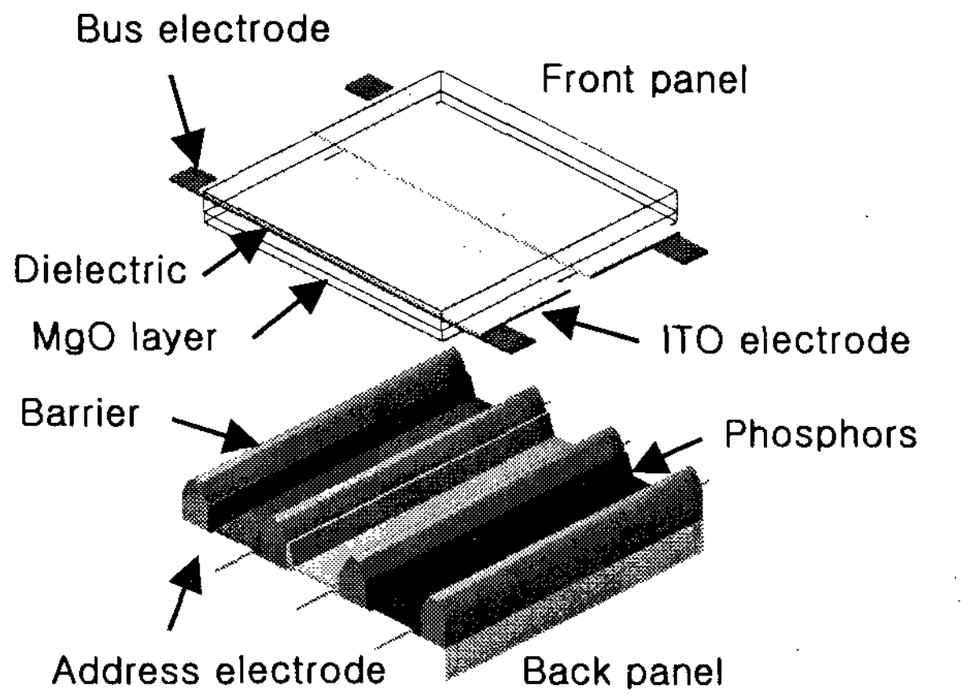

Figure 3. Schematic diagram of the single pixel structure of the AC-PDP

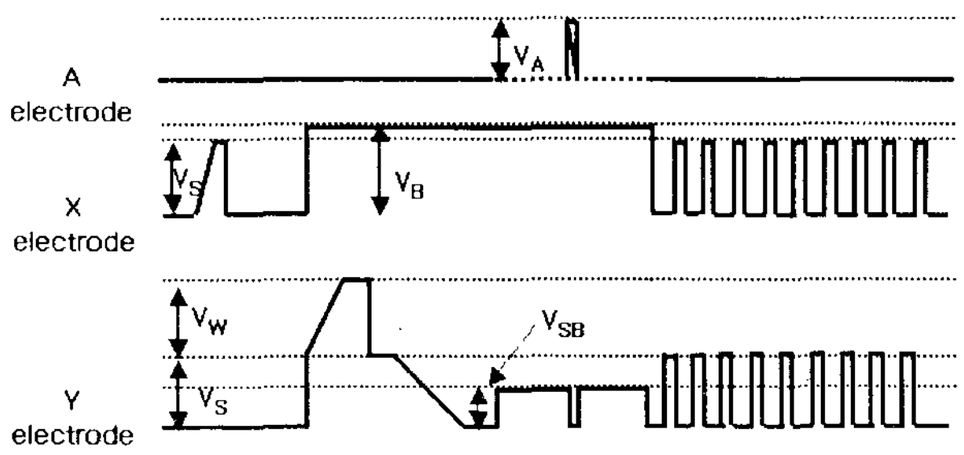

Figure 4. Schematic diagram of driving waveform

ø1.5㎜	Active Area
400㎚ to 1000㎚	Spectral Response
800㎚	Peak Wavelength
0.5 A/W	Photo Sensitivity (800㎚, gain=1)
±2.5% Typ. ±5 Max.	Temperature Stability of gain (25℃ ± 10℃ gain=30)

Table 1. Specifications of the photo detector

3 Results and discussions

Figure 5 shows the voltage waveforms and the photo waveform during the address period. As shown in figure 5, T_A is 2.5 ㎲ and T_O is 300 ㎱. V_{SB} is set to 80V. In order to decrease the address period, the scan pulses overlaps with scan pulses of adjacent line about 300 ㎱. Thus, without decreasing the address pulse width and the scan pulse width, the new addressing method can decrease the address period.

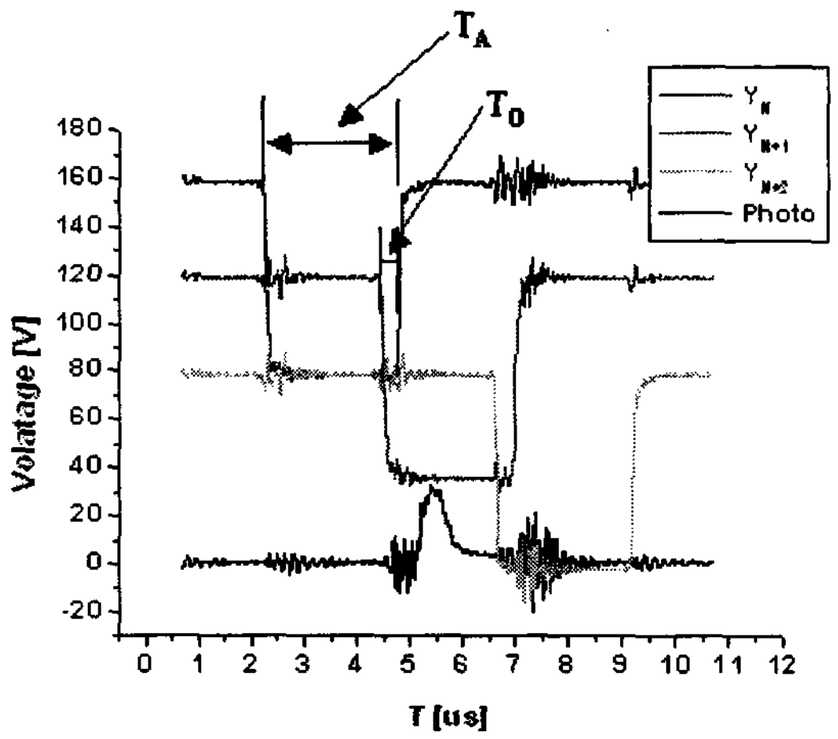

Figure 5. The voltage waveforms and the photo waveform during the address period

Figure 6 shows the address voltage margin for different T_A and T_O. T_A is the address pulse width and T_O is the overlapping time of the scan pulse and the address pulse. As shown in figure 6, the new addressing method can decrease the address maximum voltage. The longer T_O, the lower address maximum voltage. That is due to the priming particles by the address discharge of the adjacent cells. When T_A is 2.5 μs, 2.0 μs, and 1.5 μs, the scan times can be overlapped until 300 ns, 200 ns, and 100 ns. When T_O is increased, the address minimum voltage is equal to that of the conventional addressing method but the address maximum voltage is decreased.

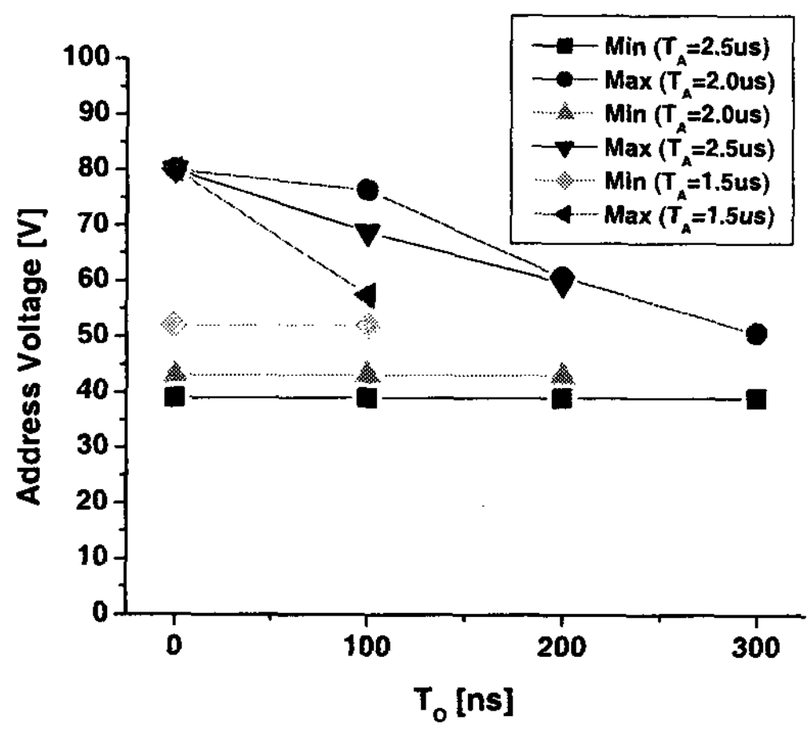

Figure 6. Address voltage margin vs. different T_A and T_O

The new addressing method has the defect of low address maximum voltage as shown in figure 6. However, the higher scan base voltage (V_{SB}) can increase the address maximum voltage. Figure 7, 8 and 9 show the address voltage margin as a function of V_{SB}. As shown in figure 7, 8 and 9, if V_{SB} is increased, the falling time of scan pulse is increased about 30ns. Thus, the address discharge is just a little weakly induced and the long falling time of scan pulse can increase the address minimum voltage by about 2V. However, the higher V_{SB} can increase the address maximum voltage of the new addressing method. When V_{SB} is 100V, it's address maximum voltage is saturated. The higher V_{SB} can improve the address margin but not increase the overlapping time compared with the result in figure 6.

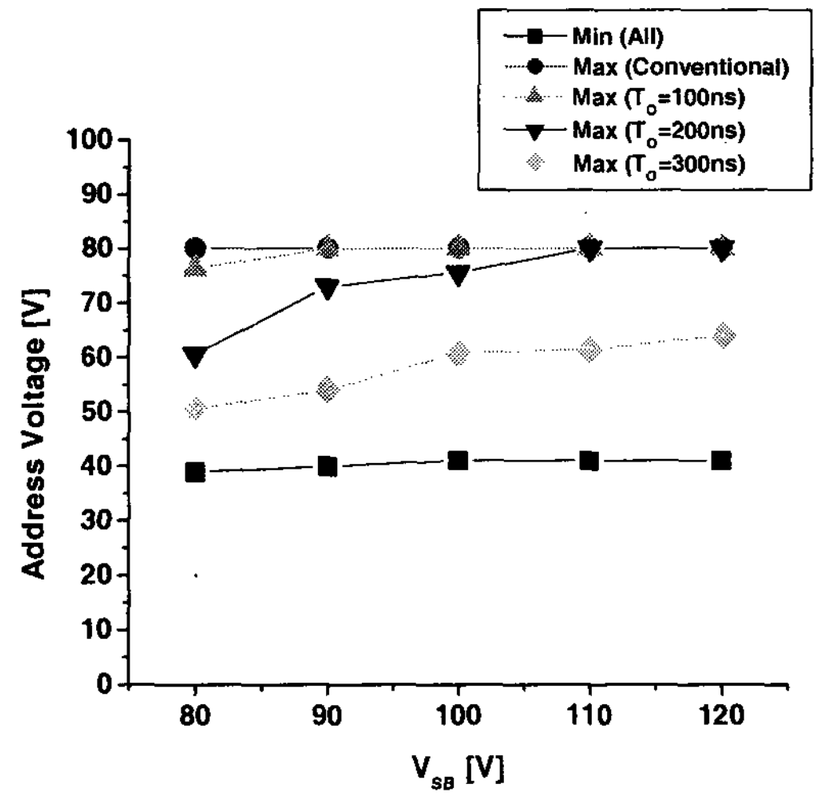

Figure 7. Address voltage margin vs. different T_A and T_O (T_A=2.5μs)

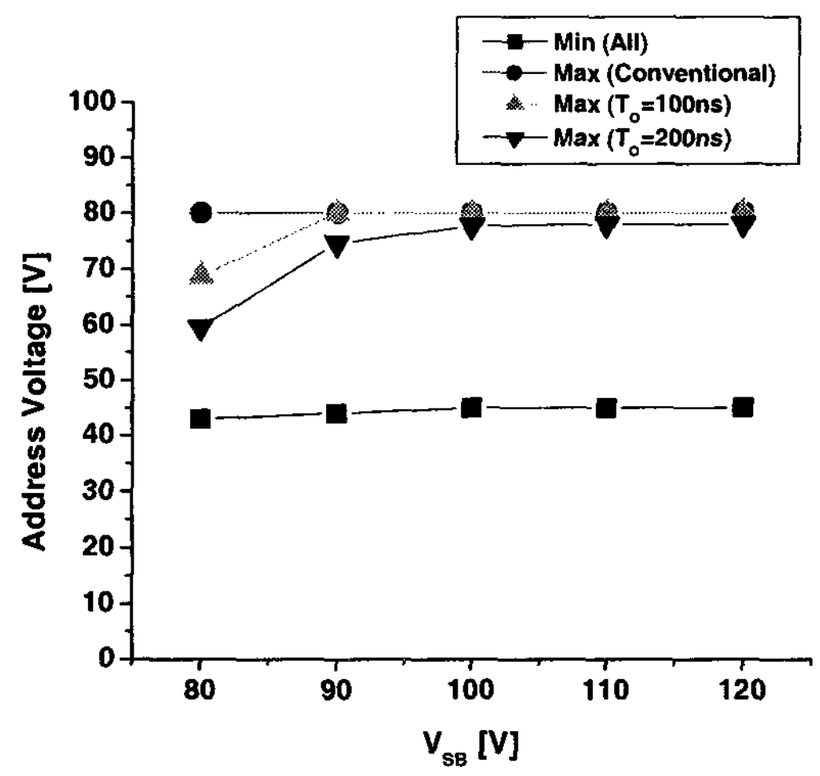

Figure 8. Address voltage margin vs. different T_A and T_O (T_A=2.0μs)

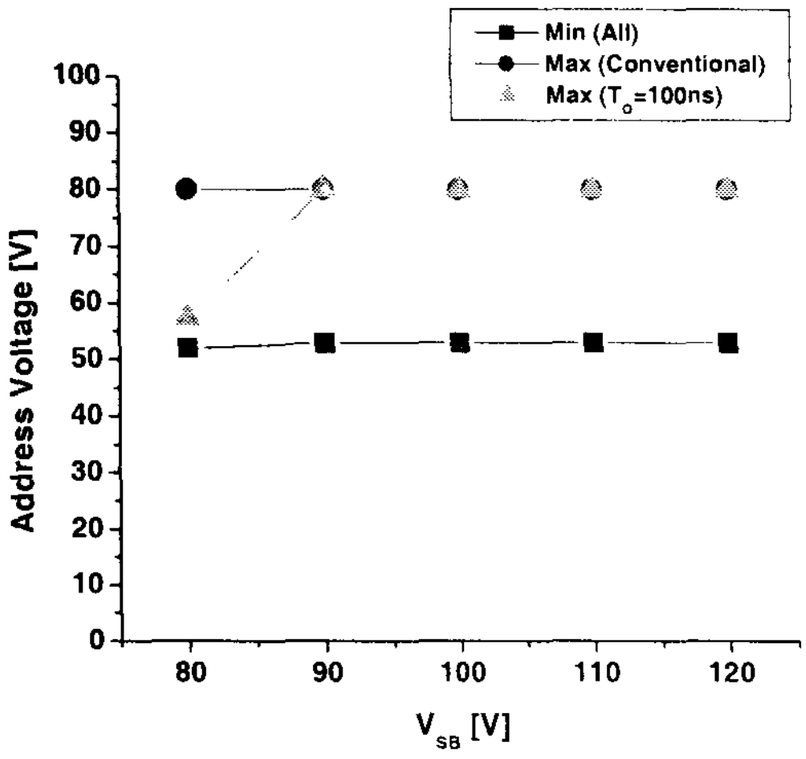

Figure 9. Address voltage margin for different T_A and as T_O (T_A=1.5μs)

Figure 10 shows the patterns which are displayed on 7.5-inch diagonal panel using the new addressing method. The displayed area is 7 lines vertically and 21 lines horizontally.

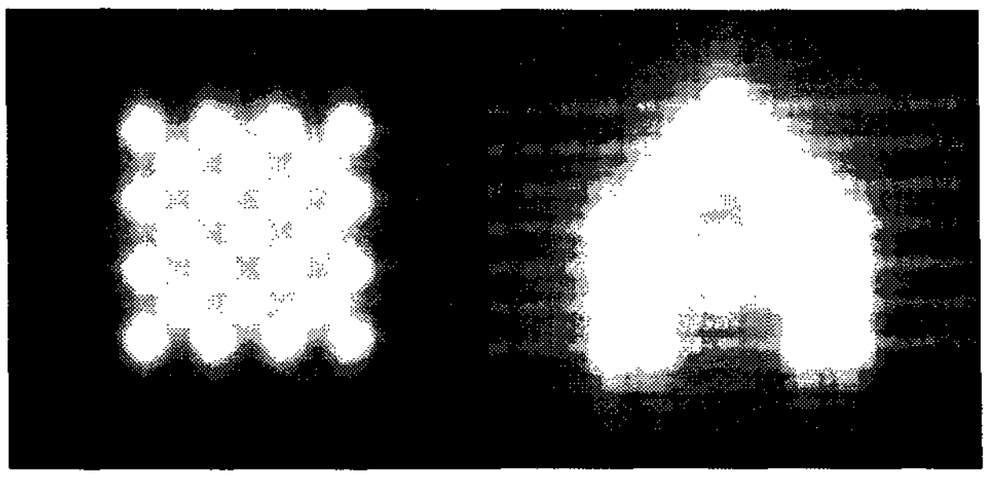

Figure 10. Photograph of the new address method

4. Conclusion

In order to reduce the long address period, which is one of the main problems of AC-PDP, we proposed a new addressing method. The scan times of the new addressing method can be overlapped during T_O. Without reducing the address margin, the new address method can overlap the scan times by 100ns~300ns. If scan times of PDP, which has vertical resolution of N lines, are overlapped by T_O, the new address method can decrease the scan time of $T_O \times (N-1)$.

5. Acknowledgements

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6. References

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[4] J. Y. Yoo et al, "High Speed-Addressing for Single-Scan of AC PDP" SID'01, pp798-801, 2001.