Measurement of Wall Voltage in Reset Discharge of AC PDP

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Abstract

In AC plasma display, it is very important to quantify the wall voltage induced by the wall charge accumulated on the dielectric surface. If we know the quantities of the wall voltage in each period of every sequence; reset period, address period and sustain period, then it helps us to design the optimal driving waveform for high efficiency plasma display. We develop a new method to measure the wall voltage with VDS (Versatile Driving Simulator) system. From this method the wall voltage induced by a wall charge profiles just after the reset discharge of every cells in plasma display panel can be investigated and analyzed successfully. It is noted that the wall voltage profiles are influenced by the space charge and then they are stabilized as time goes by. It is also noted that both the remaining wall charge at the previous sequence and space charges contribute to wall voltage quantities just after the reset discharge. It is noted that the wall charges contribute dominantly after a few hundreds microseconds, while the space charges have been decayed within 100 μs just after the reset discharge.

1. Introduction

It is very important to measure the wall voltage induced by the wall charge accumulated on the dielectric surface by the ramp detecting pulse method. The reset period in driving sequence of plasma display plays an important role in improvement of the display quality. The purpose of this study is to experimentally measure the exact wall voltage profiles at every period. For the design of the optimal reset driving waveform and the perfect initialization, we have to know that the wall voltage quantity and wall charge state. We also compared ramp detecting pulse method by VDS system with charge-voltage (Q-V) Lissajous analysis method.

2. Basic Concept

In this experiment, we have developed the ramped detecting pulse method with VDS system, which is newly introduced method to measure the wall voltage quantity and the wall charge state.

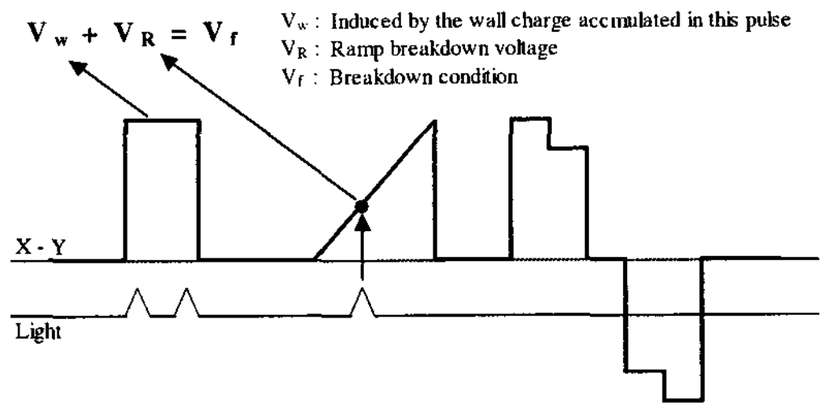


Figure 1. Breakdown condition

We measured the wall voltage by just inserting a

ramped detecting pulse at the observance timing position and making observations of the breakdown voltage on rising (or positive) or falling (or negative) slope of ramped detecting pulse. In case of applying the ramped detecting pulse to X and Y electrode, it is clear that the discharge is ignited at the moment, where the sum of wall voltage (V_w) and ramp breakdown voltage (V_R) is just equal to the firing voltage (V_f) as shown in Figure 1.

This can be written as following equation.

$$V_w + V_R = V_f \qquad (1)$$

Figure 2 is the screen capture of editing program of VDS and it shows the squared reset pulse, ramped detecting pulse and erase pulses used in this experiment. At first, as shown in Figure 3 (a), if the positive ramped detecting pulse is applied to the electrode X, the discharge is ignited at the moment where the sum of previously formed wall voltage (V_w) and positive ramp breakdown voltage (V_R^+) is just equal to the firing voltage (V_f) and this can be written as following equation.

$$V_w + V_R^+ = V_f \qquad (2)$$

Next also as shown in Figure 3 (b), the negative ramped detecting pulse is applied to the electrode Y, then the discharge is ignited at the moment where the sum of wall voltage (V_w) and negative ramp breakdown voltage (V_R^-) is just equal to the firing voltage (V_f) and this can be written as following.

$$V_R^- - V_w = V_f \qquad (3)$$

Therefore, the wall voltage is obtained from the equation (2) and (3), which is half of the difference between positive and negative ramp breakdown voltage as following.

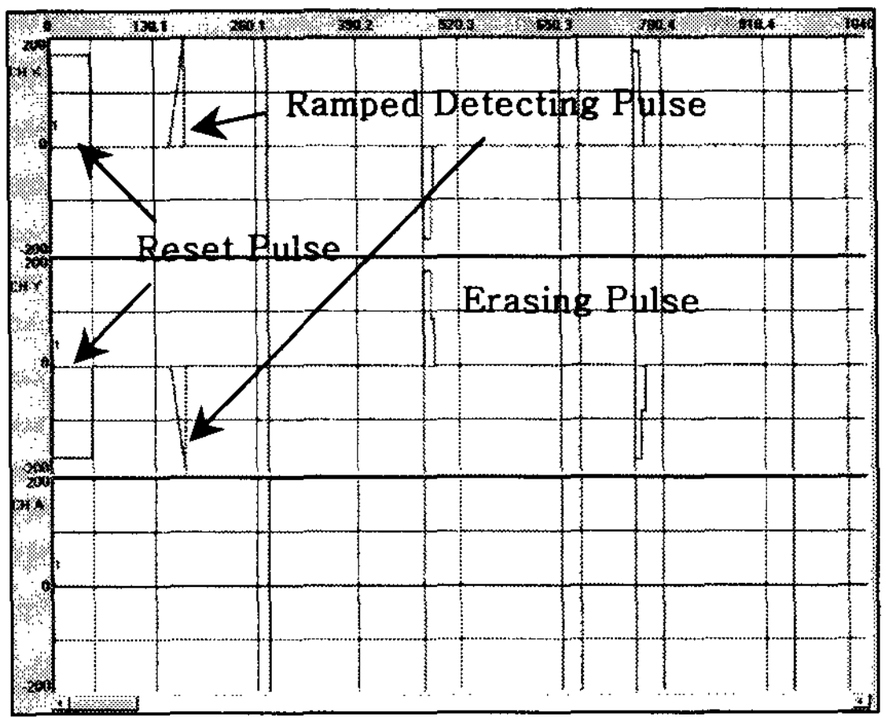
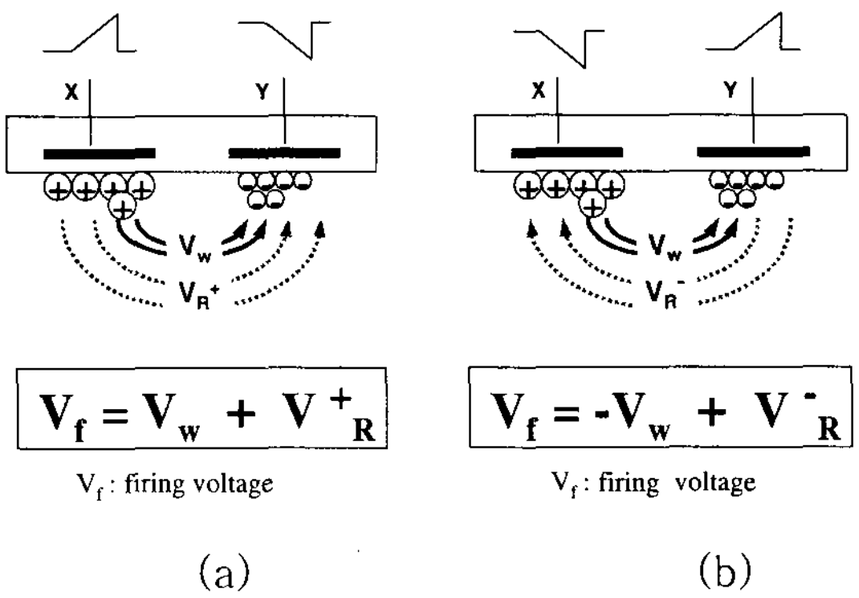


Figure 2. Screen capture of VDS system



(a) (b)

Figure 3. Firing voltage for positive and negative ramped detecting pulses

$$V_w = \frac{\left| V_R^+ - V_R^- \right|}{2} \qquad (4)$$

Consequently, we could obtain the wall voltage by just applying the positive and negative ramped detecting pulse, respectively, to the observance timing sequence.

3. Experimental Results and Discussions

The squared reset pulse is applied to the X and Y electrode with 50 μs in width and 260~380 V in height within variable voltage range. The ramped detecting pulse is also applied to the both electrodes

with voltage slope of 10 V/μs. And the time interval between reset pulse and detecting pulse is varied from 10 μs to 200 μs. Figure 4 and 5 show the positive ramp breakdown voltage (V_B^+) and negative ramp breakdown voltage (V_B^-), respectively, when detecting pulse timing after reset is varied from 10 μs to 200 μs and and variable reset voltage range of from 260 V to 380 V. Figure 6 shows wall voltage profiles, the wall voltage profiles show a disturbed tendency in the region of 0~80 μs for detecting pulse timing after reset discharge, and show a nearly constant value in the region of 80~200 μs for detecting pulse timing after reset discharge.

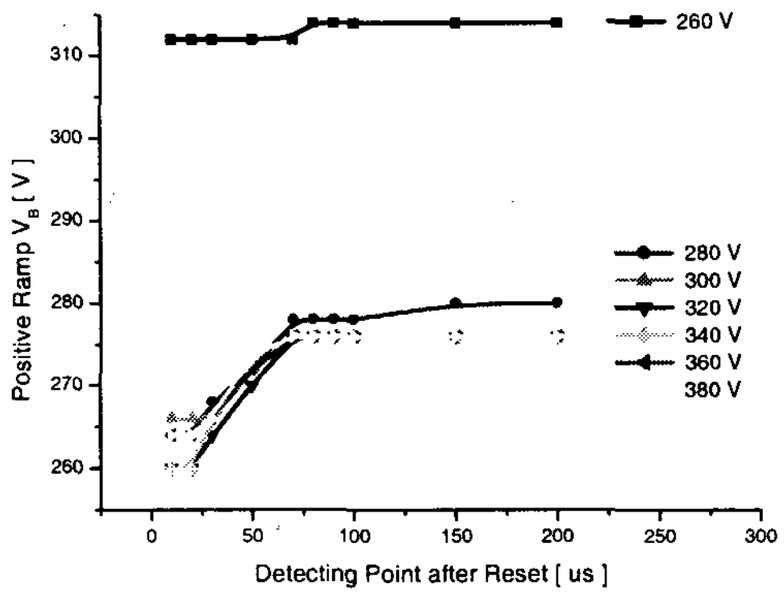


Figure 4. Positive ramp breakdown voltage with various reset voltage and detecting point after reset

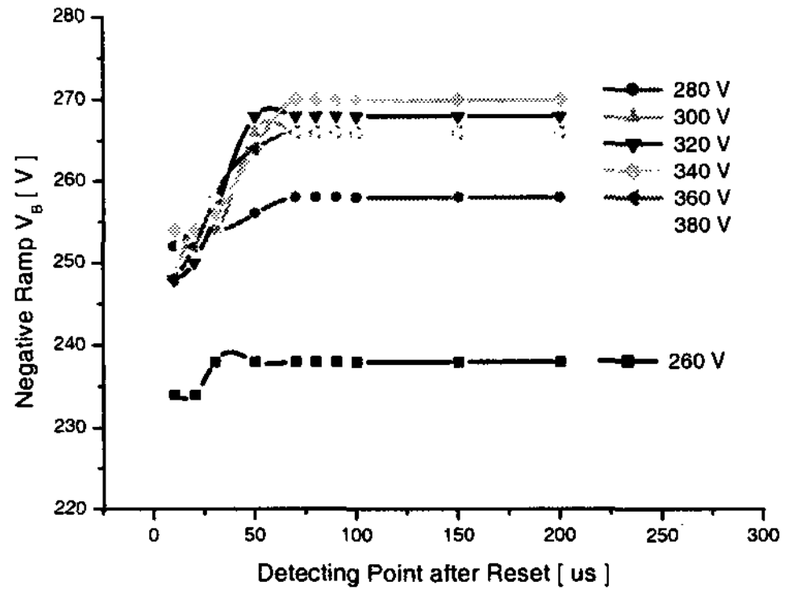


Figure 5. Negative ramp breakdown voltage with various reset voltage and detecting point after reset

These characteristics are caused both by the existence of priming particles in discharge space and wall charge accumulated on the dielectric surface. Therefore, the obtained wall voltage quantity right after the reset discharge is dominantly influenced and disturbed by the priming particles in discharge space. After 80 μs of reset pulse, the obtained wall voltage quantity is attributed to the wall charges rather than the priming particles because the most priming particles are decayed. The wall voltage after the reset discharge is found to be nearly constant value of 3 ~ 4 V in range of 80~260 μs. It is noted that the decay time of priming particles is measured to be about 80 μs, where the lifetime of the wall charge is measured to be more than 200 μs in this experiment.

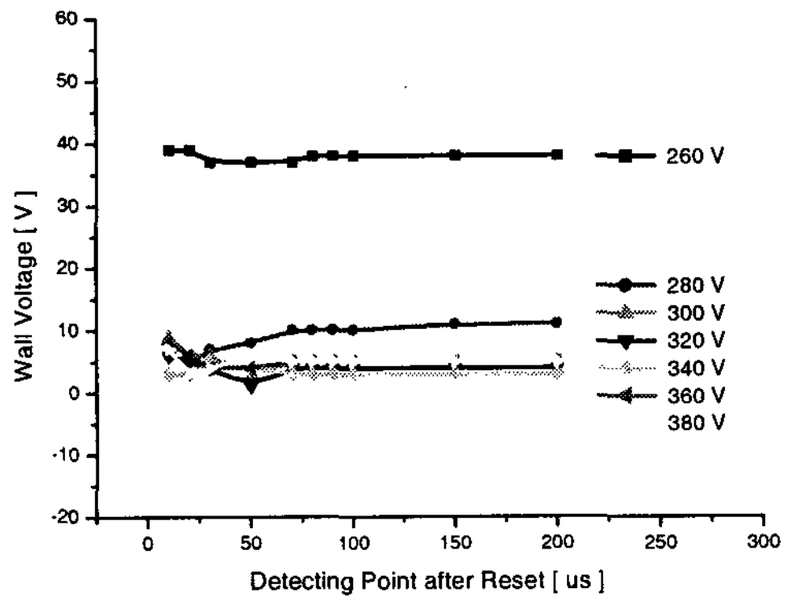


Figure 6. Wall voltage profiles with various reset voltage and detecting point after reset

In Fig. 6, the wall voltage just after the reset discharge is decreased as the applied reset voltage is increased, and nearly constant value of 3 ~ 5 V at the higher voltage regions than 280 V. These characteristics are caused by effective self-erasing discharge occurred at the preceding reset discharge. Figure 7 shows ramp breakdown voltage profiles versus reset pulse width. For relatively short pulse width ranged from 1 μs to 4 μs, the

self erasing discharge is very strong enough to change the polarity of wall charge.

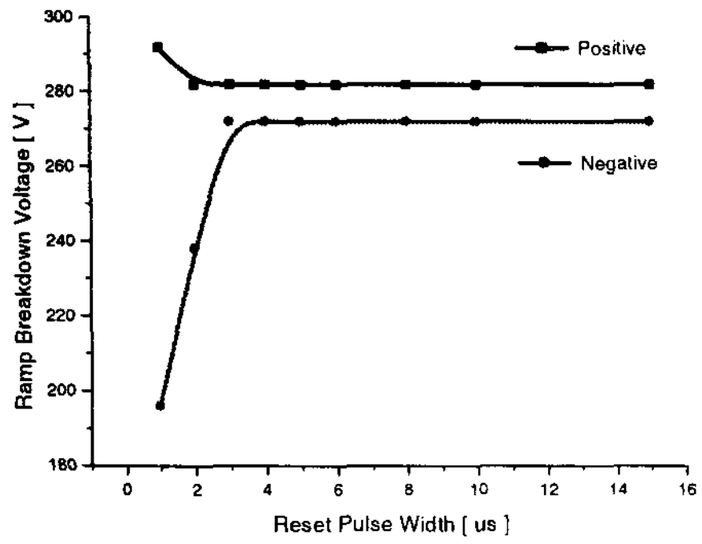


Figure 7. Ramp breakdown voltage profiles versus reset pulse width.

These characteristics might have originated from the priming particles of the space charge rather than the wall charges according to the pulse-width, in which the amount of wall charge accumulated on the dielectric surface is small for a short pulse-width compared with that in the case of the long pulse-width. These characteristics reveal that the existence of optimum reset pulse width for stable writing address. In this experiment, the optimum reset pulse width must be over than 5 μs for perfect initialization of panel and for stable writing address.

4. References

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