Design of PDP Driving Waveforms for Enhanced Stability

Seok-Il Kim and Ju Young Jeong

Dept. of Electronic Engineering, The University of Suwon, Kyongki, Korea 82-31-220-2168 jyjeong@suwon.ac.kr

Abstract

We made an optimization effort on driving waveforms for the Quantized Memory Addressing (QMA) in selective write mode of operation. It was necessary to add long ramp type erase pulses after the total write pulse and the sustain period to obtain stable intermediate luminance discharges. Furthermore, fast rising ramp type total write as well as two step addressing scheme were adopted for better discharge stability.

1. Introduction

We have reported the Quantized Memory Addressing (QMA) method[1] which modulated the wall charge quantity during the address period and exhibited various luminance during a sustain period. Since this method can express multiple gray levels at one sub-field, one can reduce the number of sub-fields[2] required and therefore increase the sustain period and effectively drives higher resolution PDP's. Furthermore, we have reported that 7 sub-field three wall charge states QMA driving could eliminate the dynamic false contours effectively[3].

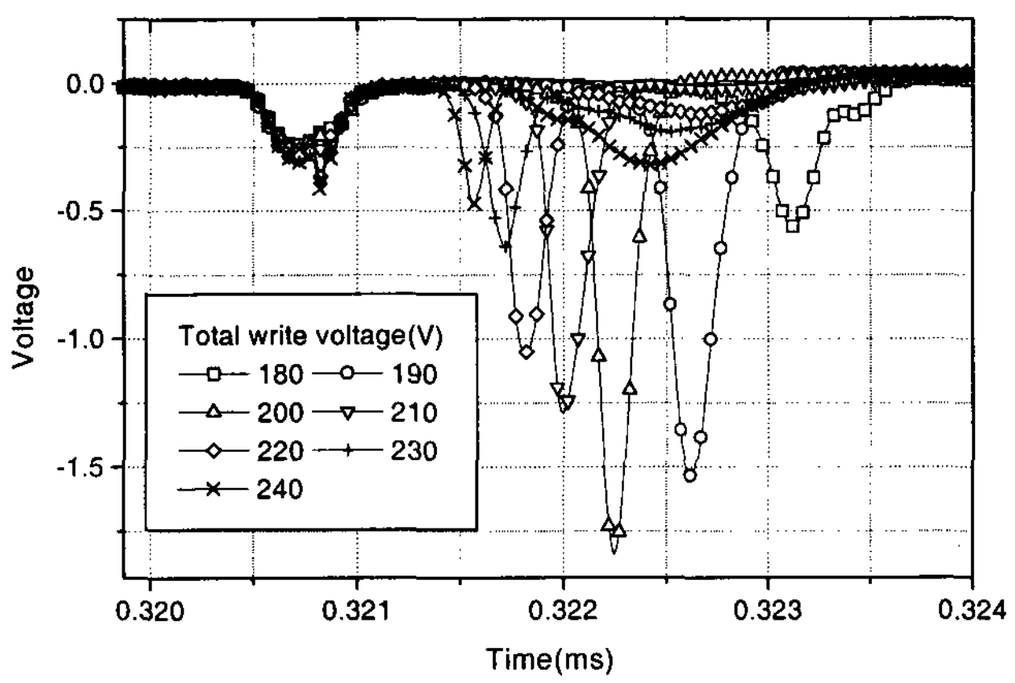
We used the selective write driving mode to minimize the background luminance and found flickers at some cells in the intermediate wall charge state (half-on state). We believed that the flickering was caused by non-uniform wall charge distributions among discharge cells. Therefore, we needed to find proper driving waveforms which could minimize the irregularities in discharge cells.

In this paper, we report the result of waveform optimization and effect of each component.

2. Experimental Results

We used 2" three electrodes test panel with phosphors and driving waveforms were designed and applied by using FT Lab's arbitrary waveform generator. We used three different methods to measure panel luminance. Average luminance was measured by photo transistor array connected in parallel for sensitivity. Discharge currents were measured by Tektronix CT-1 current probe while IR emissions were measured by Hamamatsu C6386 photo sensor/amplifier.

The goal of our experiments was to find optimum driving conditions for reset, address, and sustain period for stable half-ON state. Driving waveforms are made of reset period, address period, sustain period and erase period.



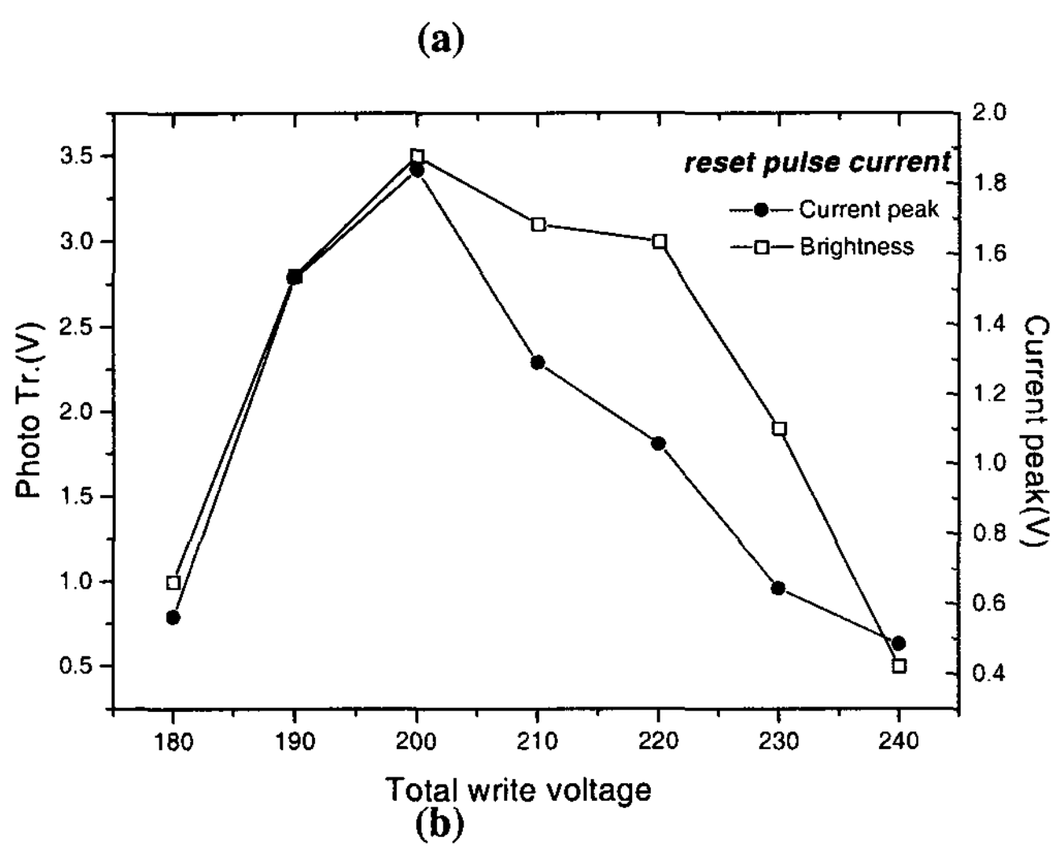
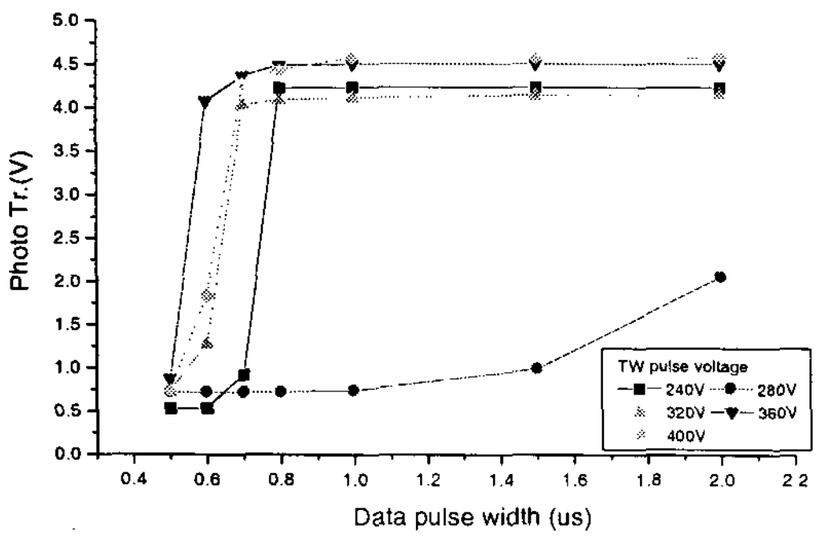
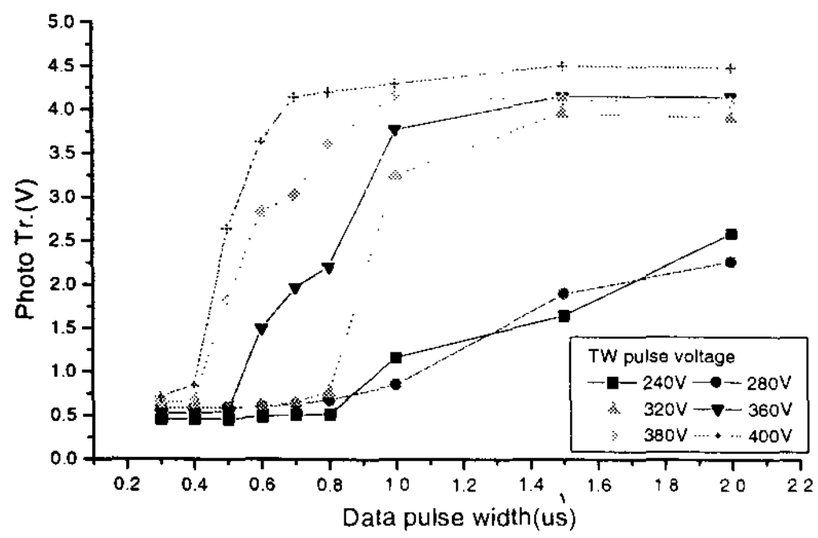


Fig. 1 (a) Discharge current of rectangular total write pulses, (b) peak discharge current and average luminance as a function of total write pulse amplitude.

As a first step, we analyzed the reset period. Since we were using selective write scheme, this period was consisted of total write pulse and total erase pulse. Regarding the total write pulse, we found the amplitude change caused discharge pattern change as shown in Fig. 1(a). One can notice that higher total write pulse amplitude resulted faster breakdown. Furthermore, higher amplitude pulses caused double current peaks. We believed that this wide second current peak was related to wall charge accumulation. Fig. 1(b) is luminance and current peak versus total write pulse amplitude plot. As one can see the peak current reached its maximum at 200 volt pulse amplitude and decreased rapidly at higher voltages. However, the luminance decreased at above 200 volt but it was not as fast as the current decrease. We found amplitude between 210 and 220 volts resulted more stable half-ON state due to proper wall charge elimination by total erase pulse. For total write pulse amplitudes of 230 volts and up, self erase at the falling edge of the pulse occurred. Since wall charges were cancelled by the self erase, following total erase pulse and address pulse acted as a write pulse and erase pulse, respectively. This phenomenon resulted rapid luminance drop and panel behaved abnormally.



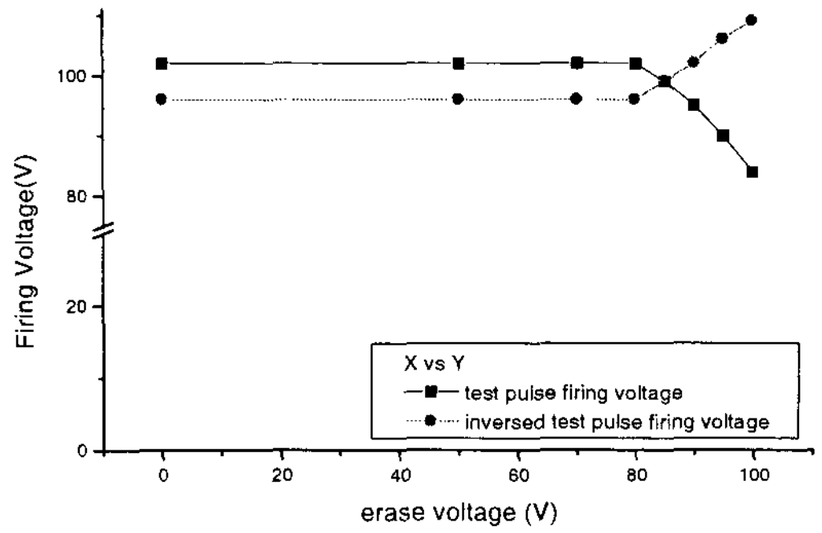
(a)



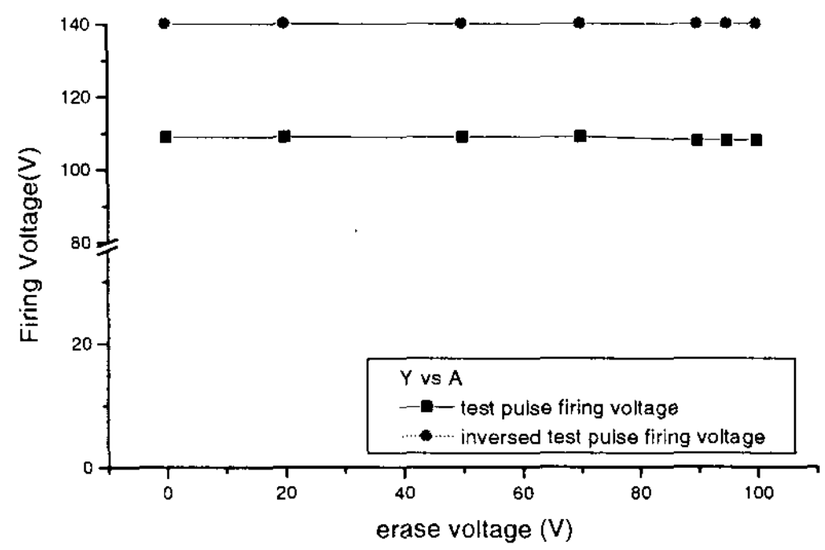
(b)

Fig. 2 Effect of total write pulse shape (a) rectangular, (b) fast rising ramp pulse

We further found that the shape of the total write pulse affected luminance characteristics. Fig. 2 shows luminance versus data pulse widths characteristics for rectangular and fast rising ramp total write pulses. For the rectangular pulse, luminance changed abruptly and half-on state was very difficult to define. On the other hand, fast rising ramp type total write pulse made the transition less abrupt and we were able to define half-on state more effectively. Typical rising time of the ramp type pulse was 5 usec.



(a)



(b)

Fig. 3 Vf measurement result for wall charge estimation. (a) Vf of X-Y discharge, (b) Vf of Y-A discharge.

Regarding the total erase pulse which was applied after the total write pulse, we used triangular pulse in order to induce weak discharge[4]. In conventional driving scheme, this total erase pulse was applied between X and Y electrodes. However, we found that there were some wall charges induced on the data (address) electrodes and caused unexpected firing voltage increase during the address period. Fig. 3 showed the firing voltage measurement results. The difference between two measurements represents the wall charge quantity. From the figure, one can see that the wall charges can be eliminated at X and Y

electrodes by applying 85 volts peak triangular total erase pulse. On the contrary, wall charges remain unchanged at the address electrodes.

Since the wall charges on the address electrodes caused firing voltage fluctuation during the address period, we added triangular pulse to the address electrode to prevent charge accumulation on the data electrodes during the total erase. In Fig. 4, we plotted firing voltage of data pulse as a function of peak value of triangular pulse applied to the data electrodes. As expected, the firing voltage decreased because the additional pulse eliminated unnecessary wall charges built up on the data electrodes during the total erase.

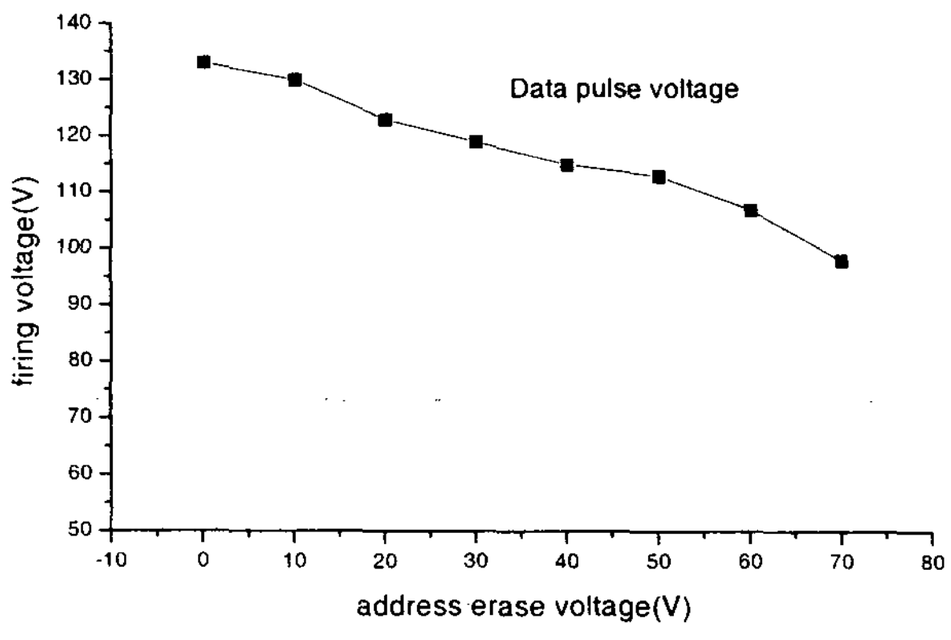


Fig. 4 Data pulse firing voltage versus peak voltage of triangular pulses applied to data electrode during the total erase.

For the address period, we adopted two step writing scheme[5] for better half-on state stability. First step of the addressing was done by applying data pulses on address and Y electrode. Additional discharge pulses on X and Y electrode was applied to stabilize wall charges induced during the first address discharge. This two step address discharge helped to obtain stable half-on state.

Moreover, we found the addition of erase period after the sustain period helps panel stability.

With the components mentioned above, we have tuned parameter values for the most stable half-on state and high peak luminance. Our intermediate tuning results were summarized in Table 2 and the shape of the final waveform is shown in Fig. 5. We were able to reduce the flickering at the half-on state but further study is required to ensure practical operating voltage margins. Photos of test panel in fully-on state and half-on state was taken and shown in Fig. 6. As one can see, we were able to achieve higher stability half-on state.

Table 1 Tuned parameters for stable half-on state driving waveforms

	X	Y	Address
$V_{total\ write}$	110 v	-110v	0
$Width_{total\ write}$	5 usec	5 usec	
$V_{peak\ total\ erase}$	-75V	75V	-70V
$Width_{total\ erase}$	30 usec	30 usec	30 usec
$V_{address\ 1st}$	20 V	-80 V	110 V
$V_{address\ 2nd}$	-50 V	50V	0
$V_{sustain}$	80 or -80V	-80 or 80V	0
$T_{sustain}$	30 usec	30 usec	

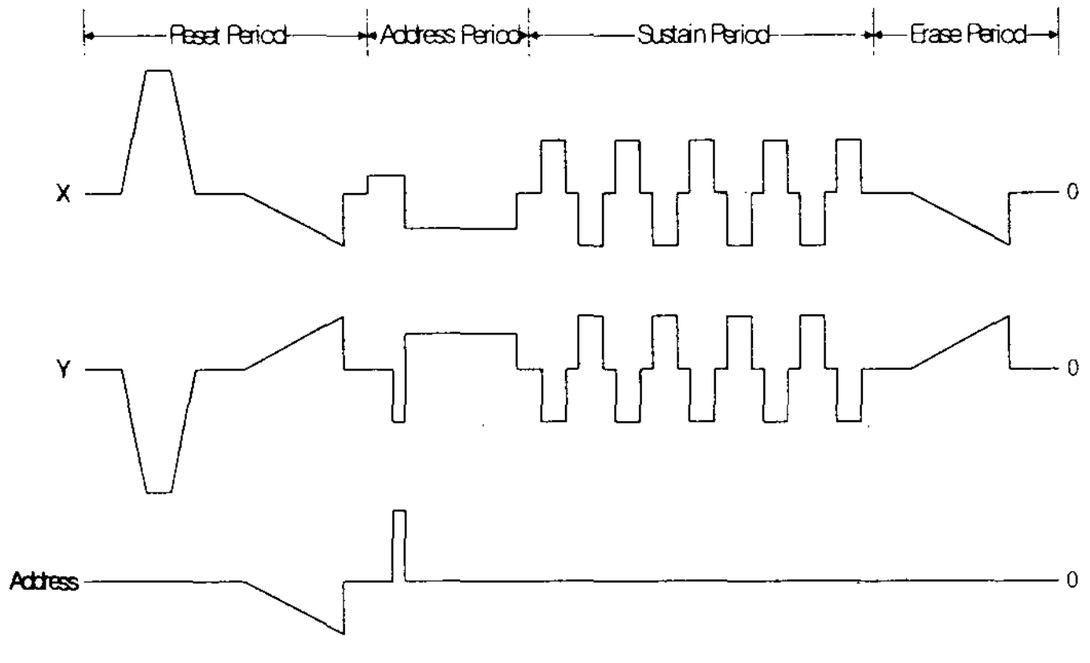


Fig. 5 Final waveform for stable half-on.

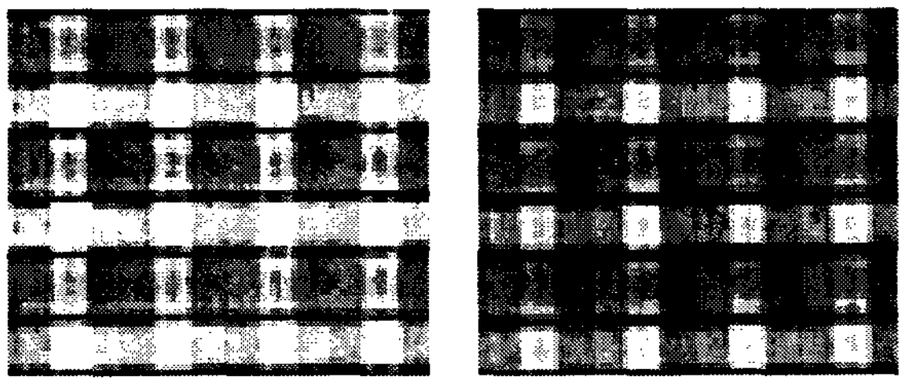


Fig. 6 Pictures of test panel in fully-on (left) and half-on (right) state.

3. Discussion

Improved discharge stability for half-on state is very important in implementing the new QMA driving technique. It also helps designing conventional driving waveforms for low power, high efficiency PDP driving.

Selective write driving scheme was chosen because of low background luminance. However, we had to use complicated driving waveform to take advantage of the QMA driving method. These advantages

include less number of sub-fields for grey scale as well as reduced dynamic false contours in moving images.

Through the process of parameter tuning for higher stability, we found that fine control of wall charge quantity was possible only by better reset process. In conventional driving methods, developers used high enough reset and address discharges which could easily overdrove the discharge cell characteristic fluctuations. However, for QMA, one needed to turn cells half-on and could not over-drove.

4. Conclusion

We designed and analyzed each component of PDP driving waveforms in order to obtain stable discharge conditions for the half-on state. We found more careful reset is essential to the three wall charge state driving. Furthermore, we needed to use two step addressing scheme in order to establish and maintain small wall charges that corresponded to the half-on state. By using more sophisticated driving waveform for reset and address period, we had to sacrifice portion of time that can be used for sustain discharges. After tuning, we were able to improve the discharge stability. However, we suspect that our results may not be optimum driving condition.

5. Acknowledgements

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6. References

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