Electrical Characteristics of Pentacene-based TFTs with Stacked Gate Dielectrics

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Abstract

Using stacked organic gate insulators and active layer of pentacene deposited at elevated temperatures, pentacene-based organic thin-film transistors(OTFTs) with improved electrical characteristics have been fabricated. Stacked PVP(Polyvinylphenol)-polystyrene gate insulators could compensate the demerits and take advantage of the merits of each other [1]. Also, for the better device performance, moderate substrate heating and high deposition rate of pentacene active layer was adopted [2, 3].

1. Introduction

The performance of OTFTs has been considerably improved for several years [4, 5]. Moreover, all-organic TFTs can allow flexible active matrix displays by their integration with organic light emitting diodes or liquid crystal cells on polymeric substrates, and present the possibility for non-planar flexible electronics. Thus, much attention has been recently paid to the all-organic TFT researches [6, 7]. However, OTFTs with organic gate dielectrics prepared using conventional methods only exhibit good performance at high gate voltages and a high dielectric constant gate insulator will reduce the device turn-on voltage. Leakage in deposited organic dielectrics is another problem, which could be reduced by organic dielectrics with high insulating capability. We have shown that, using stacked organic gate insulators (PVP-polystyrene), the drain current levels of the devices were substantially improved and the more evident saturation aspects and less leakage current values than those of the device with the single PVP gate dielectric layer are ascertained. In this study, for the better electrical characteristics of pentacene-based TFTs with stacked gate dielectrics, the effects of moderate substrate heating on the device characteristics are investigated.

2. Experimental Details

OTFTs with stacked gate insulators was fabricated on glass substrates as shown in figure 1. The channel length and width of the TFTs were 50μm and 5mm, respectively. The device has chromium gate and gold source/drain electrodes, which were formed by evaporations through the shadow masks. PVP and polystyrene were chosen as organic gate dielectric materials. Stacked layer of PVP-polystyrene was spin-coated on the patterned gate electrodes at the speed of 2000rpm. The thickness of the individual PVP and polystyrene layer is 410nm and 250nm, respectively. Ethanol and chloroform were used as the solvents for 5wt% PVP and 1wt% polystyrene solutions.

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Pentacene films (65nm thick) were deposited on the dielectric layers under a base pressure of 10^{-6} Torr and at a deposition rate of 2.5Å/sec. During the evaporations, glass substrates were held at 60°C to improve molecular ordering in the pentacene layer. The electrical characteristics of the TFTs were measured by Keithley 238 and 617 source-measurement unit. The thicknesses of the layers were measured by ellipsometry (Plasmos, SD-2100) and α-step profilemeter (Tenkor, 200).

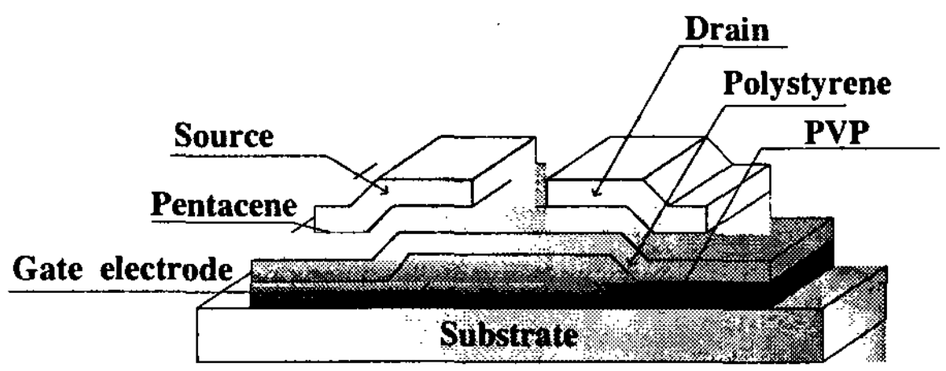

Figure 1. The structure of TFT devices with stacked gate insulators.

3. Results and Discussions

Figure 2 shows the drain current density of the fabricated devices as a function of the drain voltage at the gate voltages of -40, -60V. The saturation current ($I_{D.sat}$) is increased with the substrate temperature.

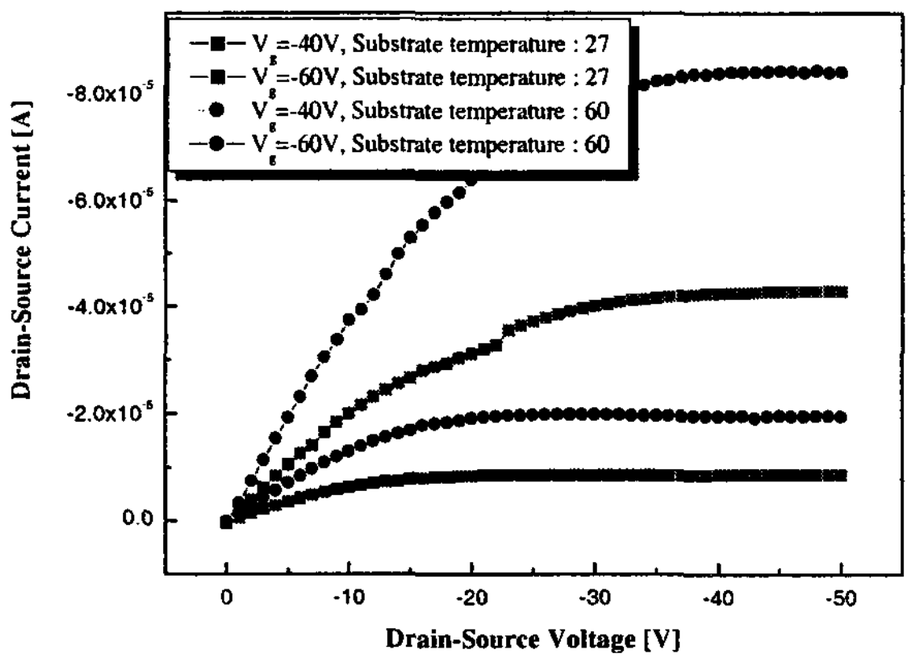

Figure 2. The output characteristics with stacked gate insulators.

The field effect mobility was extracted for this device from the electrical transfer characteristics in the saturation regime at the drain voltage of –30V, and saturation drain current equation (1):

$$I_{D.sat} = \frac{W\mu_{eff}C_i}{2L}(V_G - V_T)^2 \qquad (1)$$

where W is the channel width, μ_{eff} is the field-effect mobility, C_i is the capacitance of the insulating materials per unit area, L is the channel length, V_G is the gate voltage, and V_T is the threshold voltage [8]. The field-effect mobility, μ_{eff}, of the devices with the moderate substrate heating is improved with 0.13 to 0.2cm^2/Vs. Some critical device parameters were extracted and listed in Table 1.

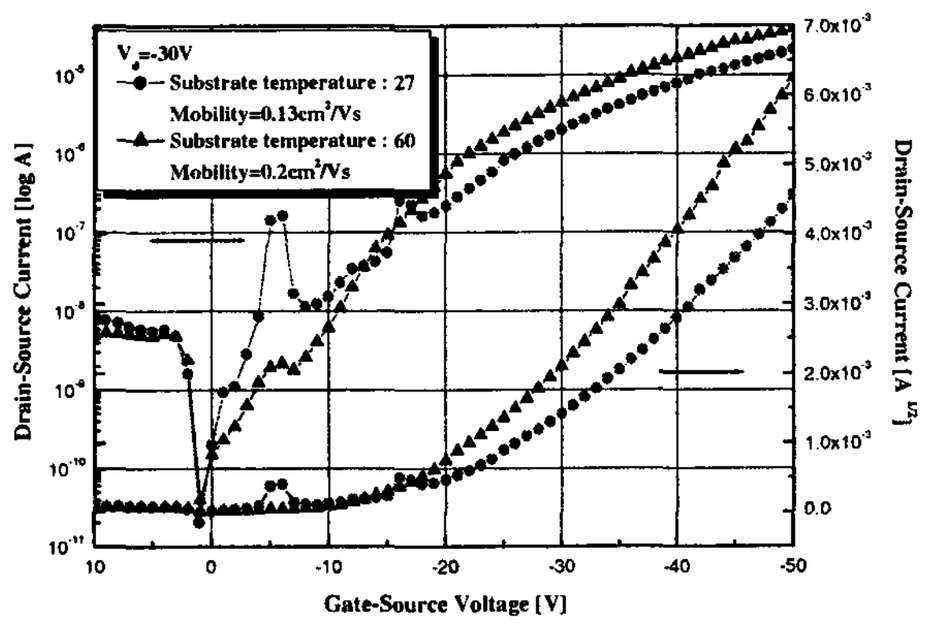

Figure 2. The transfer characteristics with stacked gate insulators.

Table 1. The device parameters of the devices

Substrate temperature [°C]	μ_{eff} [cm^2/Vs]	On/off current ratio	Threshold voltage [V]
27	0.13	$10^{5\text{-}6}$	-6
60	0.2	106	-5

4. Summary

Pentacene TFTs with substrate heating and high deposition rate of the pentacene layer have been fabricated. The electrical characteristics of organic TFT were improved with elevated substrate

temperature, which may be attributed to the molecular ordering in the pentacene layer.

5. Acknowledgements

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6. References

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