Dependence of Stress-Induced Leakage Current on Low Temperature Polycrystalline Silicon TFTs

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Abstract

The dependence of stress-induced leakage current on LTPS TFTs was characterized in this study. The impacts of poly-Si crystallization, gate insulator, impurity activation, hydrogenation process and electrostatic discharge damage were investigated. It was observed more TFTs instable characteristic under those process-assisted processes. According to the LTPS roadmap, smaller geometric and low temperature process were the future trend and the stress-induced leakage current should be worthy of remark.

1. Introduction

Low temperature polycrystalline silicon technology has been the most promising method to manufacture high performance TFTs. Compared to the conventional amorphous silicon TFTs, the LTPS has higher mobility and smaller design rule. With those benefit, the driving circuit can integrate on the LCD or OLED [1].The growing of high system level on panel, a stress induced leakage immunity was indispensable. It was necessary to suppress leakage current, but great numbers of trap states at gate insulator, interface and grain boundary tend to raise arbitrary leakage which results in lowering the design window. To achieve uniformity and smaller geometric, fully dry etching was adapted to control precisely. Moreover, excimer laser irradiation was widely used to reduce total thermal budget and applied in plastic display. The ectrostatic discharge damage was also one of the yield and reliability issues [2]. As all circuits were integrated in one panel and continuous downscaling of device geometries, the LTPS tend to be affected by ESD. To realize system integration and high-resolution display, the process-related reliability aging should be worthy of remark. In order to clarify the dependence of stress induced leakage current, we evaluated the reliability testing in different process in this study.

2. Experimental

The top gate LDD N-channel and self-align P-channel TFTs were fabricated on Corning 1737 glass substrate [1]. First, the buffer oxide layer and 50nm thickness a-Si:H films were deposited by plasma enhanced chemical vapor deposition. Then the polysilicon channel was formed by 308nm XeCl ELC. In this work, 98% laser overlap ratio was adopted to obtain large grain size and better uniformity of active layer. The island was patterned by three plasma dry etching condition (400, 600 and 1200W). The 100nm thickness gate insulator was deposited by TEOS-base oxide and stacked oxide (double-layered of 10nm silane-based oxide and 90nm TEOS oxide). The source/drain and LDD regions were formed by the non-mass-separated ion shower technique. The dopant activation was performed at 450°C thermal furnace, ELA and RTA irradiation [3]. Finally, the interlayer oxide and inter-connection metal were deposited and patterned. The H_2 plasma hydrogenation was performed in a commercial RF parallel-plate plasma reactor at 100W, 400°C with 10min in H_2 and Ar gas mixture. The SiO_2/SiN_X (100nm/200nm) interlayer film and SiN_X (600nm) passivation layer were adopted and baking at 400°C for 30min. A non-contact mode 8KV level ESD impulse was applied to TFT array to evaluate electrostatic discharge issue [4].

3. Results and discussion

3.1. Polysilicon Crystallization

Figure.1 shows the dependence of off-state leakage on inverse channel for various ELC energy densities with 5 micro width devices. We have found that leakage independent of channel length. It indicated that the leakage current was caused by reverse biased drain side. Figure.2 illustrated the relationship between stress voltage and stress-induced leakage. At low fields, the stress induced leakage decrease when increasing the ELC energy density.

The ELC energy density varied from 360 to 380 mJ/cm^2 and the grain sizes were about 200nm, 300nm and 400nm respectively. Although higher energy obtains large grain, the excess irradiation leading mixed phase of microcrystalline and large grain. The leakage can rise by carrier generated via grain boundary or inter-grain traps [5]. We found out that well chosen laser energy density has small stress induced leakage and devices deviation. Thus, the crystallization condition controlled within the optimal window to obtain better uniformity but large grain.

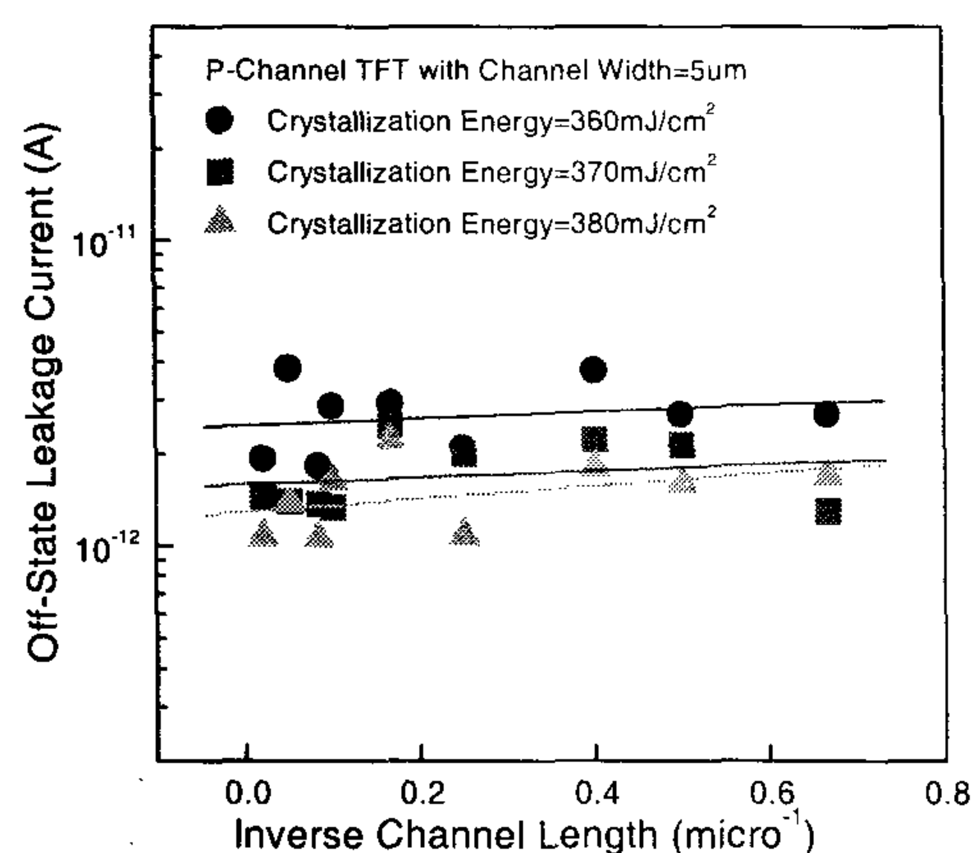

Figure 1. Dependence of the leakage current with ELC energy density on the inverse channel length.

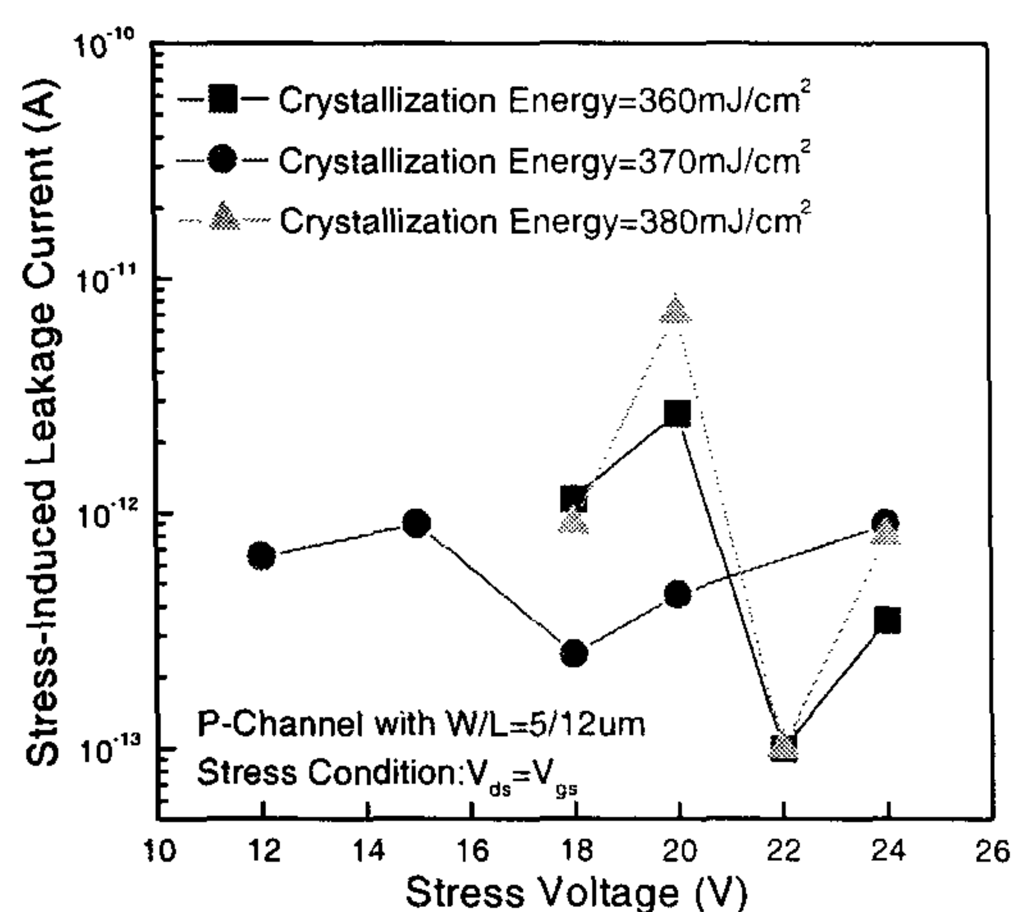

Figure 2. Relationship between Stress-induced leakage current and stress voltage with different ELC condition for P-channel TFTs.

3.2. Plasma Dry Etching Process

To achieve high resolution and throughput, fully plasma dry etching process was necessary. The quality of polysilicon film was the heart of TFTs, but great numbers of trap states in grain boundary influence the performance. The plasma powers, over-etching and antenna ratio in etching step will affect device reliability and low frequency noise characteristics. Traditionally, either hot carrier or gate bias stress has been used to reveal the latent defect in plasma-damaged device [6]. Figure 3 illustrates the stress-induced leakage under different active layer etching powers with gate bias stress. The result means that high plasma power caused more ion bombardment, irradiation exposure and charging, which multiply the meta-stability in the channel and degrade device. The large power etching power shows severe stress induced leakage current both under positive and negative gate bias stressing. It indicated that the energy of etching ion play an important role in plasma damage. The same phenomenon also shows in N-channel LDD TFTs.

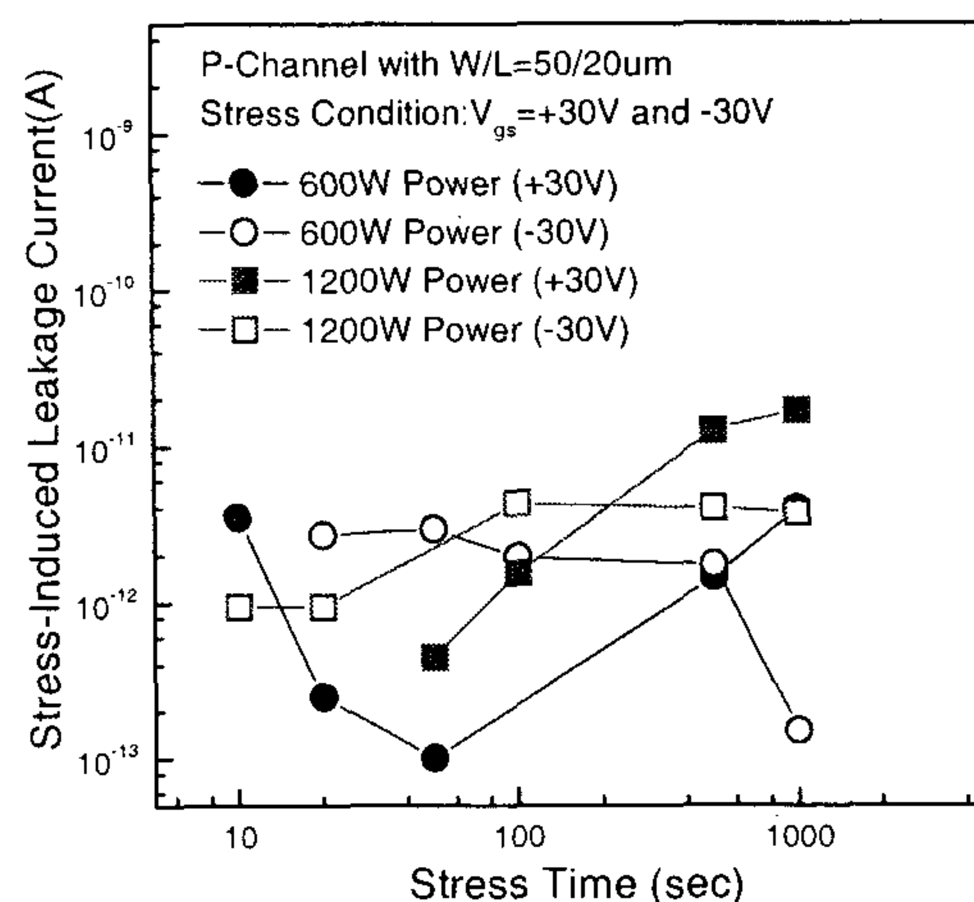

Figure 3. The stress-induced leakage current with different plasma condition during gate bias stressing (V_g=+30V and -30V) for P-channel TFTs.

3.3. Gate Insulator Integrity

To better understand the influence of the oxide integrity, we evaluated the hot carrier stress degradation by using stacked insulator to enhance interface phenomenon. Figure 4 shows that time dependence of the stress-induced leakage with and

without extra interface under hot carrier stress. It was clearly observed that device with extra oxide interface has severe threshold voltage but stress induced leakage current. We suggest that the main reason causing less stress induced leakage current with extra interface-state was the severe threshold shift. The defects within polysilicon dominate the aging mechanism than oxide interface states phenomenon.

3.4. Activation Related Process

In order to reduce residual stress and thermal budget, the ELA and RTA were widely adopt in FPD. Figure 5 shows the different activation methods related to stress-induced leakage current and we found that those with RTA and ELA have large degradation, especially in violent RTA irradiation. The latent damage is not clearly observed in initial characteristic but appears after a harsh operating condition, like gate bias or hot carrier reliability testing. It ruled out that superfluity RTA or laser energy density cause the melt area to reach the edge between source/drain and gate. This implies that it could increase the interface states in SiO_2/poly-Si for both N- and P-channel TFTs. When superfluity RTA or ELA exposures, damage of the polysilicon layer created extra interface-states and causes much more electrons trapping than holes trapping. It was necessary to prevent irradiation energy above melting threshold from the surface amorphization and extra amount of interface-states.

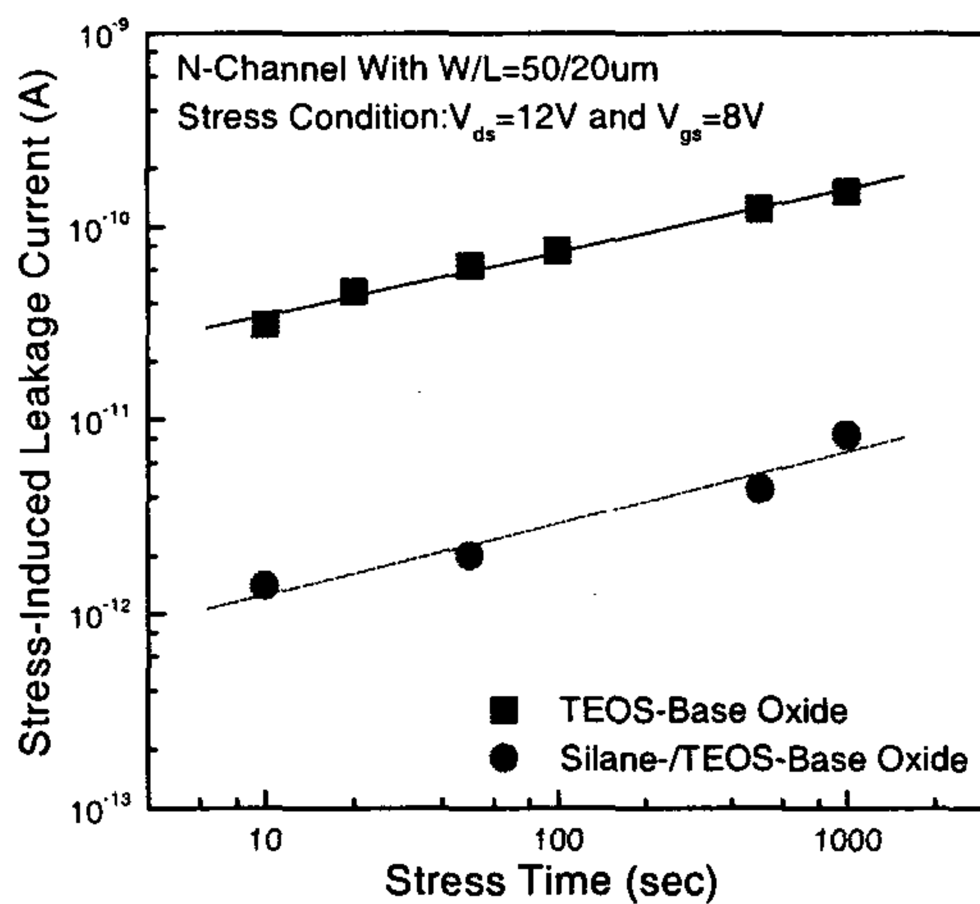

Figure 4. The stress-induced leakage current with different oxide integrity during hot carrier stressing (V_d=12,V_g=8V) for N-channel LDD TFTs.

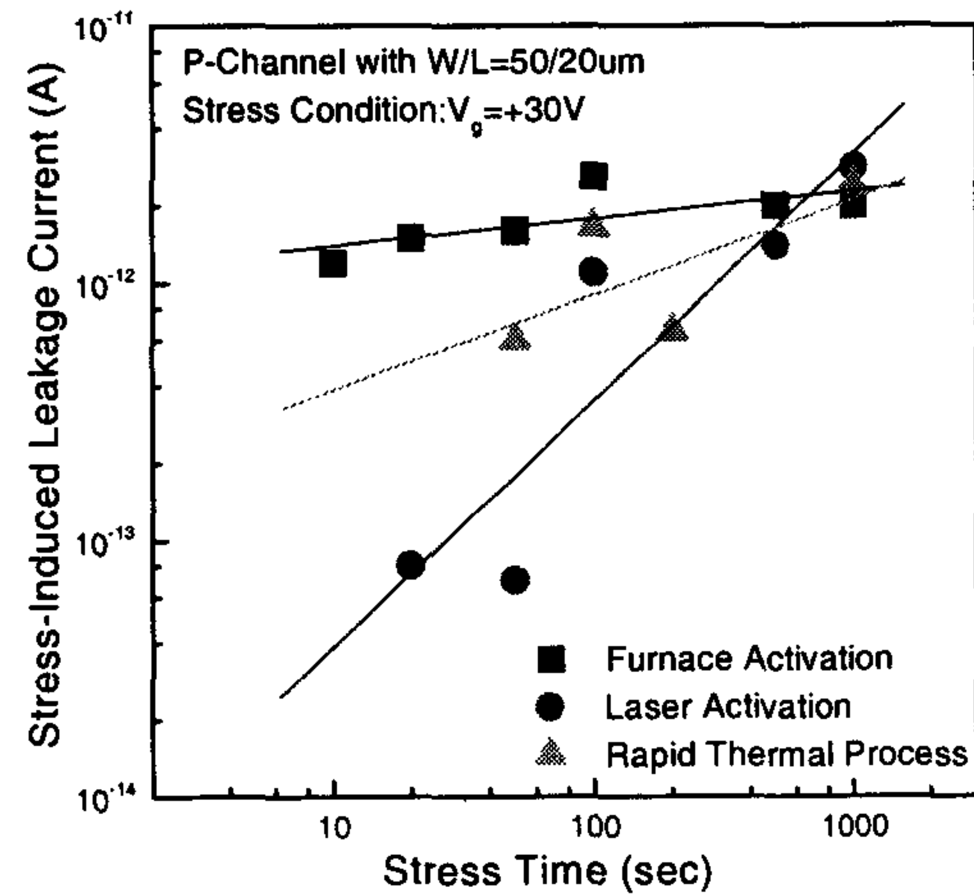

Figure 5. Behaviors of stress-induced leakage current with different activation processes during gate bias stressing (V_g=+30V) for P-channel TFTs.

3.5. Hydrogenation Assisted Process

To realize high performance LTPS TFTs, it was necessary to reduce the defect with polysilicon. Figure.6 shows the various hydrogenation-related processes under hot carrier injecting condition. The stress-induced leakage current can be observed in three kind of hydrogenation sequence. These phenomenons due to the Si-H bonds break during electrical stress, resulting in generation of traps states. The meta-stable states were less in SiN_X passivation devices and the probability of carriers trapping by hot carrier testing was lower.

According to the method described by Levinson et al. [7], the effective trap density (N_t) in polysilicon channel was assessed. We found that N_t is decreased to $7.496x10^{11}/cm^2$ by applying RF H_2 plasma hydrogenation. Furthermore, the interlayer SiO_2/SiN_X and passivation SiN_X layer make effective hydrogen passivation and decrease trap density to $5.926x10^{11}/cm^2$ and $5.11x10^{11}/cm^2$ respectively. Decreasing the trap density effectively reduces the stress induce leakage current. Therefore, the large improvement of stress-induced leakage in SiN_X ones were due to the passivation defects and dangling bonds in grain boundary. It believed that adopted SiO_2/SiN_X and SiN_X passivation were a good choice to obtain more robustness.

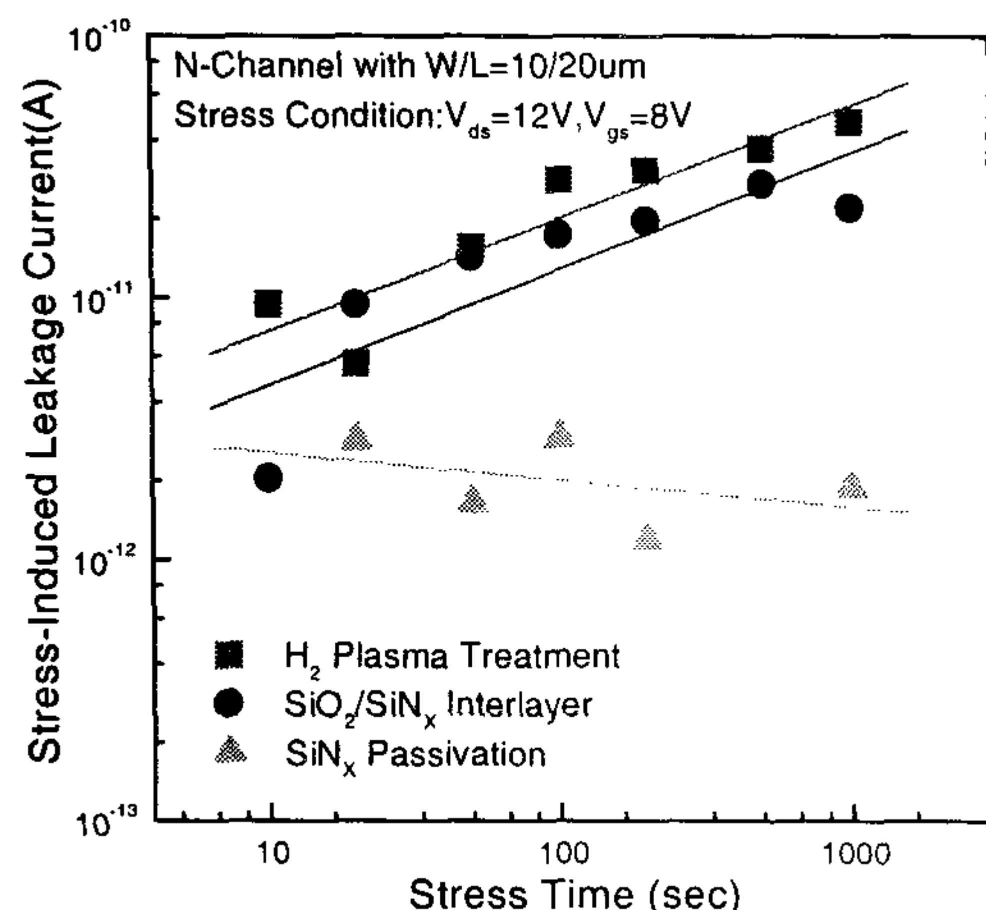

Figure 6. The stress-induced leakage current with with different hydrogenation related process under hot carrier stressing (V_d=12,V_g=8V) for N-channel LDD TFTs.

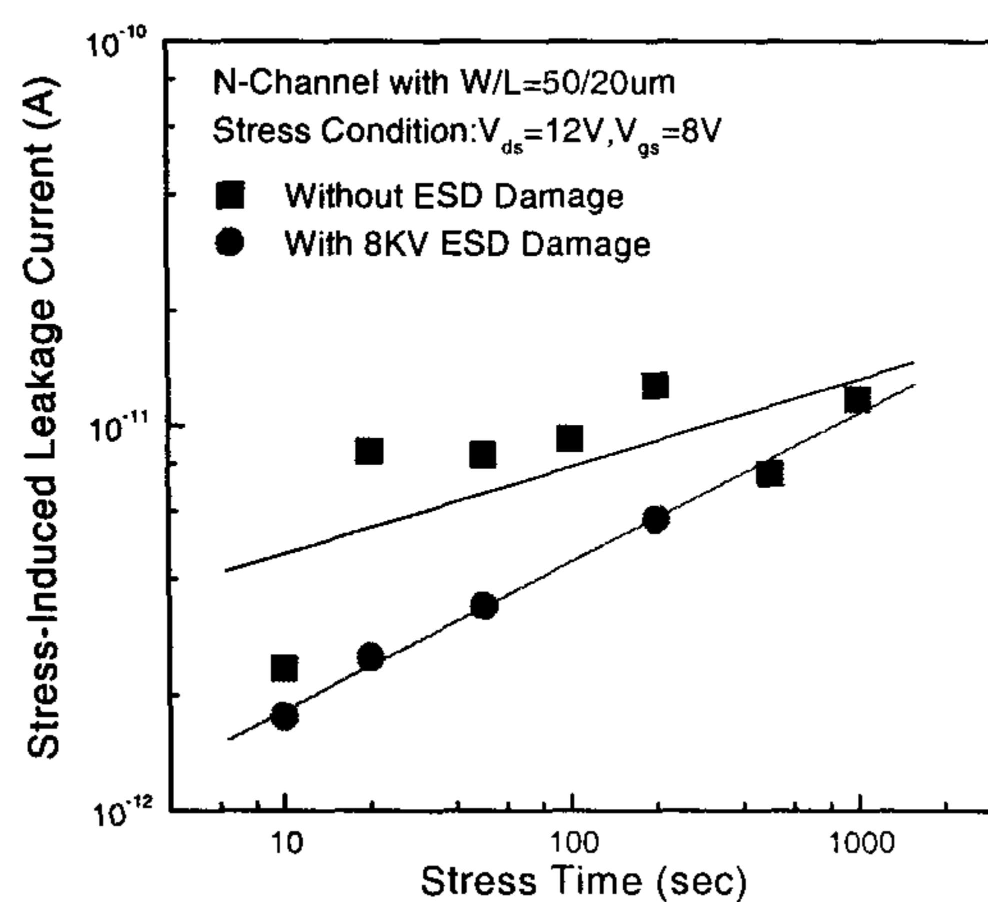

Figure 7. Behaviors of stress-induced leakage current with 8KV ESD impact under hot carrier stressing (V_d=12,V_g=8V) for N-channel LDD TFTs.

3.6. Electrostatic Discharge Damage

Figure 7 illustrates the impact of non-catastrophic ESD stress on hot carrier reliability. We characterized slight degradation in stress-induced leakage for 8KV ESD stressed than fresh one. Under 8KV level, there was not significantly decrease in leakage current. The low level electrostatic discharge pre-stress generated interface states and oxide trapped charges, which weakening of gate insulator but polysilicon layer. The results indicated that ESD induced latent damages has weakened the gate insulator near the drain [4]. During long term hot carrier stressing, the latent damages was revealed. Moreover, as the applied electrostatic discharge amplitude large than 8KV, most failure modes were regard as un-reconstruct breakdown. The same phenomenon also shows in P-channel TFTs.

4. Acknowledgement

The authors would like to thank Mr. Huang, C.-F. for his support RTP experiment and the FPD group of ERSO/ITRI for their comments and fruitful aid.

5. Conclusion

In this study, we investigated the dependence of stress-induced leakage current on LTPS TFTs. The relationship between the polysilicon crystallization, gate insulator integrity, plasma dry etching, impurity activation, hydrogenation process, electrostatic discharge and related reliability were observed. It finds that more stress-induced leakage characteristic under those process assisted processes and the reliability aging should be worthy of remark.

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