LTPS TFT LCD Status, Outlook and Challenges

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ABSTRACT

Low temperature polysilicon (LTPS) TFT LCDs are in production today at sizes ranging from 0.33" for viewfinders to 17" for LCD TVs with 21.3" recently demonstrated. Because of their form factor, resolution, brightness and other benefits, LTPS TFT LCD unit shipments, revenues and capacity are expected to grow rapidly, particularly for mobile applications. However, despite the strong outlook, LTPS TFT LCDs are still faced with numerous challenges from a market and technology perspective. LTPS TFT LCD producers were surveyed on which of the current challenges were the most problematic among other questions.

Introduction and Outlook

LTPS TFT LCDs were first developed by Epson in 1983, with an integrated driver version introduced one year later, and the first commercial product introduced in 1984 by Epson for 2" LCD TVs.[1] LTPS TFT LCDs were actually commercialized two years before Matsushita commercialized a-Si TFT LCDs. However, in 2002, LTPS TFT LCDs accounted for just 4% of the total $22 billion TFT LCD market.

LTPS TFT LCDs offer significantly higher electron mobilities than a-Si TFT LCDs resulting in numerous benefits including:

- A smaller TFT;
- Larger aperture ratios;
- Higher brightness;
- Ability to integrate driver IC and other circuitry;
- Form factor advantages due to elimination of ICs and PCBs;
- Increased ruggedness due to fewer interconnects;
- Potential for lower cost depending on the size and resolution. The higher the resolution and smaller the size, the bigger the cost advantage for LTPS TFT LCDs.
- Potential for significantly lower power through SRAM integration;
- Better ability to serve as a backplane for AMOLEDs due to smaller and more reliable transistors and improved V_{th} shift performance over time.

As a result, we expect LTPS TFT LCD shipments to rise at a 48% CAGR from 2002 to 2007 to reach over 200 million units with revenues rising from $0.9 billion to $4.1 billion equivalent to a 34% CAGR. Unyielded LTPS TFT LCD capacity is expected to rise at a 46% CAGR to 3.3 million square meters in 2007 on significant capital spending.

We are particularly optimistic on the penetration of LTPS TFT LCDs into the mobile phone market where higher bandwidth and increased functionality are boosting demand for higher resolution, increased brightness, improved color saturation, increased gray scale, sunlight readability and increased lifetimes. We also expect LTPS TFT LCD capacity targeting small/medium applications to overtake a-Si TFT LCD capacity by 2006 due to new fabs as well as older a-Si fabs converting to LTPS. As a result, we expect LTPS TFT LCD technology to become the leading color technology for mobile phones in 2005 and account for nearly a 30% share of all mobile phone displays in 2007.

Challenges

Despite the strong outlook, LTPS TFT LCDs are still faced with numerous challenges from a market and production technology perspective. LTPS TFT LCDs are not clearly differentiated in the market vs. a-Si TFT LCDs. Certainly, the typical end user does not know the difference between a-Si and LTPS TFT LCDs. In addition, a-Si TFT LCD suppliers have done a remarkable job in reducing costs due to rapid substrate size growth, process simplification, yield improvement and material cost reduction. Furthermore, a-Si TFT LCD suppliers are able to leverage the integration and cost reduction abilities of the semiconductor industry which negates some of the integration advantages of LTPS TFT LCDs.

Despite its nearly 20-year history, the LTPS TFT array process is still relatively immature resulting in slower than desired cycle time and lower than desired yields. Early challenges which prevented the rapid emergence of LTPS were high process temperatures in the silicon film deposition, crystallization and ion implant steps. These steps were performed at 600°C which not only increased equipment costs but required expensive annealed glass substrates. All of these steps can now be performed at lower temperatures of around 300°C, reducing equipment cost and allowing ordinary non-alkali glass substrates to be used.

LTPS TFT producers are currently pursuing both CMOS and PMOS processes. Companies pursuing CMOS tend to be focused on small/medium displays

where high resolution, high integration and low power are most critical. Thus, these companies are pursuing higher mobilities, narrower design rules and lower operating voltages.[2] Companies focused on large-area displays tend to be more focused on cost than integration and are pursuing PMOS to reduce the number of process steps. While CMOS processes for transmissive displays are currently at 8-9 masks, PMOS features as few as 5 masks. Unique process steps for LTPS include:

Dehyrogenation. A furnace heating step used after the PECVD a-Si deposition to reduce hydrogen concentration in the a-Si layer to <3 atomic percent. This is not a challenging step, but can slow down CVD throughput, the most expensive tool in the fab, as it is typically employed as a facet on the CVD cluster tool. Concerns after the a-Si deposition include surface roughness, film thickness uniformity and good post annealing film characteristics.

Crystallization. In the conventional overlapped scanning, excimer laser annealing (ELA) approach, the a-Si film is melted at temperatures approaching 1400°C and polysilicon grains are formed when the laser pulse turns off. Only the film is brought up to these high temperatures due to rapid absorption and short laser pulses. Pulses are overlapped to reduce the non-uniformities resulting as the middle of the pulse tends to result in better crystallinity than the edges. This step suffers from slow throughput, high consumable costs, small grains of around 0.3 μm which minimizes mobility and pulse to pulse energy variations causing hard to control grain boundaries resulting in variations in mobility and device performance. It is critical to control the size of the grains, the number of grains and their location. Between and within these grain boundaries, there are typically numerous dangling bonds or traps. The deep states, which originate from dangling bonds at the grain boundaries, negatively influence the threshold voltage and sub-threshold slope. The tail states, which originate from the in-grain defects, negatively affect the mobility and leakage current. Challenges for this step include improving pulse to pulse energy variations to less than 2%, reducing the overlap rate to improve throughput and laser life, minimizing grain boundaries, enlarging the grain size and controlling the location of grain boundaries. Two alternative crystallization techniques which produce large grains and control the location of or minimize grain boundaries and are now entering production include metal induced lateral crystallization being commercialized by Sharp which involves solid phase crystallization and ELA, and Sequential Lateral Solidification (SLS) now commercially available from leading ELA supplier JSW which also significantly boosts crystallization throughput due to a smaller overlap. Other alternatives for producing large grains include phase modulated ELA (PMELA), solid state lasers and ELA + solid-state lasers (SELAX).

Higher quality gate dielectric deposition to minimize local breakdown due to poor interface with the rough silicon surface after ELA. Must minimize fixed charge density and provide excellent uniformity to meet flat-band voltage and threshold voltage requirements. Due to these concerns, the gate dielectric has been deposited thicker than necessary and at relatively slow deposition rates which reduces throughput, increases capacitance, reduces TFT drivability and worsens aperture ratio. TEOS is typically used.

Ion implant or ion shower to define source/drain regions, reduce leakage current (LDD) and control threshold voltages (channel doping). Phosphorus and boron impurities are implanted. Because resist masks are typically used, process temperatures should be <120°C which limits high dose conditions. Ion implant systems dominate semiconductor applications, but suffer from relatively high system cost, large footprint and slow throughput in FPD applications. Ion doping systems tend to suffer from reduced dose control due to neutralization of ions produced in low intrinsic range and contamination from hydrogen ions. In addition, temperature control is not as good due to mixing of H+ leading to resist burning. Ion doping is better positioned for high dose implants due to significantly higher throughput while ion implant is preferred for low dose due to better dose control, improved precision, excellent dose countability, a wider variety of gasses, and comparable throughput.

Activation of source/drain implants to reduce sheet resistance. This step aligns implanted impurities into correct lattice sight and heals damage to the silicon. With process temperatures in some cases reaching over 700°C, there are concerns with glass warping, compaction and other damage that needs to be controlled carefully. Most LTPS manufacturers are utilizing rapid thermal processing (RTP). There are two commercially available RTP systems, gas heat type and selective heating lamp type. The gas heat type employs resistive heaters to preheat the substrate and then showers the p-Si layer with hot N_2 or other inert process gasses, momentarily raising the film temperature above 700°C to achieve activation. The selective heating lamp type is a conveyor system that uses IR lamps to preheat the substrate and then raises the p-Si film above 700°C via a UV lamp, where the primary energy is absorbed by the Si film, but not by the glass substrate. The gas heat type system provides good process control and temperature uniformity but is a large, expensive multi-chamber cluster tool. The selective heating lamp type system offers very high throughput, with a relatively small footprint and

excellent cost-of-ownership, but temperature uniformity is not as good as the gas heat type.

Hydrogenation. By the nature of the crystallization process, grain boundaries are formed. Hydrogenation is used to passivate and repair these states. Hydrogenation ties up the numerous dangling bonds and improves device performance. Hydrogenation approaches include furnace annealing, high pressure annealing, RF Plasma, solid source diffusion, and H+ ion implant. In high pressure annealing, the unoxidized silicon becomes free atoms at the Si-SiO2 interface, the free Si atoms diffuse into the polysilicon and defects in the polysilicon are restored by the free atoms.

Interlayer dielectric (ILD) deposition to form contact holes or vias to connect the data bus lines to the source/drain area. Film requirements not as severe as the gate dielectric but tend to be thick with smooth morphology, <10% film uniformity, low temperature, good step coverage, etc.

Dry Strip. After ion implantation, the photoresist will cross-link and harden and become difficult to remove. Therefore, dry strip is typically used to soften the hardened resist followed by a traditional wet strip due to remaining residues.

Finer design rules. While LTPS offers the potential to pattern significant circuitry over much larger substrates which along with eliminating expensive interconnect materials could result in significant cost reduction, the technology suffers from much slower frequencies and larger design rules resulting in larger, slower devices. With XGA data rates at 55MHz, innovating bussing architectures, dual edge clocking, pre-charge circuitry and dual bank configurations are implemented in LTPS. Higher frequencies can be achieved at higher voltages, but this increases power consumption and footprint. As a result, higher frequencies and lower voltages will be necessary for LTPS to maximize its potential. Narrower design rules enable LTPS to maximize frequencies and minimize footprint and lower power through integration of a multi-bit SRAM at each pixel. A 6-bit SRAM can be achieved at 1 μm resolutions allowing 262,000 color images to be displayed at minimal power. However, in conventional exposure systems, getting to narrow design rules will significantly sacrifice throughput as a smaller field lens with slower photosensitivity will be required. In addition, in patterning glass substrates, a large depth of focus is required due to variations in substrate flatness of >20 μm. Resolution limitations from current exposure equipment suppliers are 1.5 μm at 680 x 880mm substrates. One alternative solution is a holographic mask aligner. This technology can form 0.5 μm patterns on large substrates with no field size limitation.

Yield management. Yield management is the process of collecting process and defect data from multiple locations on a manufacturing line, analyzing that data, and generating conclusions to prevent defects and make process improvements. Yield management strategies for LTPS vary significantly from and are less mature than those used in aSi manufacturing. The main differences are the additional tests required for integrated drivers and other circuits as well as the fact that most LTPS displays are for small applications. Small displays tend to have lower quality requirements and a single display has a relatively low value. Most small panel LTPS manufacturers perform array test and inspection for process monitoring only and sort good and bad panels during cell inspection. Defective panels are scrapped, not repaired. Large area, PMOS type LTPS displays may follow a yield management model similar to a-Si, where 100% array test is performed. Integrated driver and other circuit tests are performed electrically. The mechanical issue of probing each display is one of the biggest challenges of LTPS display testing. The small display size means that a single array substrate may contain hundreds of displays, each of which must be probed and stimulated. TACT for array test tools can easily exceed 10 minutes/plate. This probing challenge has led to a greater reliance on AOI, a passive optical inspection rather than an active functional test. It is more flexible than test techniques and is more easily used on different panel sizes and technologies. The lack of common and effective array yield management strategies is believed to be one issue inhibiting the growth of LTPS. Challenges for yield management tool providers include smaller design rules for LTPS, integrating full driver and array pixel test in a single tool, array test TACT, improved defect coverage, and OLED device test capability.

We recently surveyed a number of LTPS TFT LCD producers in Japan, Korea and Taiwan on what they believed the biggest challenges were in LTPS TFT LCD production. The results are summarized below:

1. Step with narrowest process window – ELA due to laser energy variations. High maintenance costs due to required weekly maintenance and short laser tube life were also mentioned as concerns. One company claimed they had overcome most of the problems with ELA.
2. ELA throughput and laser tube replacement – Answers ranged from 20 to 20-30 substrates per hour for ELA. Companies acknowledged the new JSW FLX Series throughput using SLS technology is as high as 40 substrates per hour and is well positioned for reaching mobility

levels of >300. ELA laser tube replacement is now every 4-5 months, improved from every 3 months.

3. Ion implant/ion shower – Challenges include uniformity, dopant/hydrogen control, throughput, cleanliness and eminence costs. Contaminants and dust from the chamber collecting on the substrate were listed as the most serious implant problem for two companies. Filament life is an issue for tools with a filament type of plasma source requiring one day's work for filament exchange one time per month. Tools with RF plasma source don't have this problem.
4. Dry strip – It may be necessary after high energy, high dose implants. Wet strip is still required however to guarantee surface cleanliness and completely remove impurity residue after ion doping/implant. Stencil masks also being examined in ion implant to eliminate coating/resist stripping requirement.
5. a-Si, gate dielectric and ILD layers. Current film quality is acceptable, but LTPS manufacturers are demanding better performance. One company indicated they would like to eliminate the dehydrogenation step by depositing an a-Si film with minimal hydrogen concentration. Another company indicated that although TEOS is acceptable at current frequencies, improvements in film quality will be necessary at >50 Hz. It was also indicated that ion damage in the CVD chamber is also a concern and V_{th} must be further lowered.
6. Yield management. We asked if testing the driver area and pixels separately was acceptable, and would a combined system be desired. One company indicated it does not inspect the array due to sufficient yield. According to this company, if pixel inspection is required, there is little likelihood that further integration can be pursued. Also, it was indicated complete testing of small/medium panels is not realistic. Another company indicated it is testing integrated driver circuitry only, that pixel testing is not feasible due to slow throughput and satisfactory pixel yields. Two companies indicated that an array/pixel tester would be valuable if throughput is sufficient as users will eventually demand no defects even on small panels and introduction of pixel inspection will be a must. For AMOLED backplanes, it was indicated that because V_{th} shift and current uniformity need to be more tightly controlled than in LTPS, pixel inspection would be used more frequently.
7. Current yields and how they would improve. A number of companies indicated that it isn't fair to compare integrated LTPS TFT LCDs with a-Si TFT LCDs as integrated LTPS TFT LCDs feature far more circuitry and the system specifications become additional yield factors such as power consumption. Another company indicated that its array yields for LTPS were quite similar to a-Si. Another company indicated that its yield fallout for transflective displays is not in the array process but in the cell process as transflective displays require half the cell gap of transmissive displays. It was also indicated that electrostatic discharge was one of the biggest sources of transistor yield loss generated by many different types of process and inspection equipment. Equipment, process conditions and circuit design must be optimized to minimize this problem. Humidity in the cleanroom is the most important contributor and must be minimized.
8. Could channel doping be eliminated to simplify the process? Two companies indicated channel doping could not be eliminated, one company indicated it could be eliminated in some cases, another company indicated it could be eliminated on one side of the channel if precision was improved. Another company indicated channel doping would become more critical in AMOLEDs due to more demanding V_{th} control requirements.
9. a-Si or LTPS as an AMOLED backplane technology. It was indicated that although a-Si offers better initial V_{th} uniformity, V_{th} shifts over time make a-Si inappropriate unless these shifts are compensated for, particularly in applications demanding high brightness, long lifetimes and large-area uniformity in products such as TVs. Current capacity is also an issue as is requirement of a top emission structure.
10. Integrating current drivers for AMOLEDs. A number of companies indicated it is possible with the concern being maintaining uniformity of each pixel by circuit and process improvements. One company developed a novel current driver circuit for each pixel which compensated for the TFT non-uniformity.

SUMMARY

LTPS TFT LCD demand is growing, particularly in mobile phones, digital cameras and other mobile applications as resolution and form factor requirements increase. Despite the positive outlook, there are still a number of production challenges. However, as a growing number of TFT LCD and equipment suppliers continue to pursue LTPS TFT LCDs, we believe these challenges will be overcome as significant improvements have already been realized.

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[1] Hiroyuki Ohshima, "Overview of LTPS Technology", IDMC 2003, p.11.
[2] Ibid., p.13.