Pentacene OTFTs with Al_2O_3 gate insulator by Atomic Layer Deposition Process

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Abstract

Pentacene OTFTs of Al_2O_3 insulator treated with a diluted PMMA were fabricated for the application of the low voltage operation and large area displays. The operation voltage of 15 V and the mobility of 0.35 $cm^2/Vsec$ are obtained even adopting the thick dielectric of 100 nm which was deposited by atomic layer deposition at the temperature of 150°C. The current on-off ratio was 4.1×10^4 for the OTFTs treated with 9:1 PMMA and good saturation characteristics were obtained as drain voltage increases.

1. Introduction

For the large-area displays such as active matrix organic light emitting diodes (AMOLEDs), active matrix liquid crystal displays (AMLCDs) and electronic paper displays, gate dielectric thickness of 100 nm or more are desirable for reliability and manufacturing yield consideration [1]. As for pentacene OTFTs with thick gate insulator over 100 nm, high operating voltage and surface roughness of gate insulator can be problematic issues because pentacene growth depends on surface energy of gate insulator. To obtain pentacene OTFTs with low operating voltage and high field effect mobility, high - k material by atomic layer deposition is preferable because an atomic layer deposition (ALD) process can guarantee an excellent uniformity of film thickness for the application which requires a large area and a thick film over 100 nm. Among various high-k materials [2], Al_2O_3 gate insulator by the ALD process was chosen for pentacene OTFTs because it has a high breakdown field, high dielectric constant of 9 and low deposition temperature of 150°C. In addition, a surface modification technique by a diluted PMMA was applied to improve the electrical performances of pentacene OTFTs due to the increased grain size of pentacene on Al_2O_3 gate insulator [3].

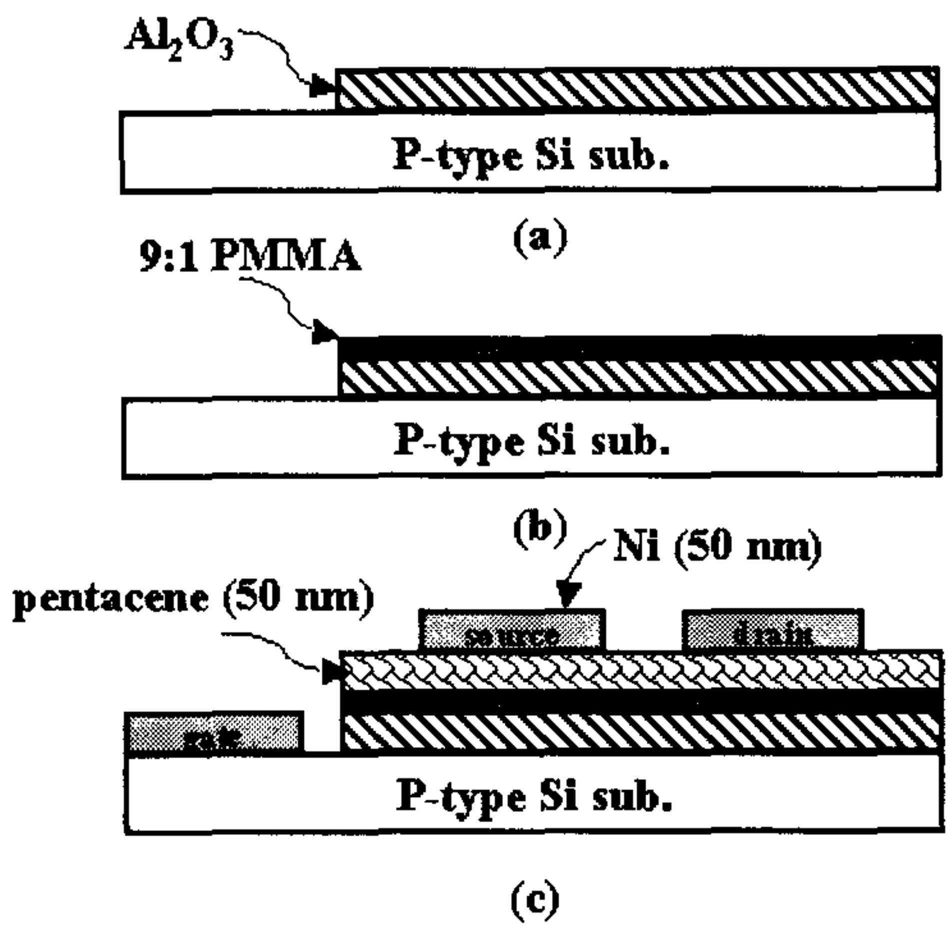


Fig. 1 Process sequences for the fabrication of OTFTs with Al_2O_3 insulator

2. Experiments

A starting substrate was chosen as p-type Si wafer. The dielectric layer of Al_2O_3 was deposited on p-type wafers by ALD process at the temperature of 150°C. The thickness of Al_2O_3 layer was split as 50 nm and 100 nm to investigate the dependency of operation voltage and gate leakage level on dielectric film thickness. As shown in Fig. 1(a), the Al_2O_3 layer was patterned by reactive ion (RIE) etching for the purpose of gate electrode contact. Fig. 1(b) shows that 9:1 PMMA was spin-coated on the Al_2O_3 layer to improve the growth of pentacene on the gate dielectric [3]. The 9:1 diluted PMMA indicates that the mixing ratio of monochlorobenzen to 1% PMMA is nine to one. And then, 50 nm pentacene was thermally evaporated on Al_2O_3 layer under the pressure of 10^{-7} torr at the substrate temperature of 80°C. Finally, 50 nm nickel was e-gun evaporated for the definition of source, drain and gate electrodes through a shadow mask. The channel width and length of OTFTs are 1000 μm and 30 μm, respectively. All electrical performances for fabricated OTFTs are measured by electrical parameter analyzer of HP 4150 in air.

3. Results and discussion

Figure 2 shows that the transfer characteristics of OTFTs with and without the 9:1 diluted PMMA layer on Al_2O_3 gate insulator. In view of electrical performances such as threshold voltage, current on-off ratio and sub-threshold slope, OTFTs with the 9:1 diluted PMMA treatment are similar to those of OTFTs without the surface treatment. Threshold voltages of OTFTs with and without the PMMA treatment were –2.5 V and –2 V, respectively. The current on-off ratio and the sub-threshold slope were about 4×10^4 and 1V/dec for OTFTs with and without the PMMA treatment, respectively. On the other hand, mobility of OTFTs with the diluted PMMA layer was improved as 0.35 $cm^2/Vsec$, which is 6 times larger than that of OTFTs without the diluted PMMA. The improvement of mobility for OTFTs results from the increase of a pentacene grain size after the surface modification by the PMMA coating as shown in Fig. 3. Figure 3 shows photograph images of pentacene grain grown on Al_2O_3 insulator before and after the 9:1 PMMA coating.

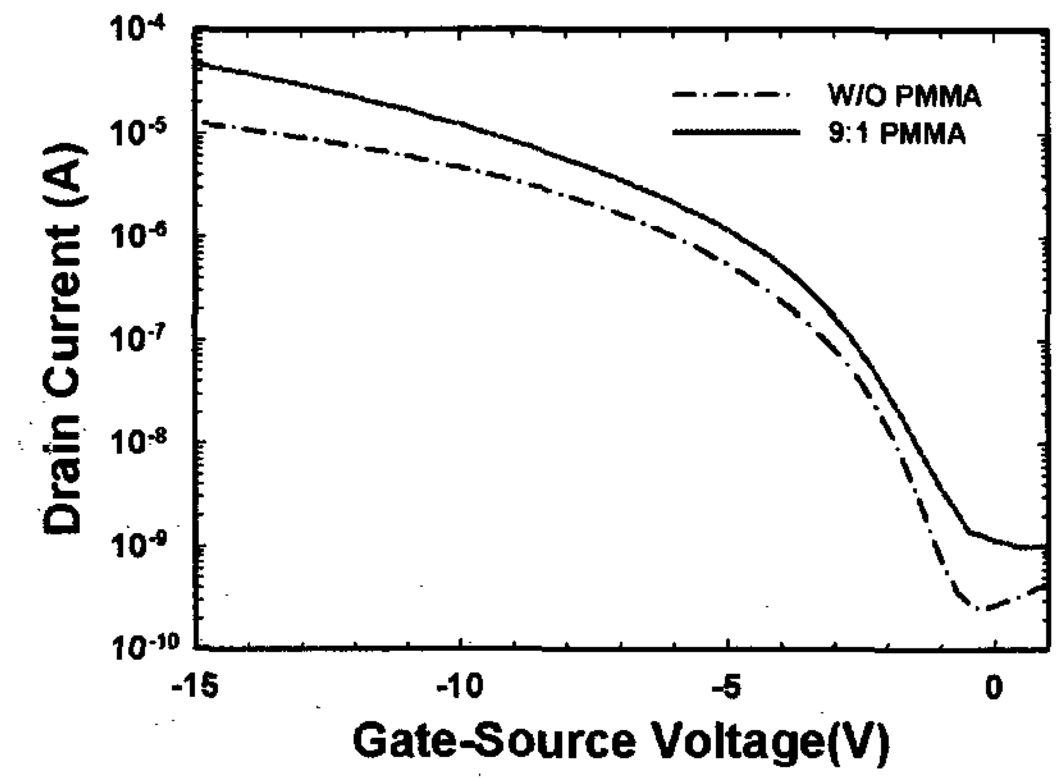
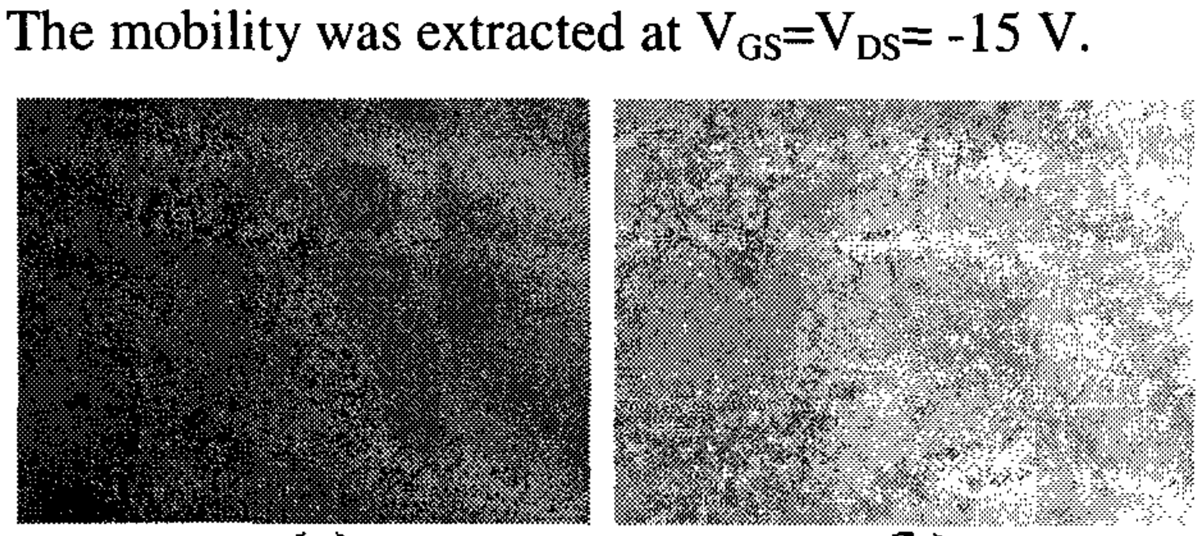
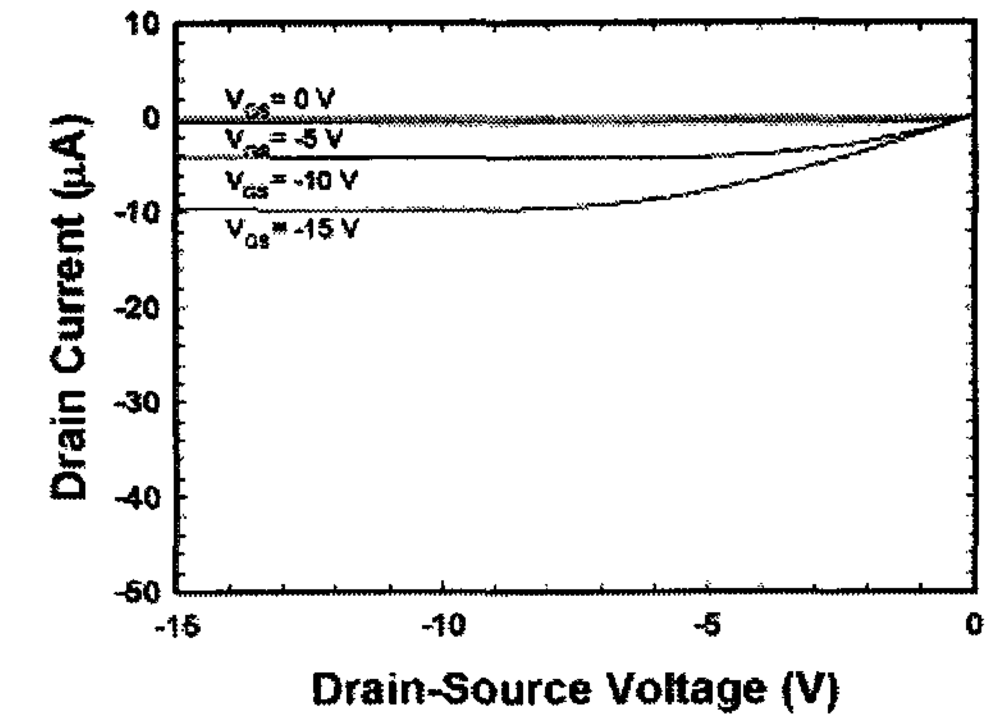


Fig. 2 Transfer characteristics of OTFTs with and without the PMMA on 100 nm Al_2O_3 gate insulator. The mobility was extracted at $V_{GS}=V_{DS}=$ -15 V.

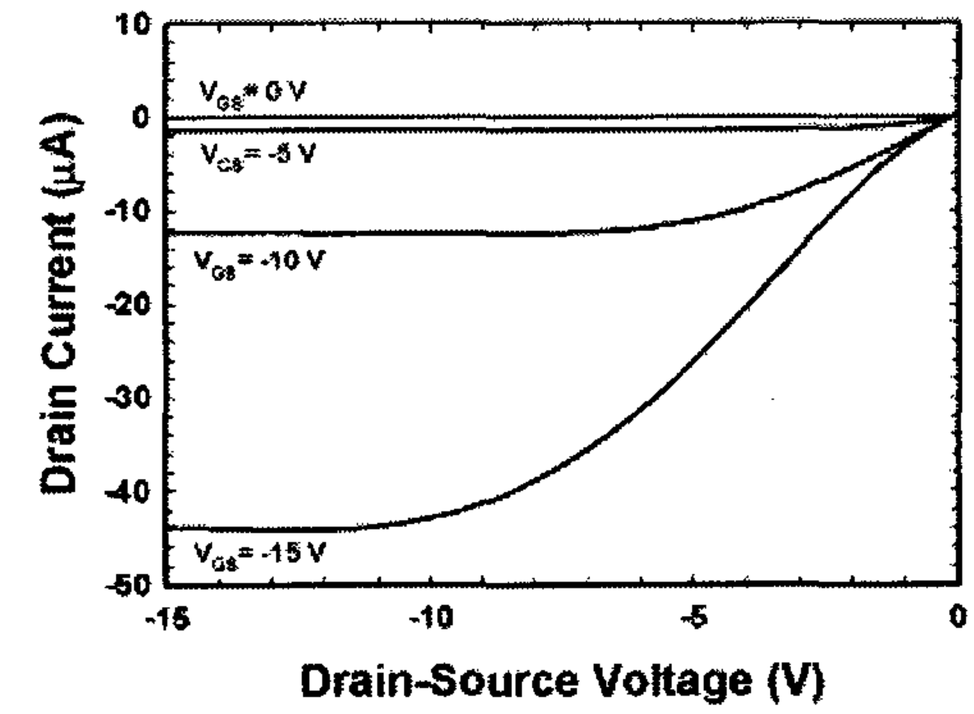


(a) (b)

Fig. 3 Photograph images of pentacene grown on 100 nm Al_2O_3 gate insulator (a) without and (b) with the diluted PMMA layer. The substrate temperature was maintained at the temperature of 80°C during pentacene deposition.



(a)



(b)

Fig. 4 Output characteristics of OTFTs (a) without and (b) with the PMMA on 100 nm Al_2O_3 gate insulator

Pentacene grain size after the PMMA treatment is about two times larger than that of pentacene before the PMMA treatment. The increase of pentacene grain size after the PMMA treatment is thought to be the decrease of surface energy on Al_2O_3 gate insulator, compared with that on Al_2O_3 before the PMMA treatment.

Figure 4 shows the output characteristics of OTFTs with 100-nm-thick Al_2O_3 gate insulators with and without the 9:1 PMMA layer. After the surface modification of gate insulators by the 9:1 PMMA layer, the saturation current level was increased from 10 μA to 42 μA at the bias conditions of V_{GS} (gate to source voltage) and V_{DS} (drain to source voltage) of -15 V. The increased saturation current was possibly due to the increase of a pentacene grain size after the surface treatment [4]. In addition, the saturation characteristics were very good over the range larger than V_{DS}=-10 V.

In order to investigate into the electrical performances of OTFTs depending on the thickness of Al_2O_3, OTFTs with 50-nm-thick Al_2O_3 dielectric were fabricated and characterized. Fig. 5 shows the transfer characteristics of OTFTs with 50-nm-thick Al_2O_3

insulator with and without the 9:1 PMMA treatment. After reducing Al_2O_3 insulator thickness from 100 nm to 50 nm, the range of operating voltage for OTFTs was reduced from 15 V to 10 V. But the drain current at the bias condition of V_{GS}=1 V as shown in Fig.2 and Fig. 5, was increased from 1nA to 100 nA even though OTFTs at the bias condition of V_{GS}=1V should be in the off-state. The result was attributed to the increase of gate leakage current due to the decrease of breakdown field. The breakdown field level of as-deposited Al_2O_3 insulator was lower than that of the annealed Al_2O_3 [2]. But the annealing process higher than 150°C was not desirable for the applications of OTFTs. Therefore the thickness of as-deposited Al_2O_3 should be larger than 100 nm for the OTFTs application in view of the uniformity of Al_2O_3 film thickness and the gate leakage current level. As shown in Fig. 5, the drain current level was also increased after the PMMA surface modification for OTFTs with

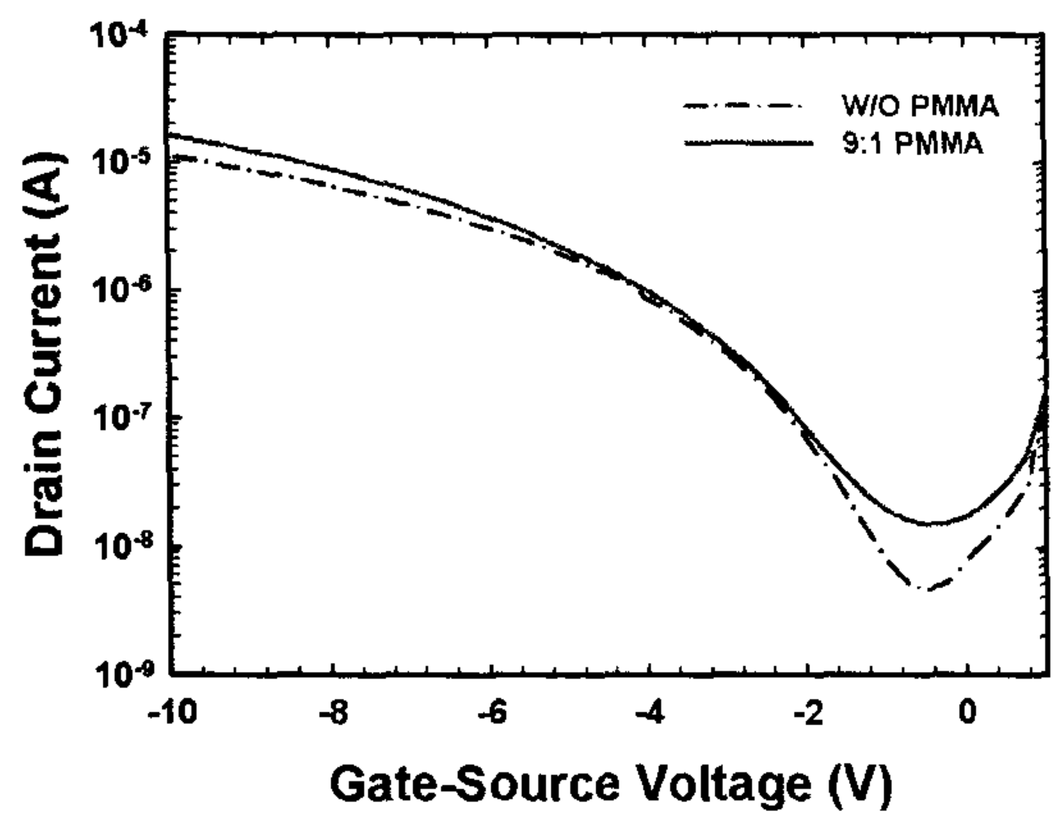
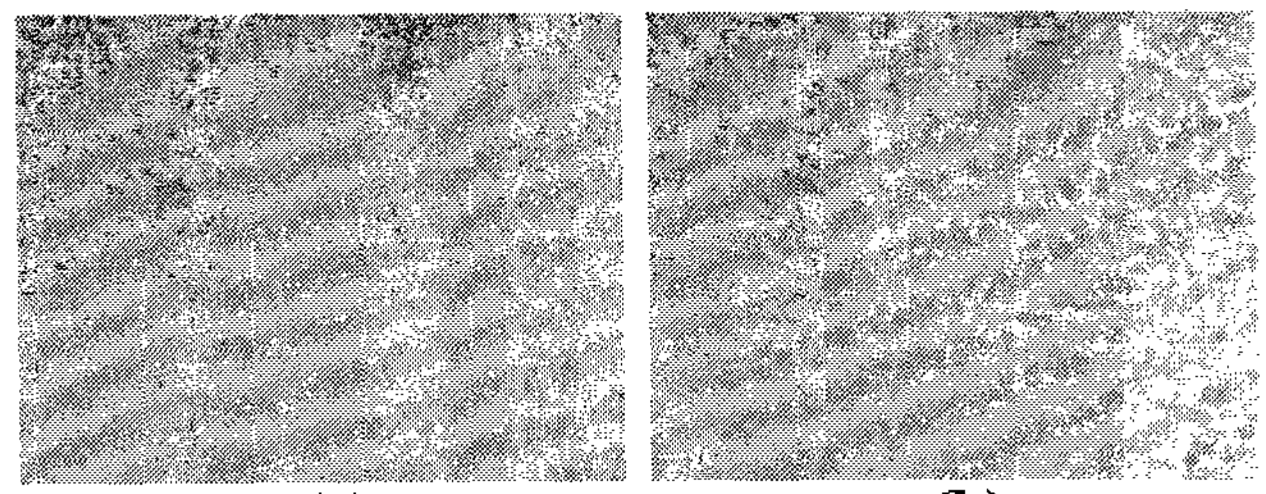


Fig. 5 Transfer characteristics of OTFTs with and without 9:1 PMMA on 50 nm Al_2O_3 gate insulator. The mobility was extracted at $V_{GS}=V_{DS}$= -10 V.

50-nm-thick Al_2O_3 insulator. The increased drain current at the same bias condition is attributed to the increased grain size of pentacene after the PMMA treatment. Electrical performances except mobility are similar for OTFTs with and without the diluted PMMA layer.

The mobility of OTFTs with 50 nm Al_2O_3 insulator without and with the PMMA layer was 0.061 $cm^2/Vsec$ and 0.104 $cm^2/Vsec$, respectively. The threshold voltage, current on-off ratio and sub-threshold slope were –1.5 V, 1×10^3 and 1.5V/dec for the OTFTs with and without the PMMA layer, respectively.



(a) (b)

Fig. 6 Photograph images of pentacene grown on 50 – nm thick Al_2O_3 gate insulator (a) without and (b) with the diluted PMMA layer. The substrate temperature was maintained at the temperature of 80°C during pentacene deposition

Figure 6 shows the photograph images for pentacene grains grown on 50 nm-thick Al_2O_3 (a)without and (b) with the PMMA treatment. After the PMMA treatment, the grain size of pentacene as shown in Fig. 6(b) was increased up to about 1.5 times as large as pentacene grain size before the PMMA treatment as shown in Fig.6 (a).

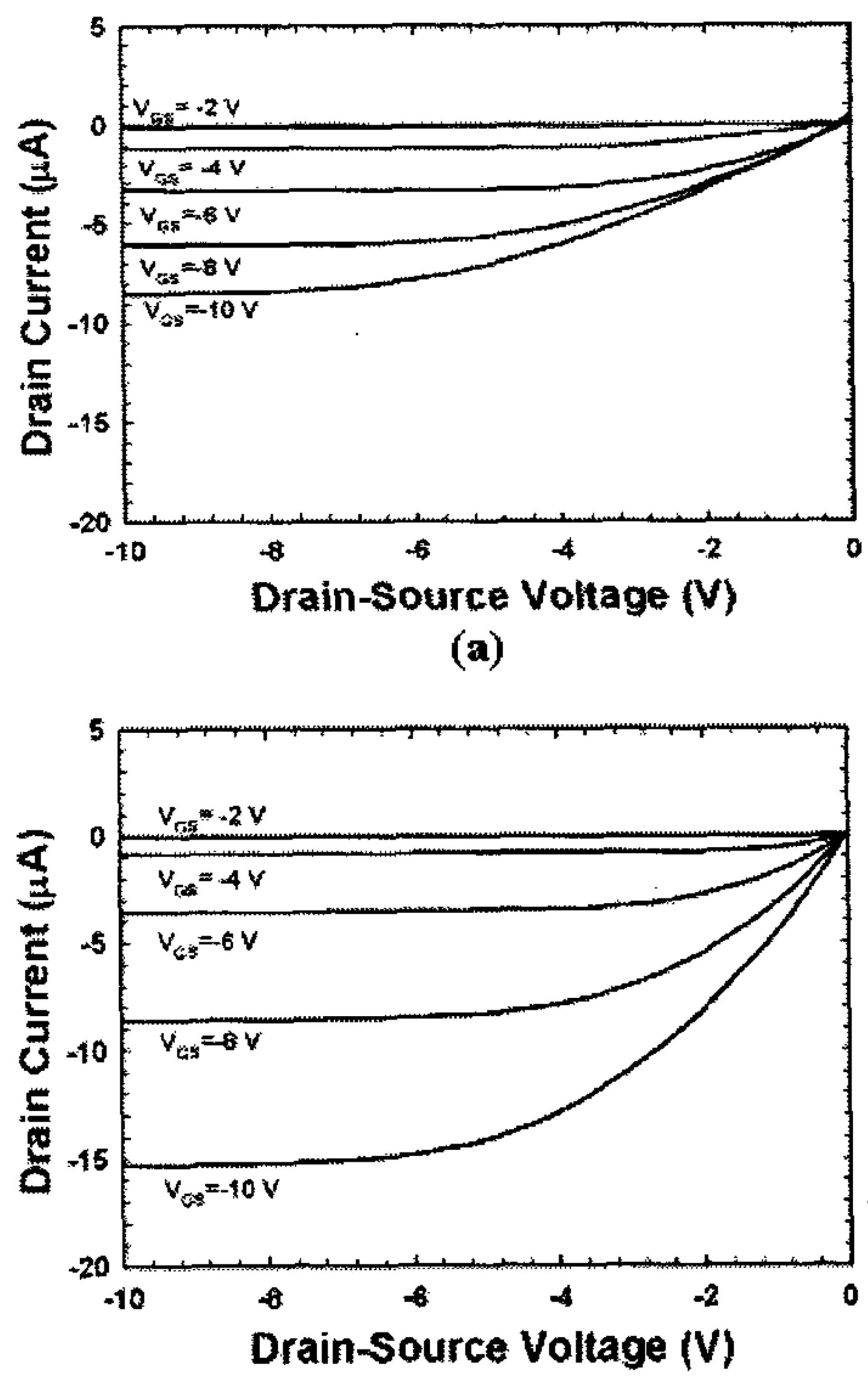


Fig. 7 Output characteristics of OTFTs (a) with and (b) without the 9:1 PMMA on 100 nm Al_2O_3 gate insulator

When it comes to the OTFTs with 50-nm and 100-nm thick Al_2O_3 insulator, the level of current improvement for OTFTs with 50 nm Al_2O_3 was lower than that of OTFTs with 100 nm because the improvement level of OTFTs with 50 nm Al_2O_3 in pentacene grain size was lower than that of OTFTs with 100 nm Al_2O_3 insulator. The different level of improvement in pentacene grain growth was possibly due to the difference of roughness for Al_2O_3 gate insulators.
Figure 7 shows the output characteristics of OTFTs with 50-nm-thick Al_2O_3 with and without the PMMA treatment. After the PMMA treatment, the saturation current level at the bias conditions of $V_{GS}=V_{DS}=-10$ V was increased from −8.5 μA to -15 μA. The improvement was due to the increased pentacene grain size after the PMMA treatment.

4. Conclusion

Al_2O_3 insulator by ALD process was applied to pentacene OTFTs for the low operating voltage, high performances and low temperature process below 150°C. The thickness of Al_2O_3 over 100 nm is appropriate for the applications of OTFTs because of gate leakage current. The mobility of OTFTs after the PMMA treatment was 2~5 times larger than that without the PMMA treatment. However, other electrical performances such as threshold voltage, current on-off ratio, and sub-threshold slope are similar for both OTFTs with and without the PMMA treatment. As for ALD process, there is no obstacle for the large area application. Therefore, ALD process can be applied to the gate insulator deposition for high performance OTFTs, which require large area application, low surface roughness, thick thickness over 100 nm of gate insulator, and low deposition temperature under 150°C.

5. References

[1] Christos D. Dimitrakopoulos and Patrick R. L. Malenfant," Organic Thin Film Transistors for Large Area Electronics," Adv. Mater., no. 2, pp. 99-117, 2002.

[2] G. D. Wilk, R. M. Wallace and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," J. Appl. Phys., vol. 89, no. 10, pp. 5243-5273, 2002.

[3] Sung Hun Jin, Jin Wook Kim, Jae-Sung Yu, Cheon An Lee, Byung-Gook Park and Jong Duk Lee, "Surface State Modification of a Gate Insulator by a Diluted PMMA Solution And Its Application to Pentacene OTFTs," The 10th Korean Conference on Semiconductors, Seoul, Korea, pp. 485-486, Feb. 27-28, 2003.

[4] D. Knipp, R. A. Street, A. Volkel, and J. Ho, "pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport, " J. App. Phys. , vol. 93, no. 1, pp. 347-355, 2003.