A new driving circuit for the low power and reduced layout area in silicon based AM-OELDs

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Abstract

A silicon based OELD driving circuit that has a new type of column driving method is proposed to reduce the driving circuit area. In comparison with the conventional method, latches in each column are removed and one DAC (digital-to-analog converter) drives several column lines. To make the DAC operate during a specific period for the low power consumption, a simple DESG (DAC Enable Signal Generator) circuit was devised and confirmed by the simulation.

1. Introduction

As a microdisplay application, the silicon based top emission organic electroluminescent display (OELD) has much potential and many researchers have been interested in this topic [1-4].

Many silicon based OELD driving circuits adopt the conventional scheme as shown in Fig. 1, which is composed of the shift register, latches, DACs in each column [2-4]. However, it is not considered to be a good method for the active matrix (AM) type microdisplay because it consumes large driving circuit area due to 8-bit latches and 8-bit DACs at every column line to implement 256 gray scales.

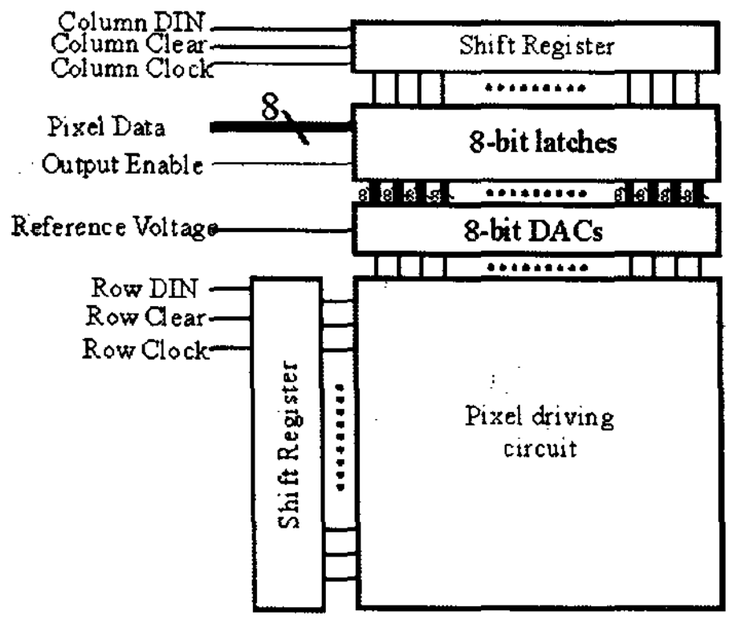


Figure 1 The conventional driving circuit diagram

for the silicon based AM-OELD.

In this work, we have proposed a driving circuit with a new type of a column driving method to reduce the driving circuit area for the silicon based OELD.

2. Circuit design

2.1 The system overview

A new type of driving circuit shown in Fig. 2 was proposed. In comparison with the conventional one, the 8-bit latches at each column are removed, and the simple analog CMOS switches are added to the DAC output. Also, an 8-bit DAC circuit is not located in each column line and it drives several column lines. These techniques help to reduce the layout area that is occupied by the column driving circuit. Although the removal of the latch means the reduction of the pixel charging time, it does not matter because the DAC implemented using the CMOS logic has sufficiently high speed.

Figure 2 The block diagram of the proposed driving circuit.

2.2 Design of circuit blocks

The shift register in the row and column driving circuit as shown in Fig. 2 is composed of MSM (master-slave-master) type D flip-flops (D-F/F) shown in Fig. 3. This D-F/F has an additional master latch block, compared with the conventional pseudo-static flip-flop [2].

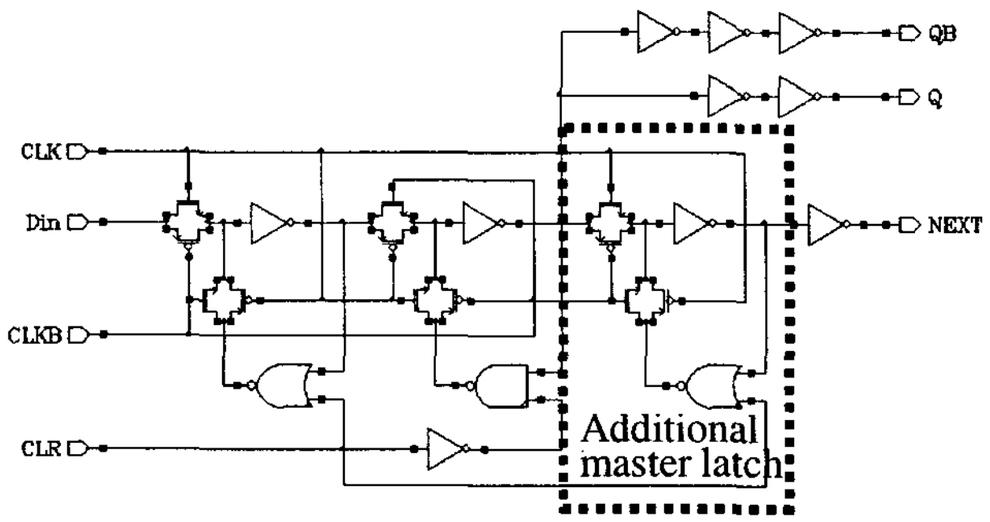


Figure 3 The MSM(master-slave-master) type D flip-flop which comprises the shift register in the row and column driving circuit.

Fig. 4 shows the timing diagram of the MSM D-F/F. The additional master latch generates the 'NEXT' signal that is the delayed signal during half-clock period of the 'Q' signal. This 'NEXT' signal is connected to the input terminal('Din') of the next D-F/F stage, and it offers maximum signal margin(setup time and hold time) to the rising edge of the 'CLK' signal and the 'Din' signal of the next stage. In other words, it can enhance the operational reliability of the shift register, especially when the chain of the D-F/F in the shift register becomes longer.

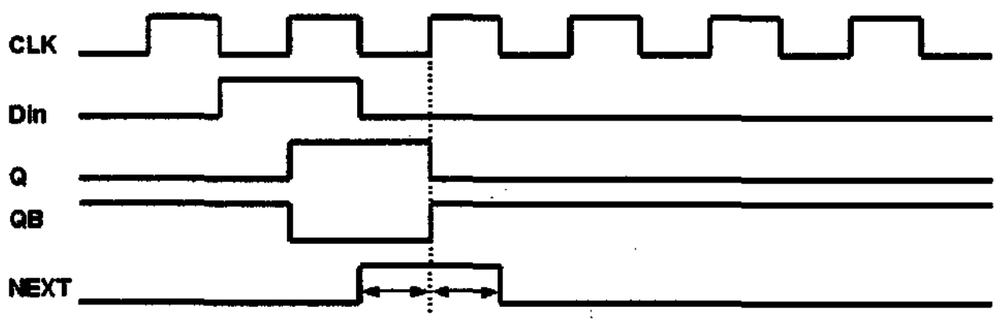
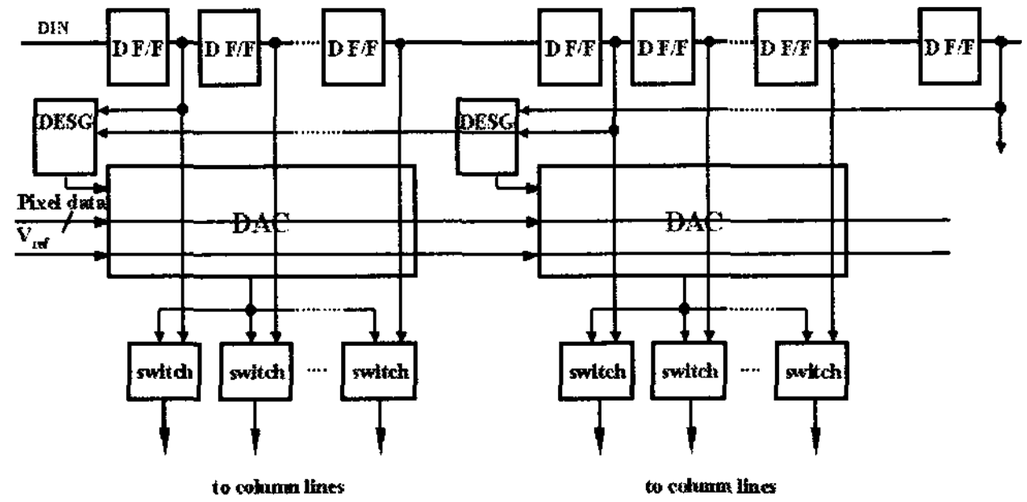


Figure 4 The timing diagram of the MSM D-F/F.

Fig. 5 shows a more detailed block diagram of the column driving circuit. 8-bit pixel data are supplied to all DACs, and they enter each column line by the switching operation of the shift register and switches after being converted to the analog signals.

Fig. 6 shows the transistor level schematic diagram of the DAC circuit. It is a current mode DAC that is implemented by PMOSFETs. The DAC output 'DO' is connected to the column data line after passing through the CMOS switch that is controlled by the shift register output. The pull-down NMOS 'N_{PD}' is necessary to form a current mirror with the driving transistor of the conventional voltage programming pixel circuit [2].



※ DESG : DAC Enable Signal Generator circuit block

Figure 5 Detailed block diagram of the column driving circuit.

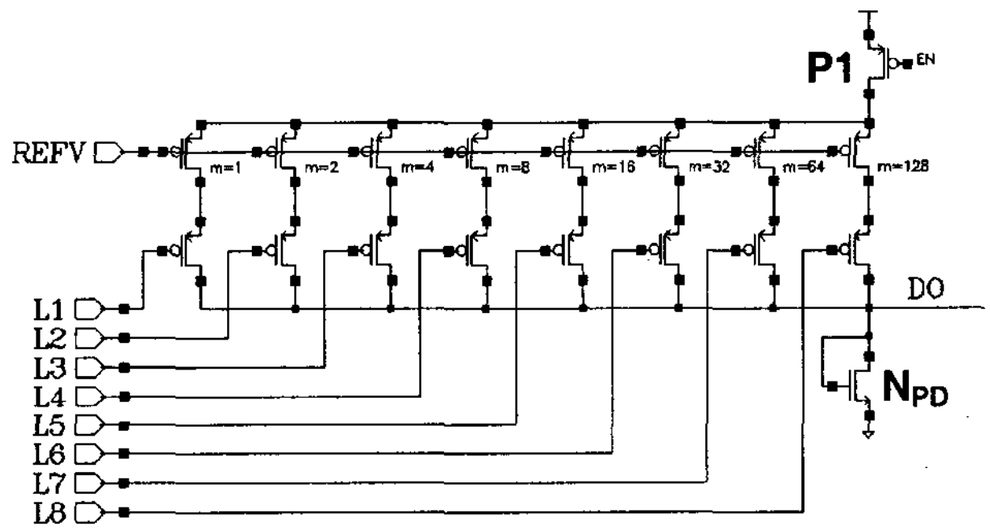


Figure 6 The current mode DAC circuit in the column circuit.

This current mirror structure has two merits. 1) it guarantees the pixel current to be linear, although the organic EL devices at each pixel have non-linear and non-uniform I-V characteristics, because the current linearity of the DAC circuit is copied to the driving transistor. 2) the DAC circuit can drive the large capacitive load of the column line because the DAC current can be copied to the pixel in the reduced scale. Fig. 7 shows the simulated pixel current when the digital pixel input data increase continuously.

But, at a specific time, only one DAC actually provides the corresponding column lines with the analog pixel data. Furthermore, the DAC consumes standby power that is generated by the current flow through the pull-down NMOS (N_{PD}) during the non-operating period. To prevent this useless power consumption, a large PMOS (P1) that is controlled by

the DAC enable signal is used in order to carry out the switching operation at the current source path.

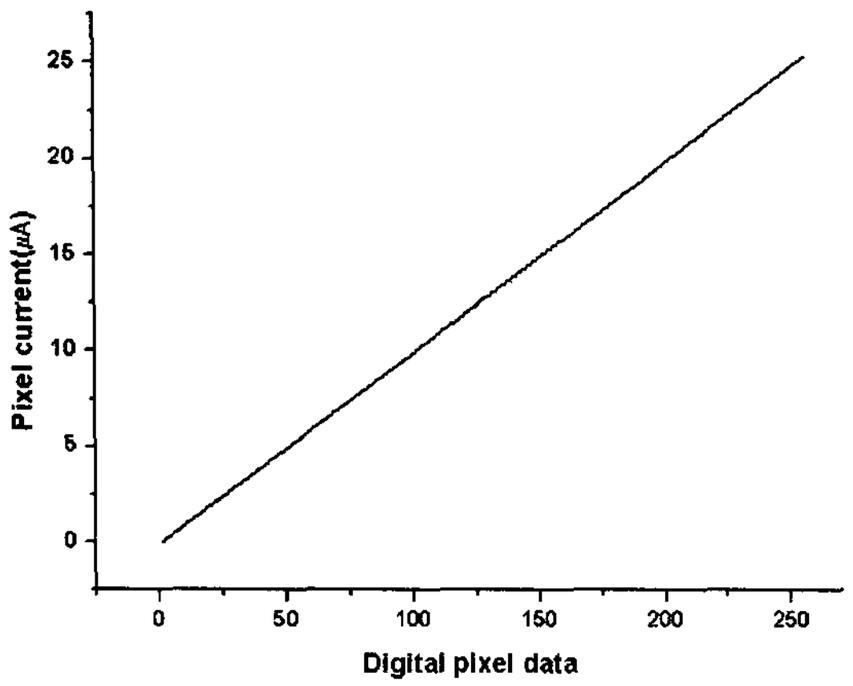


Figure 7 The simulated pixel current when the digital pixel data increase continuously.

Fig. 8 shows the schematic diagram of the DESG (DAC enable signal generator) circuit. This circuit plays an important role of making the DAC operate only at the corresponding time. Since the shift register output signal to select a column line does not enter in a random manner, but in a sequential manner, we can implement the DESG very simply.

The first D F/F output signal of a DAC ('CENB') and that of the next DAC ('CEN') can change the state of the latch by pulling up P2 or pulling down N2. Since the fighting condition between P2, N2, I1, I2 can occur, the sizes of these devices should be carefully designed. The 1-bit latch holds the current state except the rising edge of 'CEN', 'CENB'. The output buffer drives the large size PMOS, P1. This DESG circuit has a very simple structure and becomes much more effective when one DAC drives more and more columns.

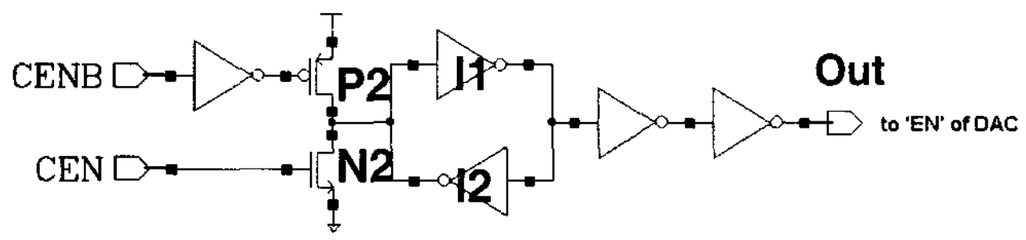


Figure 8 The DAC enable signal generator (DESG) circuit. It is composed of pull down NMOS, pull up PMOS, 1-bit latch, and buffer.

Fig. 9 shows the simulated result of the DESG block. An active LOW signal appears during the period between the rising edge of 'CENB' and the rising edge of 'CEN'.

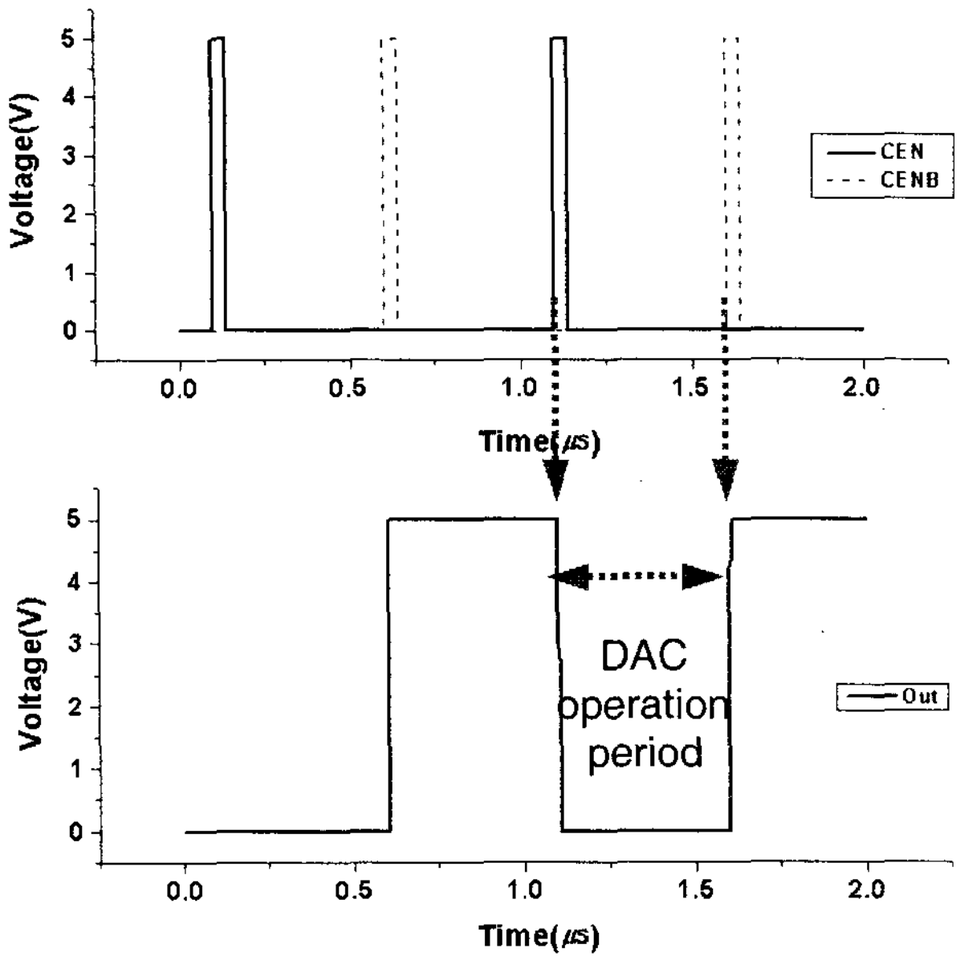


Figure 9 The simulated data of the DESG block at 25 MHz.

2.3 The driving circuit for the microdisplay

Combining the design techniques described thus far, we designed a driving circuit for the silicon based OELD which has 160×113 pixels. Fig. 10 shows the HSPICE simulation result of the whole driving circuit in the reduced time scale and reduced pixel number considering the extra parts of the circuit as an equivalent capacitance load. When the decreasing digital pixel data is supplied in turn, the corresponding pixel current flows through the organic EL device in each pixel.

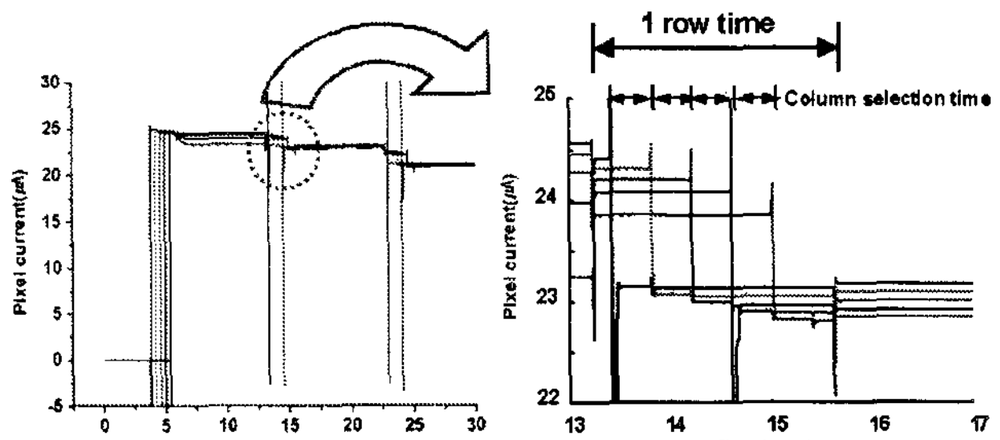


Figure 10 The simulated result of the pixel current of the selected row line.

Fig. 11 shows the layout of the driving circuit using a 1.5 μm 1-poly 2-metal standard CMOS process in the 1.3 cm × 1.0 cm area. It shows the layout area occupied by the column circuit is not large.

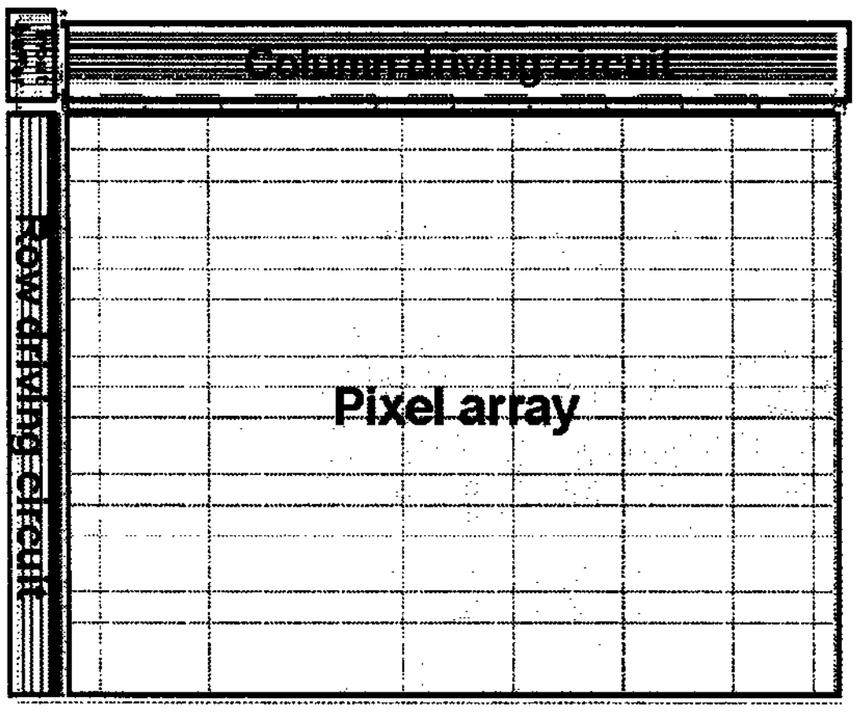


Fig. 11. The layout of the driving circuit for the silicon based OELD using a 1.5 μm 1-poly 2-metal standard CMOS process.

3. Conclusion

A new driving circuit for the silicon based AM-OELD is proposed. To be appropriate to the microdisplay, the layout area occupied by the driving circuit is reduced by means of removing 8-bit latches and reducing the number of DACs. Also, by devising a simple DAC enable signal generator, it becomes possible to turn off the DAC circuit when it does not drive column line actually. Consequently, the standby power consumed by the DAC can be reduced.

4. Acknowledgements

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5. References

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