An Implementation of Highly Integrated Signal Processing IC for HDTV

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ABSTRACT

This paper presents a signal processing IC for digital HDTV, which is designed to operate in built-in HDTV or in HD-set-top Box. The chip supports de-multiplexing an ISO/IEC 13818-1 MPEG-2 TS stream. It decodes MPEG-2 MP@HL video bitstream, and provides high-quality scaled video for display on HDTV monitor. The chip consists of ARM7TDMI for TS-Demux, PCI interface, Audio interface, MPEG2 MP@HL video decoder, Display processor, Graphic processor, Memory controller, Audio interface, Smart Card interface and UART. It is fabricated using Samsung's 0.18-um, and the package of 492-pin BGA is used.

1. Introduction

Since all broadcasting companies have put HD programs on the air, the market of digital TV is being lately matured. Therefore, the productions of digital contents that pursue the commercial success are getting increased [1][2].

We have designed and implemented a single chip HDTV decoder that is a core component for DTV. This chip would improve the performance and reduce the price of core components. Furthermore, it is expected to help DTV market to be more grown. The chip supports ISO/IEC 13818-2 MPEG2 MP@HL video decoding including ATSC 18 video formats, and de-multiplexing of ATSC MPEG2 TS stream. It also displays graphics and high-quality scaled video on an HDTV display device.

In section 2, the system level architecture of the HDTV signal processing IC is described. The section 3 is devoted to internal sub-system architecture and sub-system's functions. The section 4 describes the implementation. Finally, conclusion is made in section 5.

2. System Architecture

There are five major interfaces in this chip: digital base-band signal from the tuner, host interface, memory interface, conditional access and display. As shown in Figure 1, HDTV signal processing IC interfaces with the other blocks on the system level.

This chip can accept the base-band signal of either DIRECTV from satellite or ATSC. It also processes conditional access through Smart Card and AV chip interface.

It supports the transaction of various video formats such as frame rate, color space conversion, and video scaling after video signal is decoded.

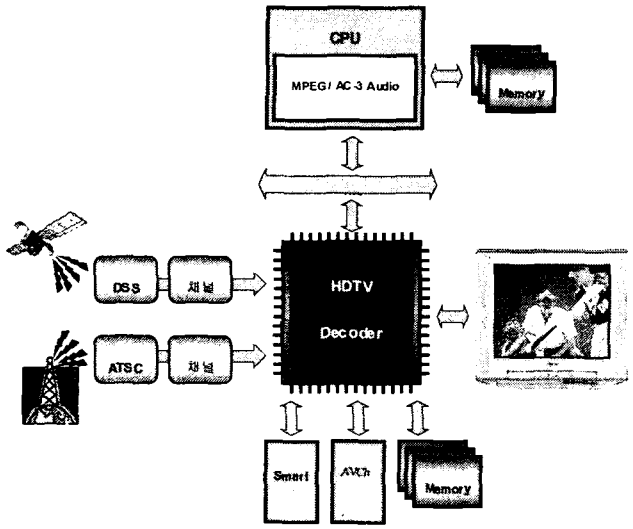

Figure 1. System Block Diagram

3. Internal Sub-system

The internal block diagram of the architecture for the highly integrated HDTV signal processing IC is shown in Figure 2. It consists of five major sub-systems: TS-Demux, PCI interface, MPEG2 Video Decoder, Display Processor, and MMU.

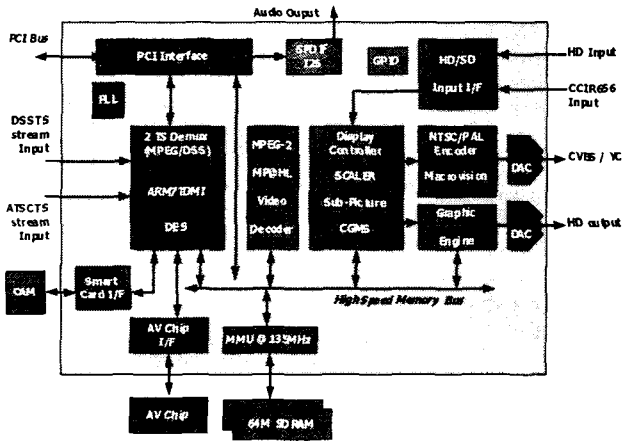

Figure 2. Internal Block Diagram

3.1 TS-Demux

TS-Demux engine contains 32-bit RISC Processor ARM7TDMI capable of parsing multiple transport formats: ISO/IEC 13818-1, DIRECTV/DSS. PSIP TS packets and A/V TS packets are analyzed and processed by the software of ARM7TDMI. In the TS-Demux engine, PSI sections are filtered and sent to external host through PCI bus. Video packet is sent to external SDRAM decoding buffer, but Audio packet is sent to host memory. TS-Demux Engine also has DES circuit for de-scrambling of a scrambled TS input, Clock Recovery circuit for PCR, program clock recovery, and external VCOX controlled by using PWM.

3.2 PCI

This chip has PCI bus interface compliant with 2.1 specifications. It supports multiple interrupts for providing interrupt-handling programming, and operates fairness or priority arbitration of master module's requests for PCI memory. The PCI connects a chain-structure of internal registers used in each module. Global status register is used in DMA operation monitoring and target module error handling.

3.3 MPEG2 Video Decoder

The MPEG2 MP@HL video decoder consists of syntax processor and video processor. Figure 3 illustrates the block diagram of MPEG2 video decoder.

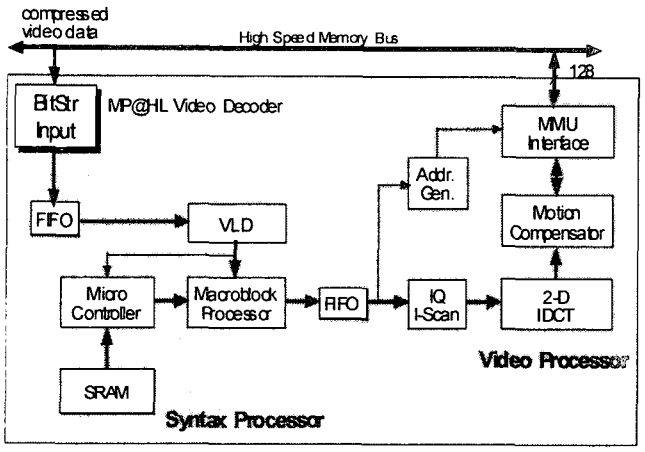

Figure 3. Block Diagram of MPEG2 video decoder

Syntax Processor has two major functions. First, it parses the elementary video stream to extract the parameters such as header information, motion vector, zero run-length, DC/AC coefficients etc. The extracted information is transferred to the other block. Second, Syntax Processor executes control instructions such as skip/repeat frame, some header scanning/blocking, 3:2 pull-down, and decoding/display timing control. Video Processor is composed of de-quantization (DQ), inverse discrete cosine transform (IDCT), motion compensation (MC). It supports all DTV (18 format) and DSS HD format decoding and operates MPEG-1/2 video decoding and horizontal down-scale decoding.

3.4 Display Processor

Display processor operates the normal-display mode and multiple-display mode including picture-in-picture (PIP) display and side-by-side display. Figure 4 shows a typical display of PIP and side-by-side. The display processor supports 4 independent planes: background, video, graphic, and cursor. They are mixed and displayed in real-time. Graphic plane is used for captioning, program guides, or other data services. In the graphics plane, the per-pixel alpha channel is used to determine the opacity of the graphics overlay at every sample point. It also supports three kinds of output formats: analog HD video output, digital HD video output and analog SD video output.

The brief features of display processor are listed below:

- Letter box / Pan-scan display
- Pillar-box(side-wall) / panorama display
- Flexible video scaling
- 3-D IPC for 480i video
- Flexible color space conversion
- High quality up-conversion and down-conversion of source video to selected display format.

(a) PIP (b) Side-by-Side

Figure 4. PIP/Side-by-Side typical display

3.5 Memory Controller

This chip has a highly optimized SDRAM memory interface. It supports multiple memory configuration (x4,x2 mode), and efficient arbitration of real time and non-real-time service.

4. Implementation

The chip is fabricated using Samsung's 0.18-um, and the package of 492-pin BGA is used. Figure 5 shows the chip's layout.

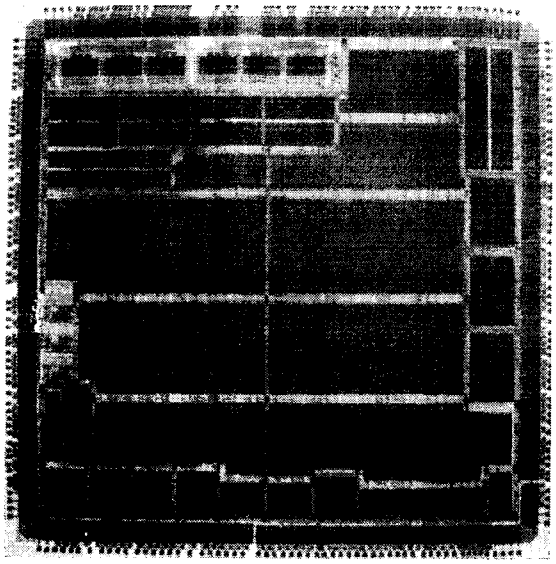

Figure 5. Chip Layout

5. Conclusion

In this paper, we have presented brief features of a single chip HDTV signal processing IC for built-in HDTV or HD-set-top Box. This chip integrates all the necessary functions for HD video decoding into a single chip and its compactness would allow for simple DTV set design. Figure 5 shows the layout of

References

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