# Satellite EOS(Electronic optical system) CCD(charge coupled device) detector control driver module design

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**Abstract:** The CCD (Charge coupled device) detector that is used to convert the light into electronic data is very important component in satellite camera. A Linear CCD Spectral detector shall be used in the MSC (Multi-Spectral Camera, to obtain data for high-resolution images) Payload. In this paper, the design concept of the CCD detector control module in the MSC CEU (Camera electronic unit) system which will be a payload on KOMPSAT is described in terms of H/W (clock speed and accuracy).

## 1. Introduction

The detector consists of 3 parallel arrays in the MSC. Each array consists of 5200 active elements with 32 TDI stages. The number of TDI stages is externally selectable in predefined stages. This control module shall be included in the FPE (Focal Plane Electronics) of CEU. The FPE board receives operating voltages from an external source. The FPE board supplies voltages (required power) as well as clocks (timing) to the CCD detector. Precise timing is supplied to the detector to ensure optimal operation in each operational mode.

## 2. EOS system

The EOS consists of two Electro-optical channels: Panchromatic (PAN) and Multi-Spectral (MS) sharing the same mirror telescope. Both channels can perform imaging at synchronous rate (nominal ground scan speed of ~6800 m/s). The EOS shall cover a swath width of 15km from an altitude of 685 km. The PAN channel has 15,000 active pixels of 1m ground resolution. Fig.1 is EOS block diagram.

The incoming light is converted to electronic analog signals by the detectors in the DFPA. The analog signals are amplified, biased and converted into digital signals (pixel data stream) in the FPE.

The digital data is transmitted to the Payload Management Unit (PMU) for pre-processing to correct for non-uniformity, to partially reorder the pixel stream (in the MS channel only) and to add header data for identification and synchronization.

The EOS is slave to the PMU and fully controlled by the PMU. The EOS receives the required power supplies from the Power Supply Module (PSM) of the PMU. The EOS is continuously thermally controlled by the THTM module of the PMU.

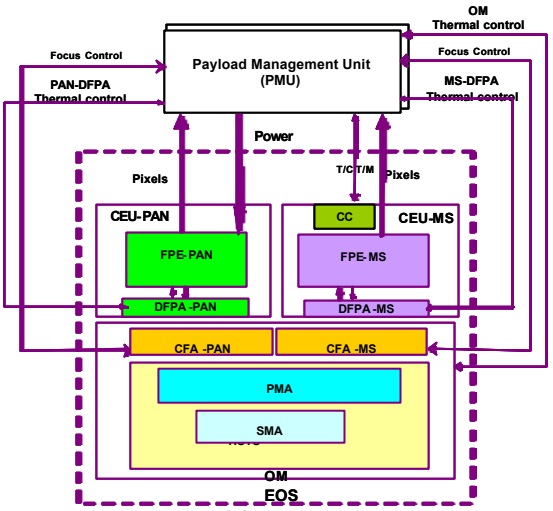


Fig.1 EOS Block diagram.

## 3. FPE system

The FPE assembly shall support the detector with the required power and timing. It shall process the analog signals, which come out of the detector and convert them to digital form. The FPE assembly shall consist of a single detector, up to twelve video channels, clock drivers, voltage regulators and control lines.

The fig.2 is the detector block diagram. The Detector is a Linear CCD Spectral detector. The Spectral separation is achieved by a customer supplied Spectral Input Window attached on the case. The detector consists of 3 parallel arrays. Each array consists of 5200 active elements with 32 TDI stages. The number of TDI stages is externally selectable in predefined stages. Electro-optical testing of the detector shall be carried out with a Clear input Window, for both options (PAN & MS).

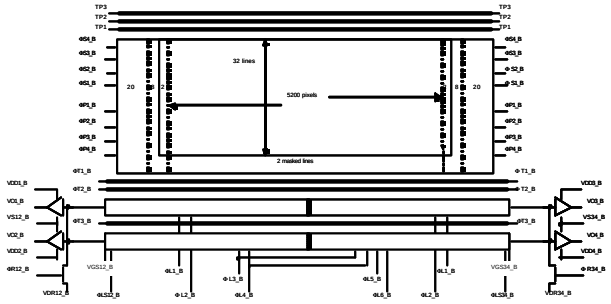

**Fig.2 Detector array block diagram**

The Fig.3 is the CEU PAN block diagram. As the fig.3, the FPE assembly shall be supplied the power and serial command from the CC (Camera controller). It shall process the analog signals which come out of the detector and convert them to digital video data format. In PAN channel, the two sides (primary and redundancy) FPEs control each of the detector bands. In the fig.3, the detector has 3 bands, the one is primary, another is redundancy, the other is not used.

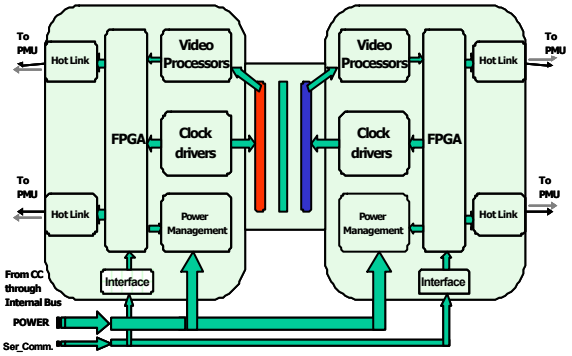


**Fig.3 CEU PAN block diagram**

## 4. Design of Clock Driver

The development of the FPE will be based on advanced design methods and tools, and will make use of novel advanced components and technology (authorized for spaceborne use), in order to reduce size, power consumption and weight and enhance performances. The FPE shall be designed to operate in IMAGING mode with up to 20% duty cycle per orbit; i.e. of up to 20 minutes during a 100 minutes orbit period.

The FPE needs the high reliability and low power consumption same as other satellite system, supplies exact clock signal to the CCD detector for the accurate control. The clock signals are PR, PT, PLS, PL, PP, PS, TP2, TP3 those control the CCD detector. The high speed clocks (PR, PT, PLS, PL) use the 'MAC0401' for converting analog signal to digital signal. The other signals (PP, PS, TP2, TP3) use the analog switch component (HS-303RH).

In this paper, the high speed clock driver circuit (PL, PLS, PR) is described. The fig.4 is pixel timing diagram for PL, PLS, PR. It has 11 MHz pixel rate(8,000 lines/sec).

Tr/Tf(ΦLi) = 0.2*(1/Fpixel) to 0.25*(1/Fpixel)
Tr/Tf(ΦLSij) = Tr/Tf(ΦRij) = 0.05*(1/Fpixel) to 0.1*(1/Fpixel)

The fig.5 is the clock driver circuit for PL, the fig.6 is the clock driver circuit for PLS and PR.

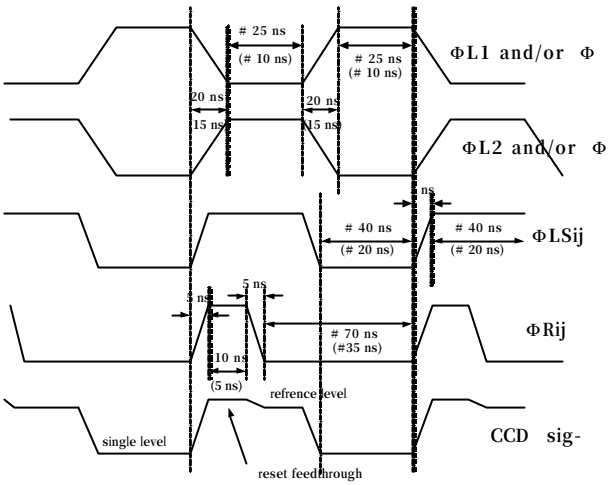


**Fig.4 Pixel Timing Diagram**

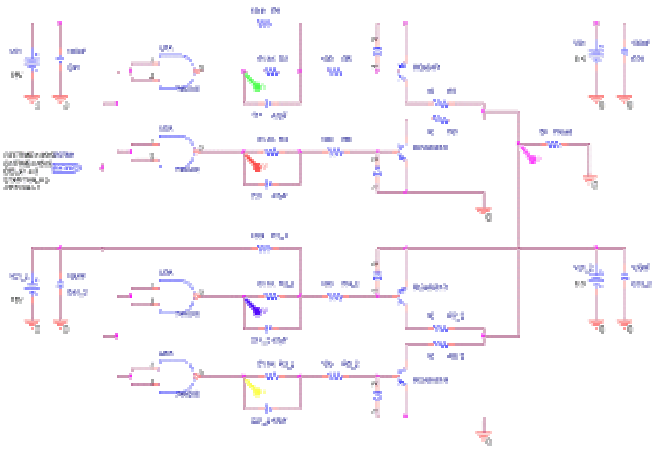

**Fig.5 PL clock driver circuit**

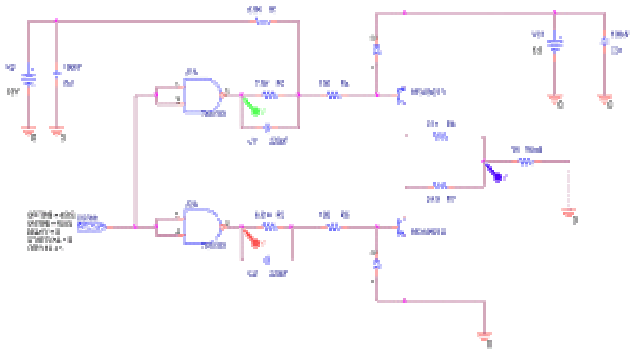

**Fig.6 PLS and PR clock driver circuit**

The sharpness for clock signal in the fig.7 and the fig.8 is decided that resistance and capacitance value in the fig.5 and the fig.6 same as the fig.3 timing diagram.

The fig.7 is the result of the simulation for resistance and capacitance. (R=7.5K, C=220pF)

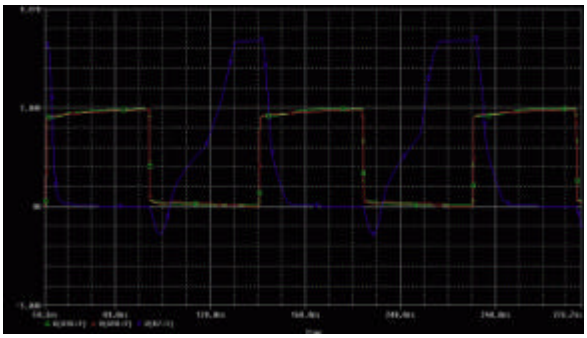

**Fig.7 simulation result (R=7.5K, C = 220pF)**

The fig.8 is the result of the simulation for resistance and capacitance. (R=7.5K, C=100pF)

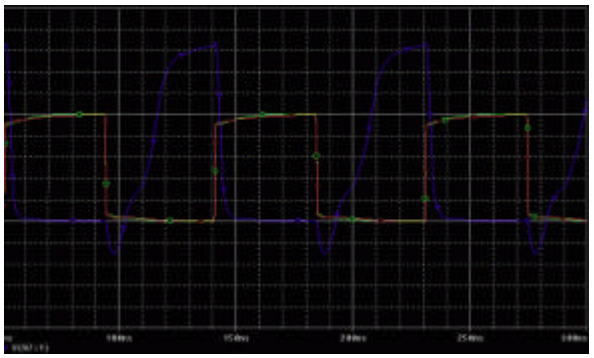

**Fig.8 simulation result (R=7.5K, C=100pF)**

As the results of fig.7 and fig.8, the sharpness of timing diagram is changed by capacitance value.

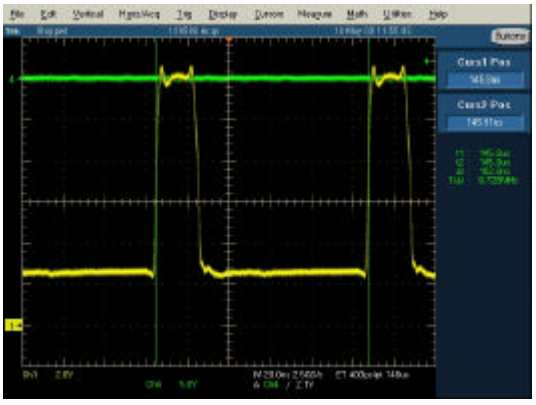

**Fig.9 FPE PAN R34 clock signal.**

From the fig.9 to the fig.11, these signals are the real signals captured by scope in this paper. These signals control and receive the video data from the CCD detector.

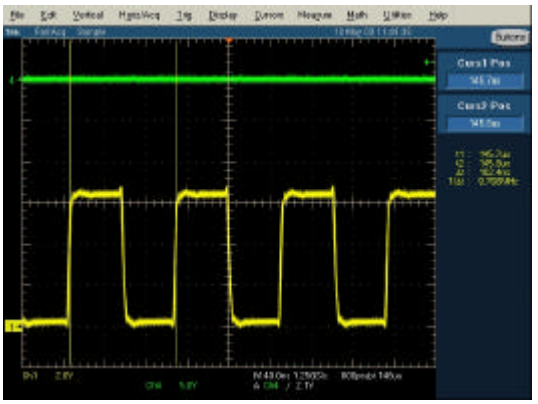

**Fig.10 FPE PAN LS34 clock signal**

**Fig.11 FPE PAN L4 clock signal**

## 5. Conclusions

In this paper, the design concept of a CCD detector control module which is described in terms of H/W (clock speed and accuracy supplied to detector). The exact and sharp control clocks will get the accurate and efficient analog video signal from detector. Also the MSC is intended to be a small lightweight camera. The development of the FPE will be based on advanced design methods and tools, and will make use of novel advanced components and technology (authorized for spaceborne use), in order to reduce size, power consumption and weight and enhance performance

## References


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