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직렬형 멀티레벨 인버터를 사용한 무효전력보상장치의 새로운 직류전압 평형기법

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A New Scheme for Maintaining Balanced DC Voltages in Static Var Compensator(SVC)

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Abstract - This paper examines the application of high voltage static var compensator(SVC) with cascade multilevel inverter which employs H-bridge inverter(HBI). To improve the unbalanced problem of the DC capacitor voltages, the rotated switching scheme of fundamental frequency is newly used. The optimized fundamental switching pattern with low switching frequency is adapted to be suitable for high application. The selective harmonic elimination method(SHEM) allows to keep the total harmonic distortion(THD) low in the output voltage of multilevel inverter. The SVC system is modeled using the d-q transform which calculates the instantaneous reactive power. This model is used to design a controller and analyze the SVC system. Simulated and experimental results are also presented and discussed to validate the proposed schemes.

I. INTRODUCTION

In the large power system network, the active control of reactive power is indispensable to stabilize the power systems and to maintain the supply voltage. A static var compensator(SVC) using the voltage source inverters(VSIs) have been widely accepted as the next generation of the reactive power controllers of power system. Several SVCs based on GTOs and a special zig-zag transformer have been developed and put into operation in recent years[1-2]. It has been recognized that these SVCs have advantages over the conventional SVCs of generating less harmonic current to the system and requiring a much smaller reactor. However, zig-zag transformers used in these SVCs are bulky, expensive and unreliable. SVCs based on multilevel voltage source inverter have been widely studied due to its capability of eliminating the zig-zag transformer. In this multilevel VSI based SVC category, there are mainly three different system configurations. They are 1) diode-clamped converter configuration[3-4], 2) flying-capacitor converter configuration[5] and 3) cascading converter configuration[6]. The first and second configurations require a very large number of clamping diodes or flying capacitors, respectively. But the third one has the advantages of using small number of diodes and capacitors. Moreover, packaging and physical layout is very easy due to its modular structure. It is constructed by cascading several voltage source H-bridge inverters. Although the above merits, it suffers the following disadvantages:

(1) To control the reactive power, off-line calculation of modulation index(MI) was adopted to adjust the SVC output voltage. The transient response is slow such as to the step change of var commend.
(2) The DC voltage unbalancing between capacitor makes it difficult to regulate the output voltage of SVC with cascade multilevel inverter.
(3) The DC voltage unbalancing makes system design, maintenance and stocking of spare parts complicated.

In this paper to solve these problems above, the main objective is to improve the unbalanced DC voltages of the SVC based cascade type multilevel inverter and analyze the performance of the designed prototype. One of the major limitations of the multilevel inverters was the DC voltage unbalancing between each HBI cell. To solve this problem, the novel fundamental rotated switching scheme of fundamental frequency is newly developed. To eliminate the low order harmonic of output voltage and line current, selective harmonic elimination method(SHEM) is presented. When the fundamental switching frequency is used in the proposed SVC system, THD of the inverter output voltage and current results in less than 5[%]. In the simulation and experiment, the proposed SVC system is verified on the transient response such as unit step change, most severe var commend.

II. CONFIGURATION OF POWER CIRCUIT

The simplified block diagram of the SVC system presented in this paper is shown in Fig.1. This system consists of a 7-level inverter, a set of linked reactors and series connected DC capacitors, DSP control board and the ac source mains. In this system, the three phase source volt-ages mean v_{sa}, v_{sb} and v_{sc}, and the three phase currents i_a, i_b and i_c, and the three phase inverter output voltages of SVC, v_{ca}, v_{cb} and v_{cc},, respectively. Fig. 2(a) shows the three phase unit structure of H-bridge inverter(HBI) constructed IGBT devices. It consists of the connection diagram for a wye connection 7-level inverter. Fig. 2(b) shows one module(cell) of the H-Bridge inverter with IGBT. Each HBI can generate three level outputs, $+V_{dc}$, 0 and $-V_{dc}$.

The operating principles of the SVC system can be explained by considering the single fundamental equivalent circuit. An equivalent voltage source, V_s is connected to the AC mains through a linked reactor, L and a resistor R representing the total losses in the transmission line, including inverter, as shown

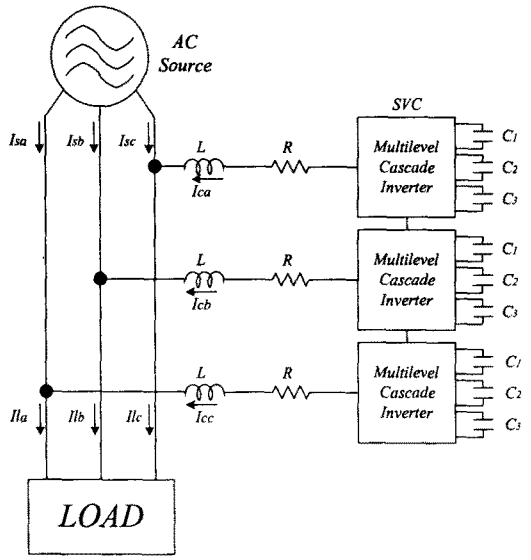

Fig.1. Structure of the SVC with cascade multilevel inverter.

in Fig. 3. By controlling the phase angle, α of the inverter output voltage with respect to the phase of source voltage, the DC capacitor voltage V_{dc} can be changed. Thus, the amplitude of the inverter output voltage, V_c can be controlled. Fig. 4(a), (b) and (c) show the phasor diagram for leading(capacitive), zero and lagging (inductive) var generation, respectively. When the inverter output voltage, V_c is higher than the ac system voltage V_s, leading reactive current is drawn from the system(var is generated). When the inverter output voltage V_c is equal to the ac system voltage V_s, reactive power exchange is zero. When the inverter output voltage V_c is lower than the ac system voltage V_s, lagging reactive current is drawn from the system(vars are absorbed). Accordingly, a large amount of reactive power drawn by the SVC

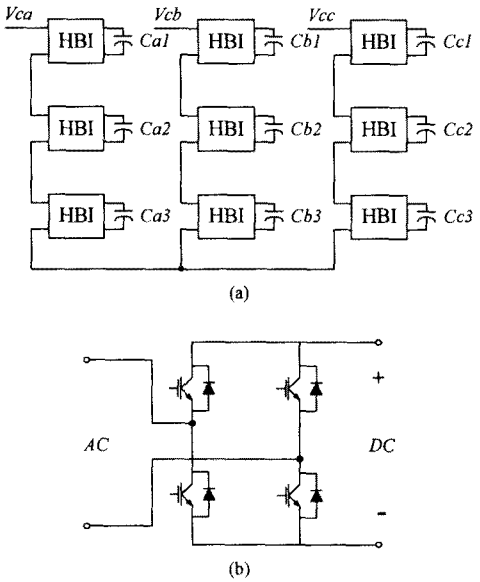

Fig. 2 Three phase cascade multilevel inverter.
(a) Main circuit of cascaded 7-level inverter,
(b) H-bridge inverter(HBI) with IGBT.

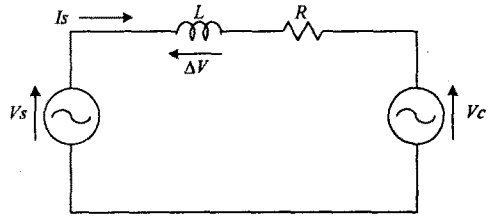

Fig. 3. Single phase equivalent circuit

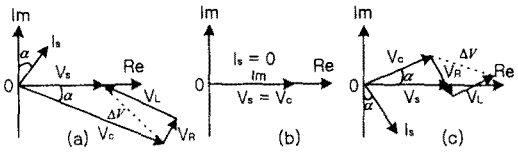

Fig. 4. Phasor diagram of the SVC.
(a) Leading current (b) Zero curmet (c) Lagging current

can be controlled by adjusting the phase angle α by the small amount. Fig. 5 shows the synthesized phase voltage waveform of a 7-level cascaded inverter with three H-bridge inverters. For each phase of the compensators, the power circuit consists of a cascade multilevel voltage inverter of independent HBI modules. The DC capacitors are floating, and no transformer is required for coupling to the transmission system. For each unit, the current rating is the nominal current of the power system. The ac voltage rating and, therefore, the DC bus capacitor voltage rating depend upon the total compensation voltage required, the number of inverters, and the sharing of the total capacitor voltage among individual units.

III. SWITCHING AND CONTROL STRATEGIES

For a stepped waveform such as the one depicited in Fig. 5 with 7-steps, the Fourier Transform for this waveform is as follows:

$$V_c(\omega t) = V_{dc}\frac{4}{\pi}\frac{1}{n}[\cos(n\theta_1)+\cos(n\theta_2)+\cos(n\theta_3)] \quad (1)$$

where $n = 1, 3, 5, 7\cdots$

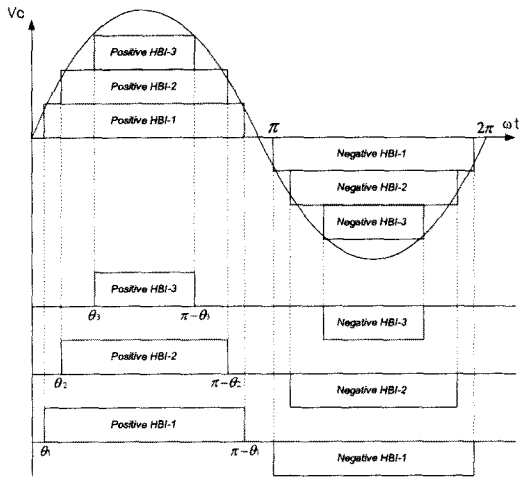

Fig. 5. Waveforms of the 7-level cascade inverter.

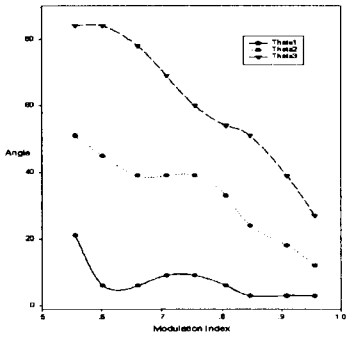

Fig.6. Range of switching angle as a function of modulation index.

Let the equations from (1) be as follows:

$$\begin{aligned}
&\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)=3M\\
&\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)=0\\
&\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)=0\\
&\cos(9\theta_1)+\cos(9\theta_2)+\cos(9\theta_3)=0
\end{aligned} \tag{2}$$

The set of equation (1) are nonlinear transcendental equation which can be solved by an iterative method. From equation (2), 5, 7, 11th harmonics can be eliminated such as Fig. 6. A fundamental switching pattern which is used the selective harmonic elimination method (SHEM) is continuously applied to the switches in each HBI module. This method is employed because it offers lower THD of SVC output voltage and lower switching frequency, thus less stress on switching devices and reduction of the switching losses are obtained by the resolution of a set of nonlinear equations. In order to overcome the DC voltage unbalancing, these switching pulses every half cycle, as shown in Fig. 7, is used. As a result, all DC capacitors are equally charged and discharged per one half cycle.

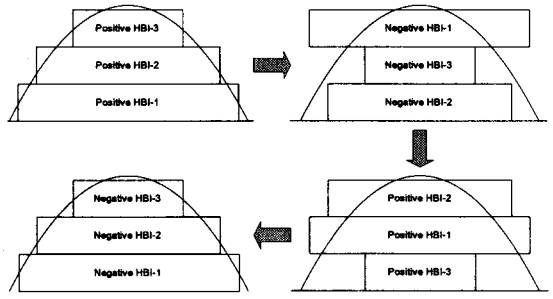

Fig. 7. Method of fundamental switching pulse rotation.

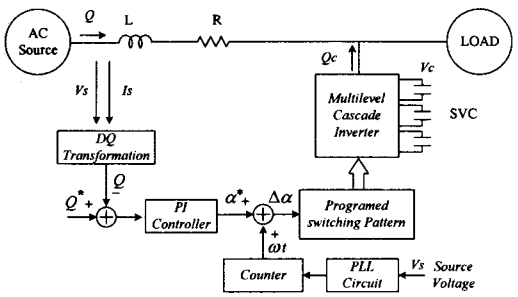

Fig. 8. Block diagram for SVC control.

This means that each switching devices in HBI modules is turned on and off equally. So, the DC voltage of capacitor is balanced in each HBI module. From the transfer function [7], a controller can be designed in order that the SVC system has fast dynamic characteristics. The SVC system equation (3) is modeled using the d-q transform which calculates the instantaneous reactive power.

$$\frac{\Delta Q}{\Delta \alpha} = C(sI-A)^{-1}=\frac{I(s)}{H(s)} \tag{3}$$

where $I(s)= V_s^2[\frac{s^2}{L}+s\frac{R}{L^2}+\frac{M^2}{L^2C}]$,

$$H(s)=s^3+2\frac{R}{L}s^2+s(\omega^2+\frac{R^2}{L^2}+\frac{M^2}{LC})+\frac{M^2R^2}{L^2C}$$

This model is used to design a control strategy based on the control of the phase angle, α of the fundamental switching pattern also. Fig. 9 shows the control diagram of this system constructed by PI controller. Reactive power feedback using a PI controller makes it possible to improve the transient response of the reactive power. The calculated reactive power Q and reference reactive power Q^* are

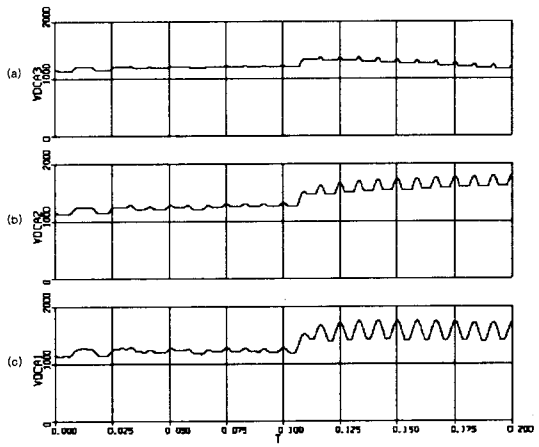

Fig. 9. DC voltage in fundamental frequency.(from 0 to -1Mvar step change); (a) DC voltage of first HBI cell, (b) DC voltage of second HBI cell, (c) DC voltage of third HBI cell.

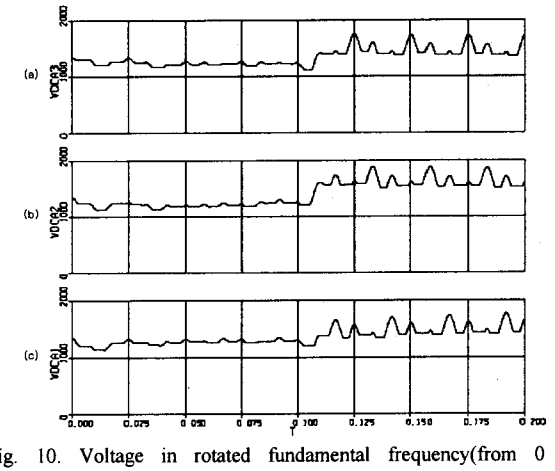

Fig. 10. Voltage in rotated fundamental frequency(from 0 to -1Mvar step change); (a) DC voltage of first HBI cell, (b) DC voltage of second HBI cell, (c) DC voltage of third HBI cell.

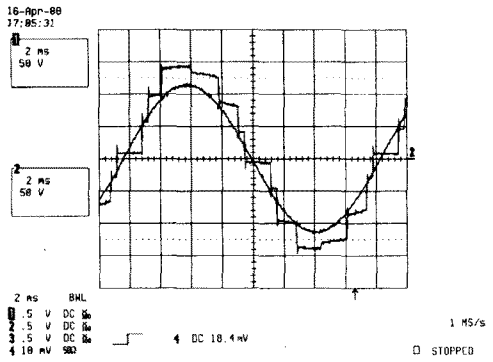

Fig. 11. Source voltage v_{sa} and output voltage v_{ca} of capacitive var generation for Q^* = -0.8[kvar].

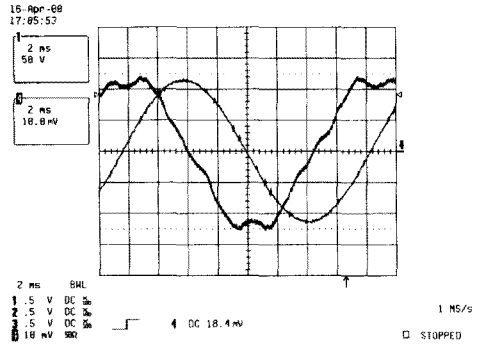

Fig. 12. Source voltage v_{sa} and current i_a of capacitive var generation for Q^* = -0.8[kvar].

applied to the PI controller. The output of the PI controller is reference signal representing the phase angle. α The counter produces the phase information, ωt from a signal generated by a phase locked loop(PLL) circuit. The phase comparator compares α with ωt, and determines the times which the corresponding switching devices are turned on and off. Each time the a angle is changed the DC capacitor voltage keeping a new stable operation voltage. Because the DC voltage changes, the output voltage of cascade multilevel inverter does too, altering its amplitude. The amount of reactive power generatedor absorbed) is basically dependent on the difference of amplitude between the source voltage and output voltage of cascade multilevel inverter.

Ⅳ. SIMULATED AND EXPERIMENTAL RESULTS

To verify analytical key results and the validity of the proposed control scheme, the aforementioned SVC structure was tested by simulation. Computer simulation was carried out using ACSL, with the system parameters given: rms line to line voltage V_s =3300[V], frequency f=60[Hz], other system parameters L=5[mH], R=0.2[Ω], C=3300[uF]. Testing of the proposed SVC system was performed for dynamic response such as step change. The reference of reactive power Q^* was adjusted to cause the system to swing from 0 to lagging mode. In the non-rotated

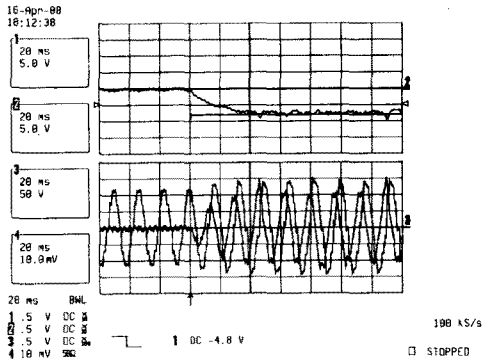

Fig. 13. Transient response for step change of reactive var commend Q^*. (capacitive var generation: from 0 to -0.8kvar)

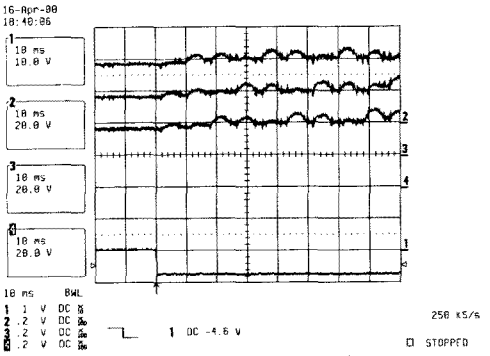

Fig. 14. HBIs DC voltages for step change of reactive var commend Q^*.(capacitive var generation : from 0 to -0.8kvar)

switching pattern, Fig. 9 shows the simulated reactive power response to a reference changed from 0[kvar] to -1[Mvar], capacitive var generation. In the rotated fundamental switching pattern, Fig. 10 shows the DC voltages in capacitive var generation and step change of reference is performed from 0[Mvar] to -1[Mvar]. In the simulation result, the rotated switching scheme can be improved by the DC voltage unbalancing of each HBI cell in Fig. 10. To confirm the validity of the presented switching method and scheme, an experimental 5kVA prototype is implemented and tested also. This sysstem consists of a 7-level inverter, a set of linked reactors and series connected DC capacitors, DSP control board(TMS320C31) and the ac source mains. This SVC system is constructed with the values given as follows: rms line to line voltage V_s=130[V], frequency f=60[Hz], other system parameters L=5[mH], R=0.2[Ω], C=2200[uF].

Fig. 11 plots the ac source voltage v_{sa} of phase A and the inverter output voltage v_{ca} of phase A. Fig. 12 is presented in the ac source voltage of phase A and the ac line current i_a, respectively. When var commend is changed from 0 to -0.8kvar, Fig.13 is plotted in the transient state result for capacitive var generation. Fig.13 is shown in the var commend reactive var Q, the phase output voltage v_{sa} and ac line current i_a. Fig. 14 is plotted in the var commend Q^* and the separate DC capacitor voltages of each HBI module. Fig. 15 is show in the harmonic

spectrums of current in capacitive var generation.

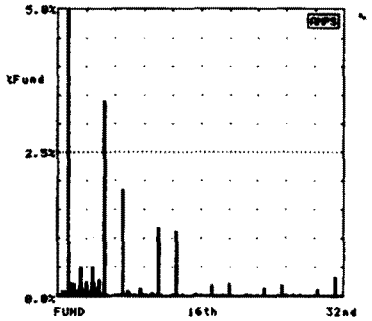

Fig. 15. Harmonic spectrums of current in capacitive var generation.

A THD of current is 4.3[%], which is satisfied with the design value below 5[%].

V. CONCLUSION

This paper presents the high power application of SVC system using cascade multi-level inverter. To equalize the separated DC capacitor voltage constantly, the fundamental rotated switching scheme is proposed. This scheme offers design, maintenance and stocking of spare parts simply. The SHE method is employed to reduce the low order harmonics of the output voltage and current of cascade multilevel inverter. The optimized fundamental switching pattern is adapted to be able for high application. The SVC system is modeled using the d-q transform and this model is used to design an efficient control strategy and analyze the SVC system. In the simulation and experiment, the proposed SVC system is verified on the transient response such as unit step change, most severe var commend. This cascade multilevel inverter is also suited for transformer-less high power application such as FACTS.

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