# 1.8V Gilbert Cell CMOS Downconversion Mixer Using

# Bulk for 2.4GHz ISM band

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## Abstract

In this work, we have designed Gilbert cell downconversion mixer using 0.25um Anam CMOS process, we also have analyzed Conversion gain and IIP3 using Taylor series in our own unique way. Especially, bulk terminal is used as LO( Local Oscillator) input for reduction of power consumption and supply voltage. Supply voltage used in this design is lower than 1.8V and core current is less than 500uA.The simulation experiments showed that the conversion gain, IIP3, and power consumption were -1dB, 4.46dBm, and 0.8mW, respectively,

Keywords — Downconversion mixer, conversion gain, IIP3, Bulk, Power Consumsuption

## 1. Introduction

In a view of the production cost and the power consumption, it is preferable for wireless applications to realize the RF front ends circuits on a same chip as the digital signal processing circuits. The downconversion mixer is one of the indispensable RF blocks in communications receivers, where its main function is the translation of the incoming RF signal to an intermediate frequency for analog and digital signal processing. Therefore, a CMOS downconversion mixer is considered for the single chip approach, because most baseband chips are implemented using CMOS process. To meet the requirements of low power

consumption mixer, the various structures of mixer have been studied[1]. Gilbert cell mixers are still the main architecture of up-downconversion mixer. However, standard Gilbert cell mixers are difficult to operate such low supply voltage due to stacking architecture. In this paper, we present a 1.8V Gilbert

cell downconversion mixer for ISM band, using bulk terminals to alleviate the stacking architecture. The conversion gain and IIP3 of the proposed mixer were analyzed using Taylor series.

## 2. Basic concept and Theoretical analysis of Bulk driven mixer
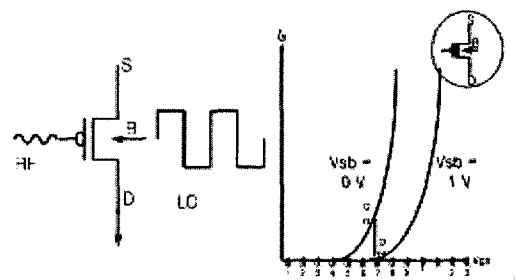


Figure 1. Basic concept of one PMOS switch

As shown in Fig. 1, bulk terminal is driven by a large square signal. If the PMOS device is switched between on and off according to variations of Vsb (the bulk terminal voltage) PMOS device can be linear system under small signal RF swing in the saturation[2]. It is an appropriate assumption because the LO signal is sufficiently larger than the RF signal. LO signal and RF signal are applied to the bulk and the gate, respectively, as shown in Fig. 1. With uses of MOSFET I-V characteristics including short channel effects [3], Kirchhoff's voltage law, and Volterra series technique [4], we calculate the differential current $I_{RF}$ as a function of the signal source voltage $V_{in}$ ;

$$I_{RF} = \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3 \ldots\ldots \qquad (1)$$

Assuming the complete switching of LO driven transistors, we can obtain the desired IF by multiplying $\omega_{RF}$ and $\omega_{LO}$ together. So the voltage conversion gain , Av, and the power conversion gain, Ap, can be expressed by [2];

$$A_V = \frac{2}{\pi} G_m R_{load} \qquad (2)$$

$$A_P = A_V{}^2 \frac{R_{source}}{R_{load}} \qquad (3)$$

In our calculation, We have used the current equation including short channel effects and body effect to accurately calculate the conversion gain and IIP3 [3].

$$Id = Iz \times \left( \left( Log\left[1 + e\left[\frac{Vgs - Vtp}{2n\phi_T}\right]\right]\right)^2 - \left( Log\left[1 + e\left[\frac{Vgs - Vtp + nVds}{2n\phi_T}\right]\right]\right)^2 \right) \qquad (4)$$

where n and Iz are given by;

$$Iz = 2\mu C_{ox}' \frac{W}{L} n\phi_T^2 \qquad (5)$$

$$n = -1 - \frac{\gamma}{\sqrt{-Vsb - \phi}} \qquad (6)$$

where $\phi_T$ is the themal voltage kT/q (0.0259mV) and Vtp is the threshold voltage which can be expressed by Vto-(n+1)Vsb. All other symbols have their usual meanings and accurate expressions for which are given elsewhere[5]. Note that all voltages expressed in Eq. (4) and equation (6) are taken with respect to the body. Therefore, Eq. (4) and Eq. (6) are very important to analyze the conversion gain and IIP3 in this calculation. Since bulk is used as a switch, we can express the value of transconductance (Gm) using Eq. (3)

$$Gm = Iz \times \left( \frac{\left(e\left[\frac{Vgs - Vtp}{2n\phi_T}\right]Log\left[1 + e\left[\frac{Vgs - Vtp}{2n\phi_T}\right]\right]\right)}{\left[1 + e\left[\frac{Vgs - Vtp}{2n\phi_T}\right]\right]n\phi_T} - \frac{\left(e\left[\frac{nVds + Vgs - Vtp}{2n\phi_T}\right]\right)}{\left[1 + e\left[\frac{nVds + Vgs - Vtp}{2n\phi_T}\right]\right]n\phi_T} \times \frac{Log\left(1 + e\left[\frac{nVds + Vgs - Vtp}{2n\phi_T}\right]\right)}{\left[1 + e\left[\frac{nVds + Vgs - Vtp}{2n\phi_T}\right]\right]n\phi_T} \right) \qquad (7)$$

Substituting Eq.(7) to Eq.(2), conversion gain can be easily obtained. Fig.2 shows that the difference of the Gm by the difference of Vsb in accordance with an increase of Vgs.



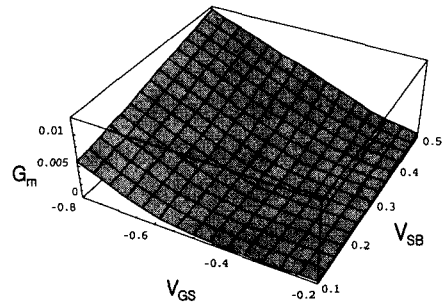Figure 2. Gm versus Vgs and Vbs

IIP3 which is the intercept point between the basic frequency output power and the output power of third-order frequency components is well known to be simlified by using the coefficient of the Eq. (1), It is also expressed as equation (6).

$$IIP3 = 20 \times Log\left(\sqrt{\frac{4}{3} \times \frac{|\alpha_1|}{|\alpha_3|}}\right) \qquad (8)$$

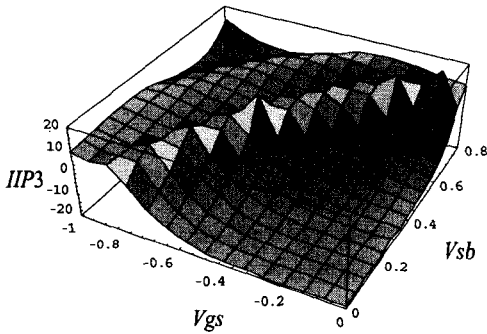IIP3 can be determined by the coefficient which is used in Eq.(1) by applying to Eq. (6).



Figure 4. Proposed Gilbert cell mixer



Figure 3. IIP3 versus Vgs and Vbs

Fig.(3) shows the variations of the IIP3 according to the alternative of Vgs and Vsb. The proposed mixer is shown in Fig.4. This mixer is Gilbert cell type, where the bulk is driven by large LO(Local Oscillator) signal. The gate terminals are driven by the differential RF signal having frequency of 2.45GHz , and the bulk terminals are driven by the differntial LO signal having frequency of 2.4GHz.
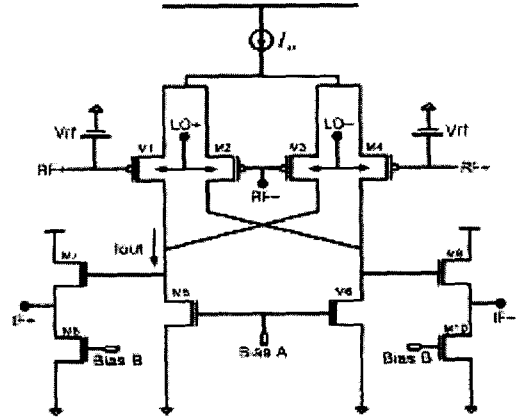
M1, M2, M3 and M4 are PMOS devices. There are two important reasons why pMOS transistors are used as switchs in this architecture. One is that the $f_T$(unity current gain frequency) of pMOS transistors is relatively high (>20GHz), they can be used in RF circuits to drive current. and the other is that the pMOS transistor can be used to fold the RF signal from one supply branch to another. Therefore, the use of pMOS transistor as a switch can reduce the overall supply voltage of the circuit[6]. M5 M6 are nMOS transistors. These transistors were used as load resistors to realize the desired conversion gain. The value of the load resistance is controlled by their width and the bias A. M7, M8 and M9, M10 are output buffers designed for driving 50 $\Omega$ load.

Since the conventional Gilbert cell mixer where RF and LO path consist of cascode structure has voltage headroom problems, the design of mixer structures without tail current source have been studied. However, the characteristics of relationships between Vrf and Iout may show different characteristics each other when the mixer includes the tail current source or not.   Vrf and Iout mean the RF input voltage and output current showed in Fig.4. Saturation voltage (Vs) can be expressed as follows.

$$Vs = \sqrt{\frac{2I_{SS}}{\mu C_{OX} W / L}} \qquad (9)$$

According to the equation(7), the increase of DC current or the decrease of the ratio the W/L causes the increase of Vs. However, since, both cases have trade-off between the linearity and the conversion gain, designer should make a choice of profitable structures in accordance with the purpose of the design specification.. In this work, the structure having tail current source has been selected to improve linearity.

## 3. Simulation Results

Table 1 summarizes the simulation results. The RF, LO, and IF frequencies used are 2.45GHz, 2.4GHz and 100MHz. respectively, the conversion gain is illustrated in Fig. 5. According to the Figure, the power conversion gain is –1 dB up to the RF power of –13 dBm. Fig. 6 shows the result of conversion gain, where Vrf voltage variations are starting from 0.3 V to 0.5 V. Fig. 7 shows the result of IIP3 where the Vrf is swept from 0.2 V to 0.8 V. As expected in the previous analysis, IIP3 value is very sensitive to Vrf.



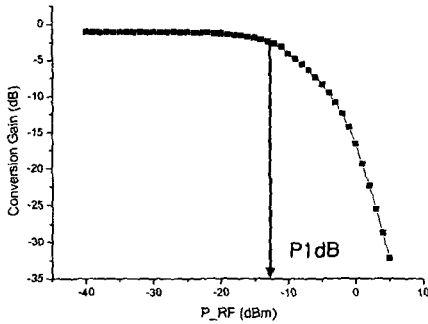Figure 6. Simulated Conversion gain



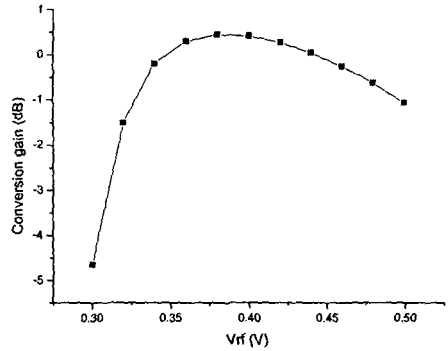Figure 7. Simulated IIP3



Figure 5. A<sub>P</sub> versus RF input power
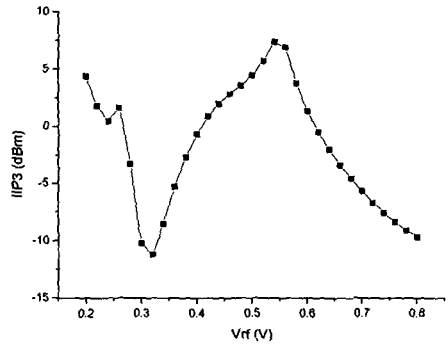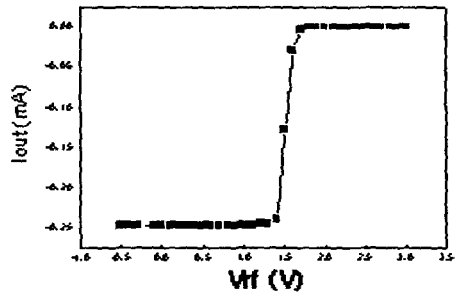


Figure 8. Vrf versus Iout with tail current source
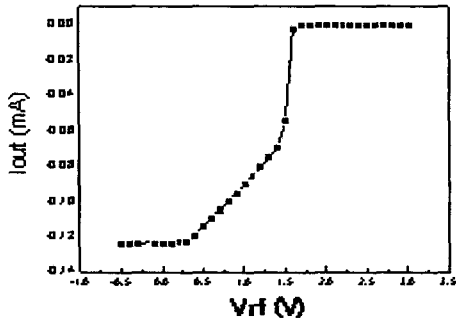
**Figure 9. Vrf versus Iout without tail current source**

**Table 1.**

**Summary of mixer performance**

| | Performance |
|---|---|
| Supply voltage | 1.8 V |
| Power dissipation | 0.8 mW |
| Input LO power | 0 dBm |
| RF frequency | 2.45GHz |
| LO frequency | 2.4GHz |
| Conversion gain (Ap) | -1.2 dB |
| IIP3 | 4.46dBm |

## 4. Conclusion

In this work, we have designed Gilbert cell downconversion mixer using bulk terminal for LO path, and have analyzed conversion gain and IIP3 in our own unique way. The results of analyzed conversion gain and IIP3 are in agreement with the results of simulation. This proposed Gilbert cell mixer's power dissipation is less than 0.8mW.

## 5. References

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