MRAM technology - Recent progress and issues

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1. Introduction

Since the attainment of large tunneling magnetoresistance at room temperature in 1995,[1)] magnetoresistive random access memory (MRAM) based on magnetic tunnel junctions (MTJs) has become a focus of interest among researchers. The MRAM is a nonvolatile memory having the advantages of low operating voltage of less than 1 V, unlimited read/write endurance, high-speed operation, and a high degree of CMOS process compatibility.

In order to prove the advantages of MRAM, it is necessary to solve two problems: (1) lack of bit uniformity, and (2) high write current requirement. In this paper, recent progress in the NEC-Toshiba MRAM development alliance is reported. First, we report integration of 1 Mbit MRAM. Some measures were taken to increase the bit uniformity. Second, a yoke wire technology, which is thought to solve the problem of high write current, is reported. The yoke wire was successfully implemented in 1 kbit MRAM, and proved its effectiveness. Lastly, issues that need to be resolved if MRAM is to be a versatile memory are discussed.

2. Integration of 1 Mbit MRAM

We chose 1 Mbit test element group as a technology vehicle for the development of the MRAM. The element was based on a 1-Transistor and 1-Magnetic Tunnel Junction (1T1MTJ) bit cell. A bit yield was measured as a function of writing currents. After improvement of the integration process, more than 80% bit yield was obtained for a 1 Mbit MRAM for a relatively broad range of bit-line and word-line currents.[2)] The improvement consists chiefly of two points as follows. First, the uniformity in the switching field was increased by increasing the anisotropy of a free layer of the MTJ. Second, adjustment of an MTJ patterning shape decreased the number of short-circuits in MTJs.

3. Yoke wire technology

To reduce the writing current, the yoke wire technology has been developed. The bit-line and word-line are covered with the yoke made of a NiFe thin film, which has high magnetic permeability and concentrates the magnetic field on the MTJ. We have fabricated a 1 kbit MRAM

yoke-covered bit-line and word-line. As a result, the writing current was reduced to less than a half of the value without yoke. After improvement of integration process of the yoke wire, a 100% bit yield was successfully obtained for a 1 kbit MRAM.[3]

4. Other issues

In order to combine the attributes of high density and high speed of MRAM, a readout signal should be increased. Since magnetoresistance ratio decreases with increasing applied voltage, small voltage dependence is desired. A double MTJ has been proposed for a large-readout-signal device showing small voltage dependence. Recently, a 1 kbit MRAM using the double MTJ in each memory cell has been successfully fabricated.[4]

The tunnel barrier in MTJ is typically an approximately 1 nm-thick aluminum oxide layer. Short-circuit of the tunnel barrier during etching of the MTJ devices is one of the main failure modes. So, the MTJ patterning technique is still a key issue. Recently, a chemical assisted ion etching technique, which has sufficiently long time margins in the etching process, has been developed.[5]

5. Summary

The 1 Mbit MRAM without yoke wire and 1 kbit MRAM with the yoke wire, were successfully fabricated. Once the problems discussed in this paper are solved, MRAM will become a versatile memory applicable to both commodity and embedded memory.

6. References

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