# *Integration Technologies for 3D Systems*

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## Outlook

- Wafer-Level Chip-Scale 3D-Integration (WL-CS-3D)
- Handling Concept
- Relevant Technological Integration Concepts
- Features of demonstrated Metalization System
- Introduction of „InterChip Via (ICV) / SLID" Process Flow for Vertical System Integration VSI®
- Summary



## Status

1990 .... 2003 2007 2010

Research on Different Technological Strategies

**Increasing 3D-Complexity** → **Full 3D-Integration Era**

**Entry to Market**
(Announcement of Infineon)

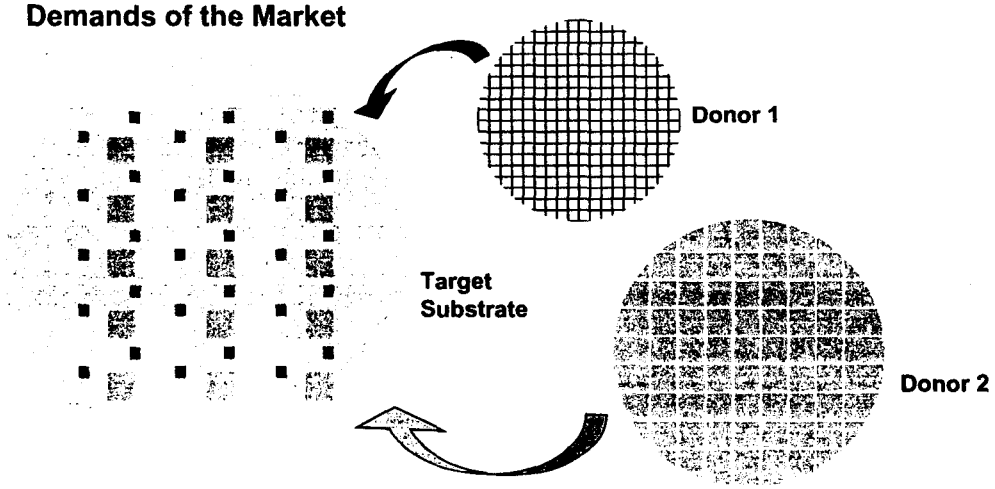
- Reduced Layout Effort
- Placement of InterChip Contacts below Bondpads
- Layer dedicated Functionality
- Standard Wafer-Level Testing
- Remaining Silicon Thickness 10 µm < d ~ 50 µm
- Automatic Design- and Layout Softwaretools
- Arbitrary Placement of InterChip Contacts
- Split-Layout for Chips to reduce Area per Layer
- Testability Concept for each separate Layer before Stacking
- Remaining Silicon Thickness << 10 µm

Chance: Increase of Performance
but: Costs per Chip (or Interconnect) as Main Criteria





## Demands of the Market






## Requirements for WL-CS 3D-Integration

- Integration Concept for „low"-Placement Accuracy
- Suitable for
  - different IC-Technologies
  - different Wafersizes
  - different Chipsizes
- Modular Process Scheme for building Multilayer-Stacks
- 3D-Integration as Add-On Process
  for completed Product Wafers (Extension of Backend Processing)

**Some Restrictions**

Standard Al-Metallization: $T_{max}$ < 450 °C;
Fuses: $T_{max}$ < 300 °C;
MRAM: $T_{max}$ < 200 °C;





## *Handling Concept*



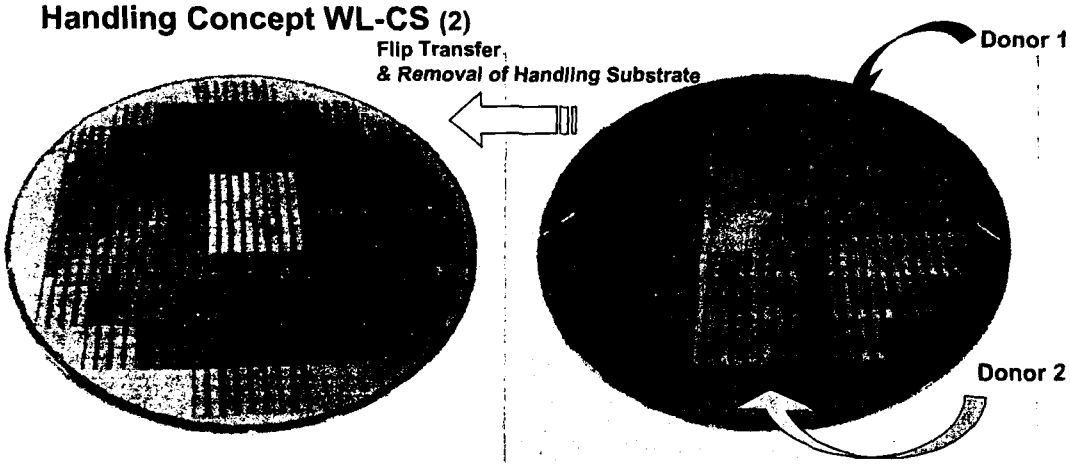
## Handling Concept for Wafer-Level Chip-Scale Processing (1)

- Placement of Chips on Handling Substrate
  - Grid of Aligment Marks according to the Positions on the Target Wafer
- Processing of Chips on Wafer Scale
  (e.g. cleaning prior to bond, thinning, backside metalization etc.)
- Transfer to Target Wafer
  - Adjusted Soldering
  - Removal of Handling Substrate
- Further Processing of new Stack (if necessary)



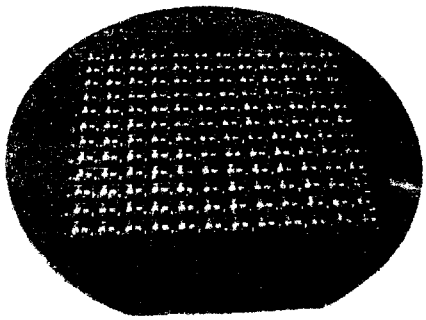


## Handling Concept WL-CS (2)

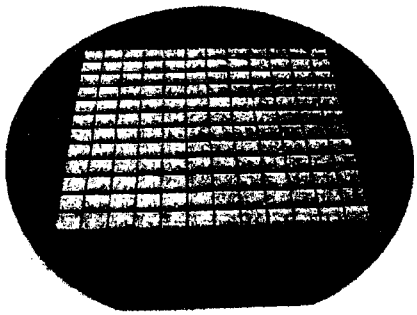





## Handling Concept WL-CS (3) Removal of Copper Oxide



**Chips on Handling Substrate;
blue colour of chips results from copper oxide formation during placement procedure**



**Clean copper surface after wet chemical removal of copper oxide (wafer or batch)**



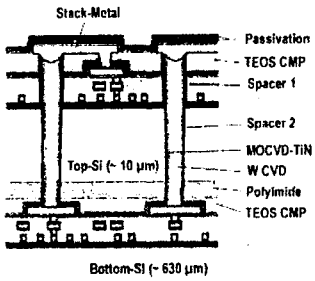


## *Concepts and Realization*



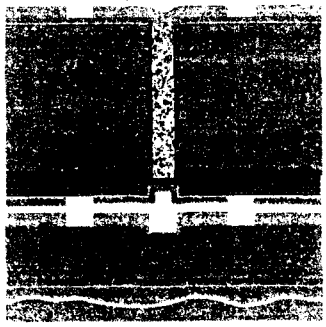
# Vertical System Integration – *Three relevant Concepts (IZM-M)*

**InterChip Via (ICV)**



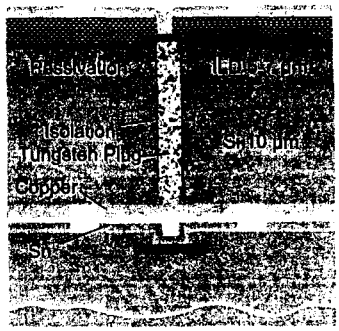

W-Plug / Polyimide

**Face to Face modular (F2F-M)**



W-Plug / Cu / Sn

**ICV / SLID**




W-Plug / Cu / Sn

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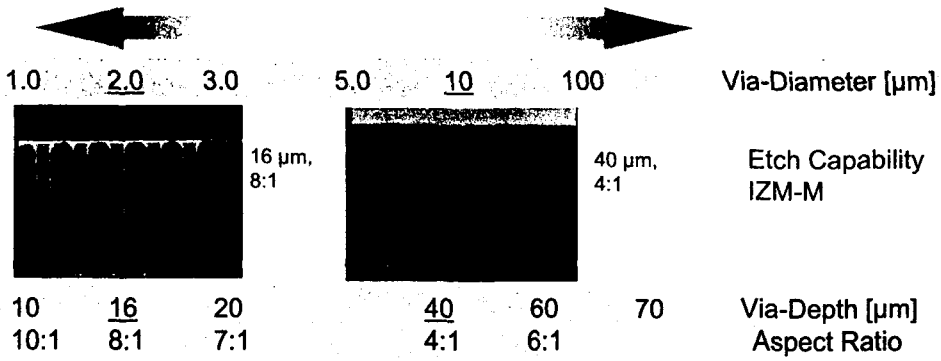
# Via Formation for VSI – *Via Etching*

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# Via Formation for VSI – *Via Metal Filling*

| 1.0 µm | 3.5 µm | 5 µm | 10 µm | .... | 100 µm | Via-Diameter |
|---|---|---|---|---|---|---|
| CVD of<br>- copper<br>- tungsten<br>- TiN | | Electroplating of<br>- copper<br>PVD of Seedlayer<br>- Ti:W / Cu | | | | Process for filling |
| | 10 µm | | 70 µm | .... | 100 µm | Via-Depth |
| 10:1 | 3:1 | 2:1 | .. 7:1 | | 1:1 | Aspect Ratio |

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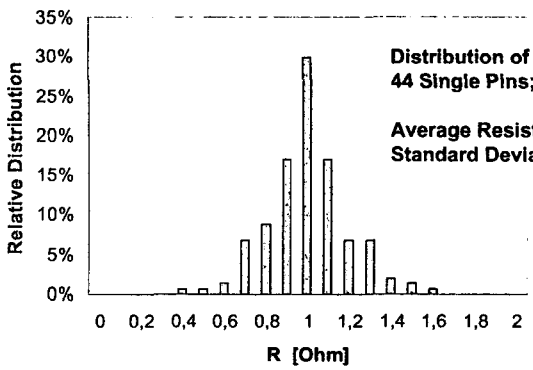
# Via Formation for VSI – *Tungsten Pin Resistance*

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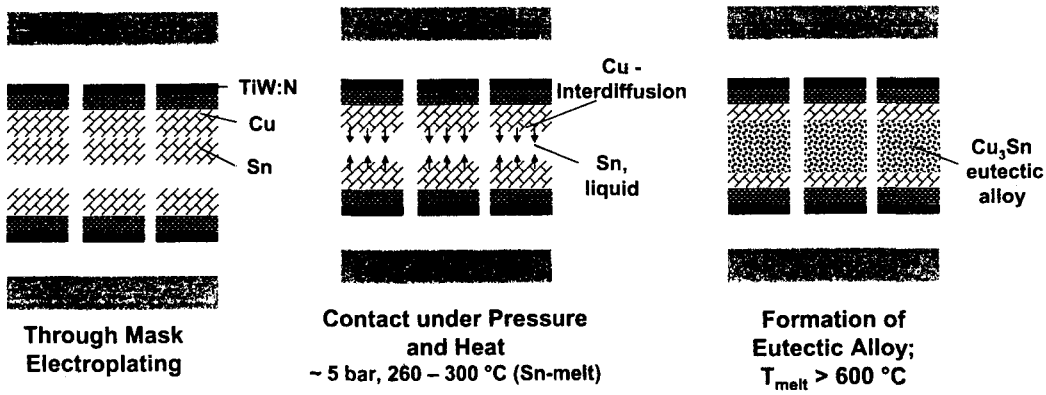
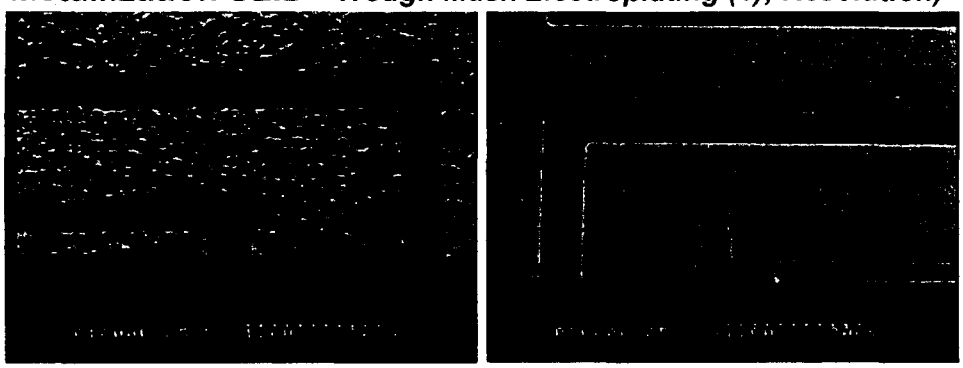
# Metallization SLID (Solid Liquid Interdiffusion)





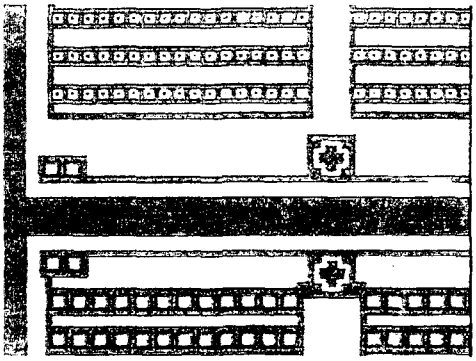



# Metallization SLID - *Trough Mask Electroplating (1); Resolution)*

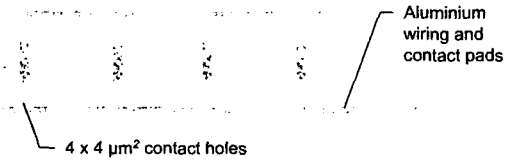


- Complementary structures with tin and copper
- 10 µm trenches in metal surface

## Metallization SLID - *Trough Mask Electroplating (2)*
## *Testchip for F2F-M & ICV/SLID*



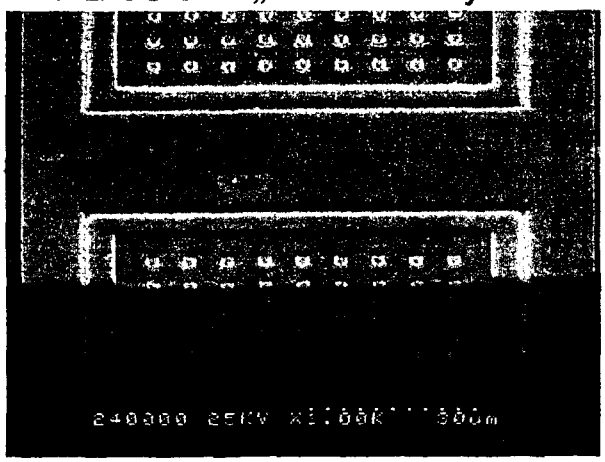
- **Copper / Tin-Alloy:**
  - **Simultanious formation of electrical and mechanical connection**
  - **Thin layers (10 µm in total) with large contact area replace underfiller**
  - **Testchip with dedicated wiring- and soldering layers**



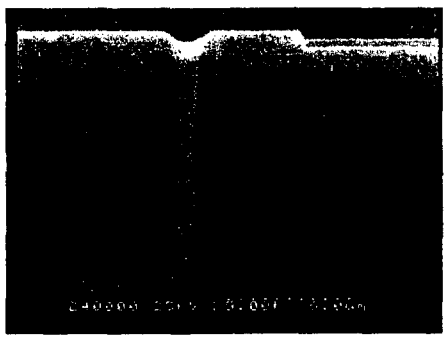




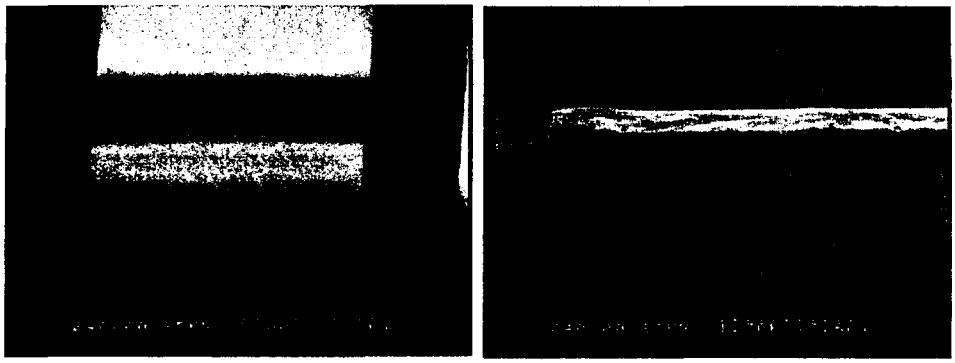

## WL-CS-3D - *„low – Accuracy Placement" Layout (1)*



- Pin-Array and Isolation trenches
- combination of contact printing with stepper lithographie is possible



## WL-CS-3D – *„low – Accuracy Placement" Layout (2)*



- Copper pads on top of pin-array; development of „Electroplating prior to thinning"

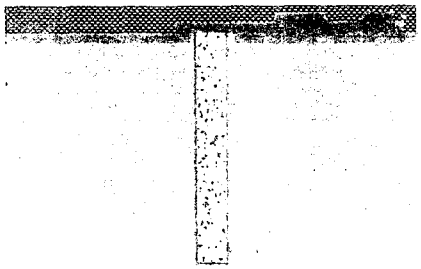




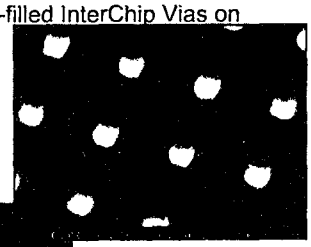
## *Two Layer Stack with InterChip Via / Slid*

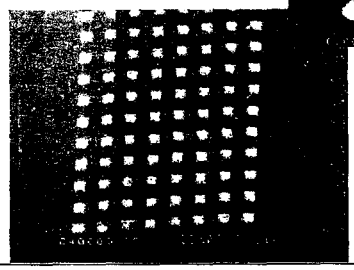


## ICV / SLID - *Concept vs. Realization (1)*



- Fabrication of Tungsten-filled InterChip Vias on Top Substrate
- Via Opening and Metallization (CVD)
- Thinning

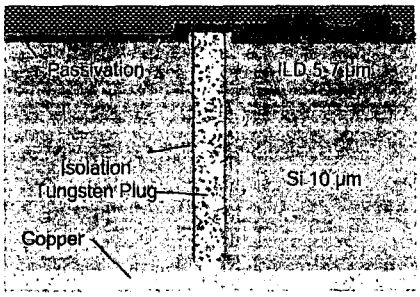






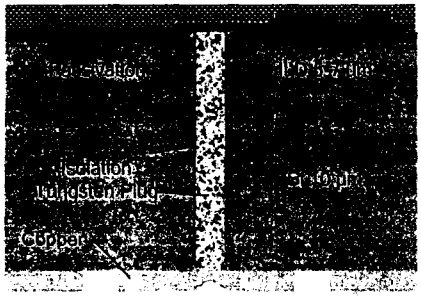
3D System Integration

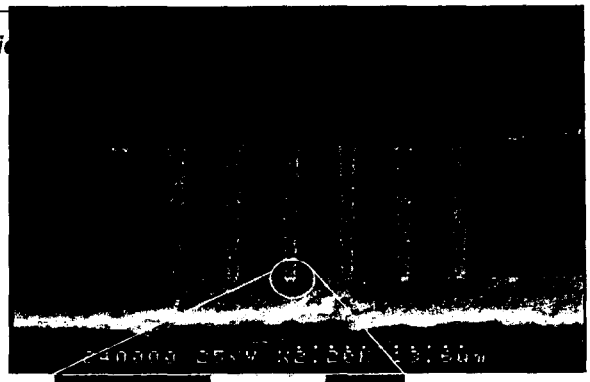
## ICV / SLID - *Concept vs. Realization (2)*




- Fabrication of Tungsten-filled InterChip Vias on Top Substrate
- Via Opening and Metallization
- Thinning
- Opening of Plugs
- Electroplating

## ICV / SLID - *Concept vs. Realizati*

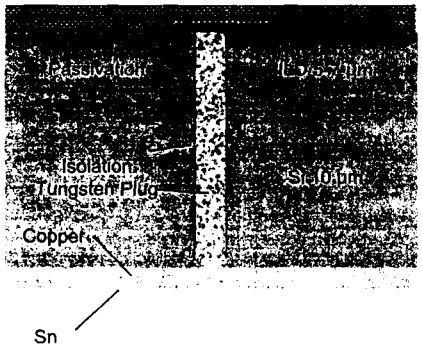


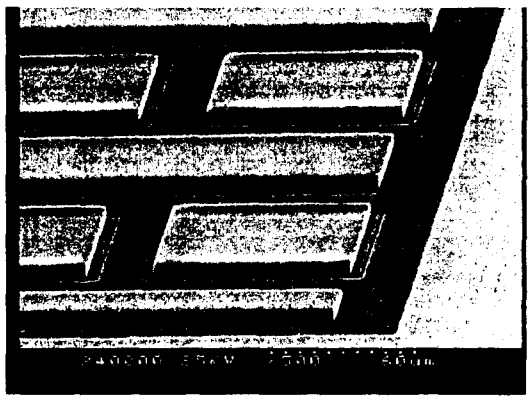





3D System Integration

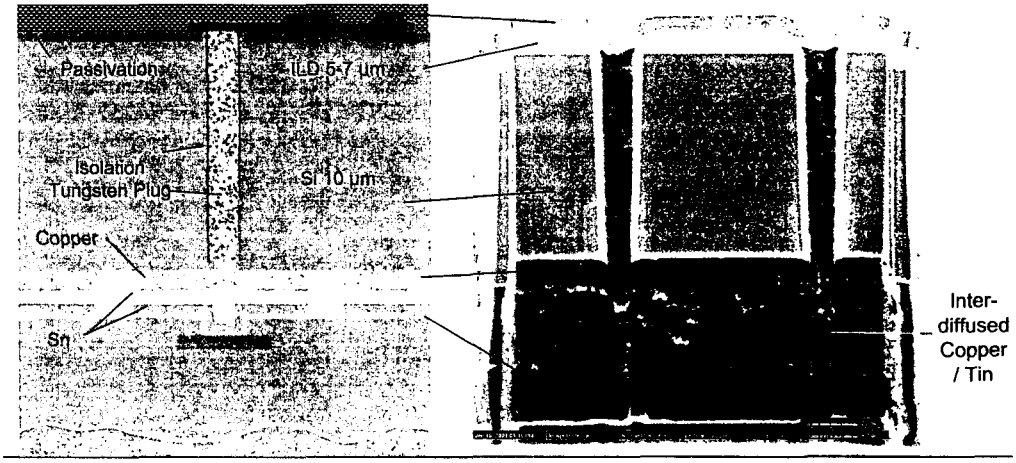
## ICV / SLID - *Concept vs. Realization (3)*





## ICV / SLID - *Concept vs. Realization (4)*



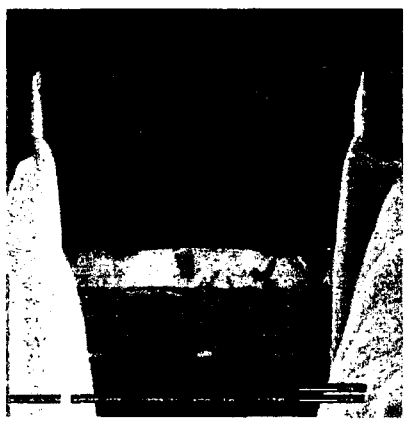





## Metallization SLID - *Details (1)*

Influence of (Non)-Precleaning:

- Nearly complete Consuption of the underlying Copperlayer
- Sn does not dissolve Copper Oxide
- Removal of Oxide on Copper is essential
- Sn seems to dissolve it's own Oxide



## Metallization SLID -
***Details (2)***

Detail of Interface:

- Formation of Voids due to Volume Loss ?
- Oxide Residues ?
- Influence on Electrical Properties ?
- Influence on Reliability ?

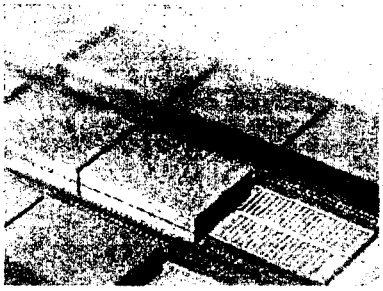




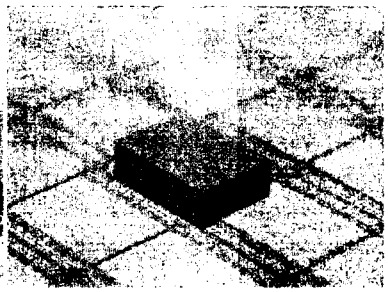
## WL-CS-3D – *Three layer stack (0)*

***Three Layer Stack with Face-to-face Modular***

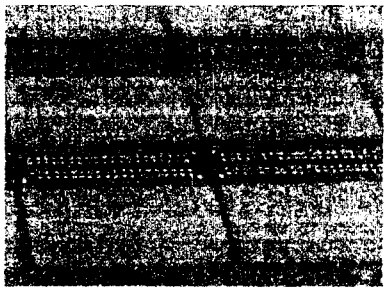
# WL-CS-3D – *Three layer stack (1)*



**C2W-Transfer Development**
After Chip Transfer from Intermediate Handling Wafer to Target Substrate
Chip Thickness 500 µm



After Thinning on Target Substrate
Chip Thickness 10 µm
plus original Chip for Comparison



After Thinning on Target Substrate
Chip Thickness 10 µm

**Measured Resistance with Daisy Chain Structure:**
**0.5 Ohms / Contact (incl. 2 Diffusion Barriers)**

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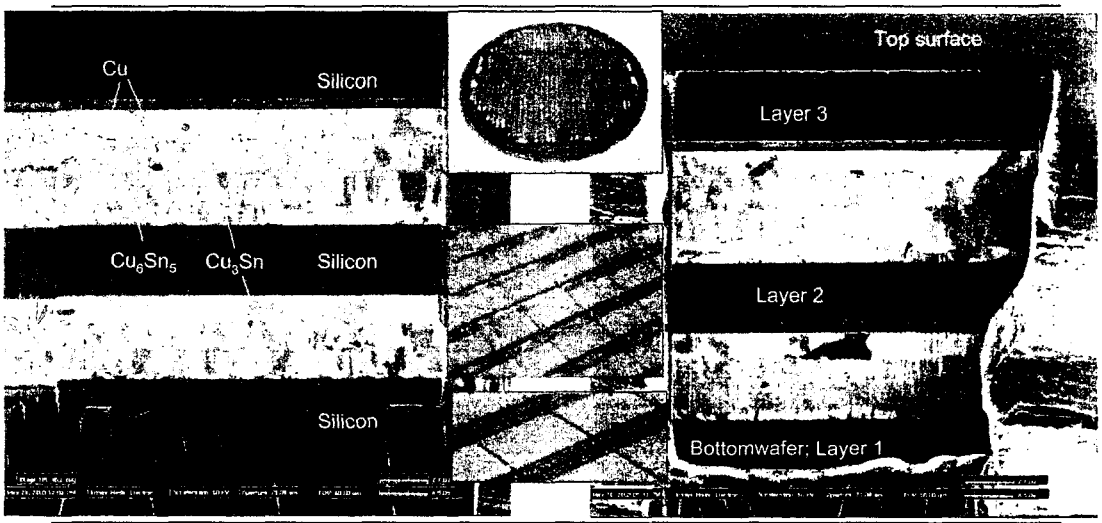


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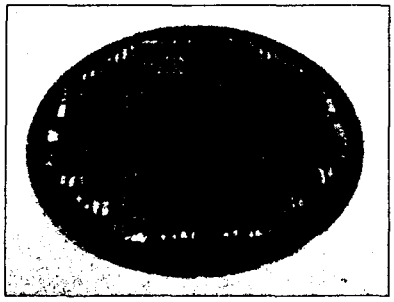
## WL-CS-3D – *Three layer stack (4)*



8"-Bottom Wafer with Three Layer Stacks

Detail: Thinned Top- and Medium Chips on Bottom Chip (Electrical Measurement Pads visible)





## WL-CS-3D – *Three layer stack (5)*

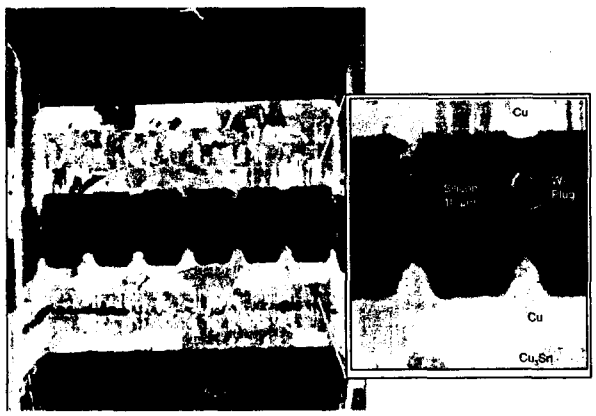
Top Chip; Layer 3

Soldering Layers

Pin Array of Medium Chip; Layer 2

Soldering Layers

Bottom Chip; Layer 1



## Electrical measurements

Daisy Chains with up to 240 elements

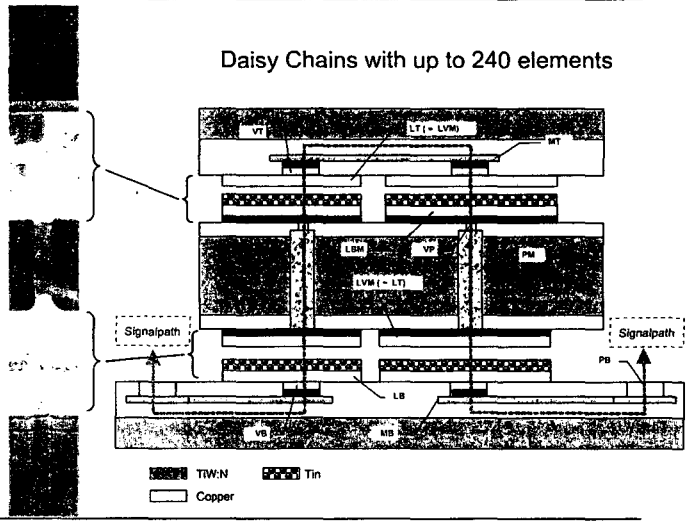
Measured values:

Contact hole + soldering layers. 0.43 Ohms

W-plug: 1 Ohm

Contact hole + soldering layers. 0.43 Ohms

Sum Value calculated from 240 element chain: 2.5 Ohm








## Summary (1)

### Concepts

- Wafer-Level Chip-Scale Concept with Handling Substrate
- Low Accuracy Placement Layout with Isolation Trench
- Possible Pitch of Interconnections down to 10 µm (Sn-Grains)
- Wafer-to-Wafer Equipment Adjustment Accuracy meets this Request of Alignment Accuracy (+/- 1.5 µm)
- Adjustment Accuracy of High-Speed Chip-to-Wafer Placement Equipment starts to meet this request
- Face-to-Face Modular / SLID with Flipped Device Orientation
- Interchip Via / SLID with Non-Flipped Orientation



## Summary (2)

### SLID Technology Features

- Demonstration with Copper / Tin-Alloy (SLID) and W-InterChip Vias (ICV)
- Combination of reliable processes for advanced concept
  - Filling of vias with W as standard wafer process sequence
- No plug filling on stack level necessary
- Simultanious formation of electrical and mechanical connection
- No need for underfiller: large area contacts replace underfiller
- Cu / Sn SLID layers ≤ 10 µm in total are possible





## Summary (3)

### Electrical Results

- Measurements of Three Layer Stacks on Daisy Chains with 240 Elements
- 2.5 Ohms per Chain Element
- Contribution of Soldering Metal only in the Range of Milliohms
- Soldering Contact Resistance (0.43 Ω) dominated by Contact Resistance of Barrier and Seed Layer
- Tungsten Pin Contribution in the Range of 1 Ohm