The trend of packaging technology in Japan

Seiko Epson corporation
Production engineering and
Development Department
Kazumi Hara

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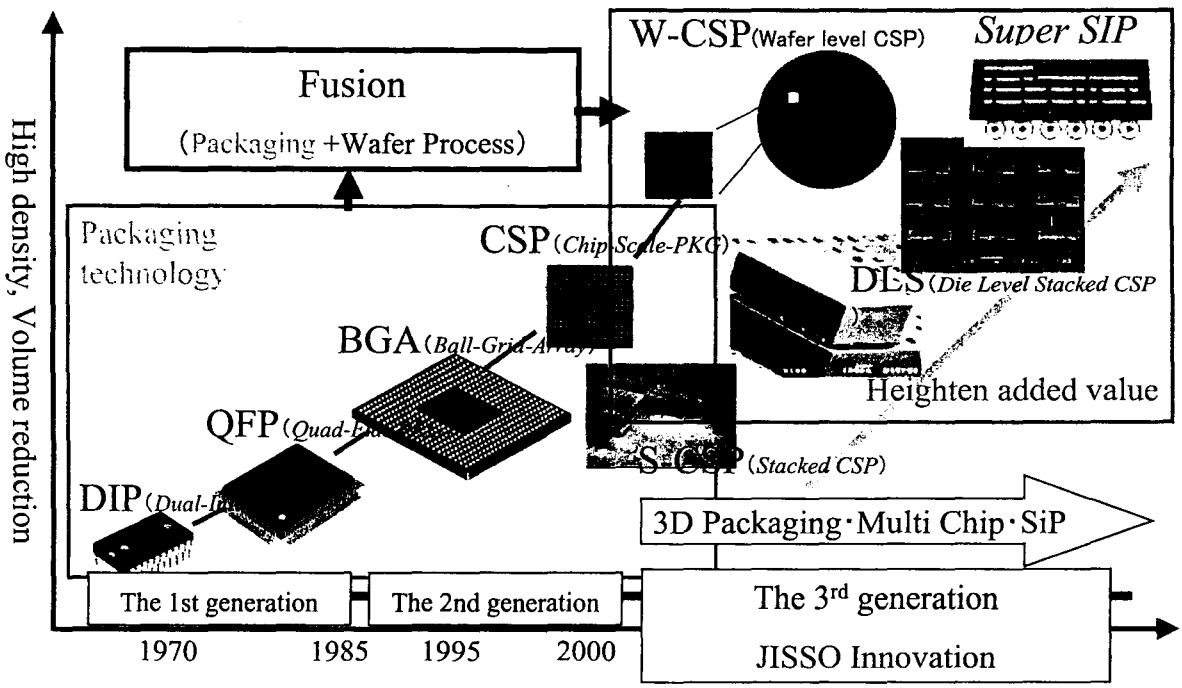
SIP technology and the latest issues

Development of Packaging technology



Advantage of SiP

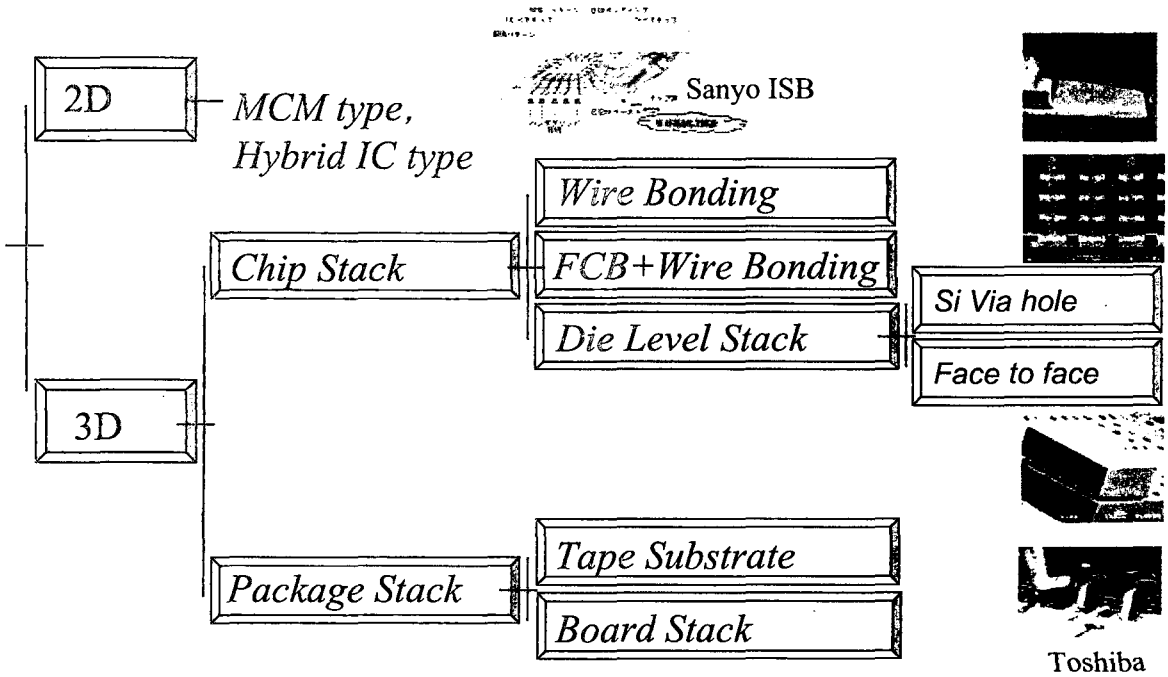
◆Features

- High performance

  Sophisticated functions ,Body shrinking
- Quick delivery
- Match with merchandise life cycle
- Expectation for high yield

  KGD are available

Classification of SiP



Package stack

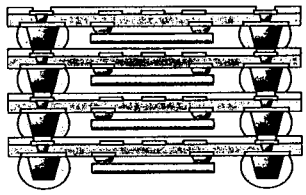
◆Features

- Most flexible for design
- Material cost increase, because some substrates are required
- Applications of the original technologies of the company

◆Venders

Sharp ,NEC, Toshiba, North

DT Circuit technology, NASDA,Kyosera



NMBI
North

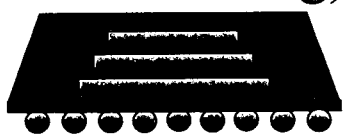
System block module
(Paper Thin Package)
Toshiba

Toshiba

Chip stack (connection by wire bonding)

◆Features

- The conventional packaging technologies and machines are available.
- Low cost
- Quick delivery



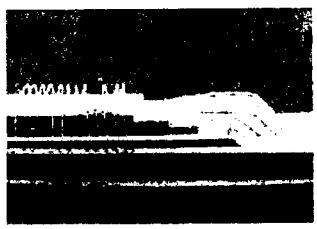
Image

FCB+Wire bonding
Seiko Epson

◆Venders

NEC, Hitachi ,Fujitsu, Sharp,

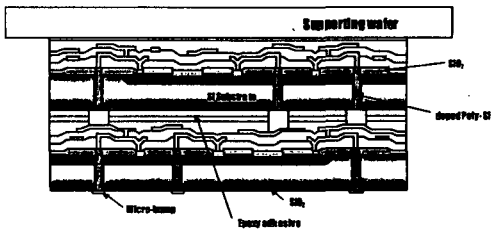
Mitsubishi, Seiko Epson, etc



4 layer stacked package

From the website of SHARP

Chip stack (direct chip connection)



CREST
Tohoku University

◆Features

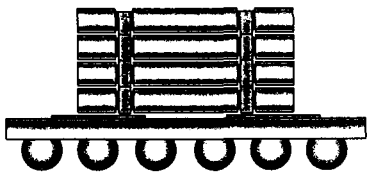
- Extremely small and light
- The shortest line length

  Good for high frequency circuits
- Restrictions in design (chip scale , pad layout, etc)

  Collaborations between IC benders and packaging benders are needed

◆Venders

Tohoku university	Wafer on wafer
Fujikura	Wafer on wafer
Aset	Chip stack
Seiko Epson	Chip stack
Rohm	Chip stack (Face to face)



Aset

Comparison of types of structure

◆Summary

Evaluation terms	Package stack	Chip stack wire bonding	Chip stack with vias
Size and weight	weak	better	excellent
Usage of existing chips	possible	some limitations	special chip only
Flexibility for design	exellent	some limitations	some limitations
Time to delivery	quick	quick	weak
Cost	high material cost	better	better
Neccesity of investment	a little	none	a lot
Sprit of inovation	original	conventional	progressive

The latest issues

◆Needs of thin wafer

- Mass production : 140um (Seiko Epson)
- Under development : less than 100um

◆Difficulties of thin-wafer-handling

- Warpage of wafer
- Crack

Warpage of wafer

Crack of wafer

Wafer support system WSS

◆Concept

- Reduction of damage
- Easy handling

◆Requirement

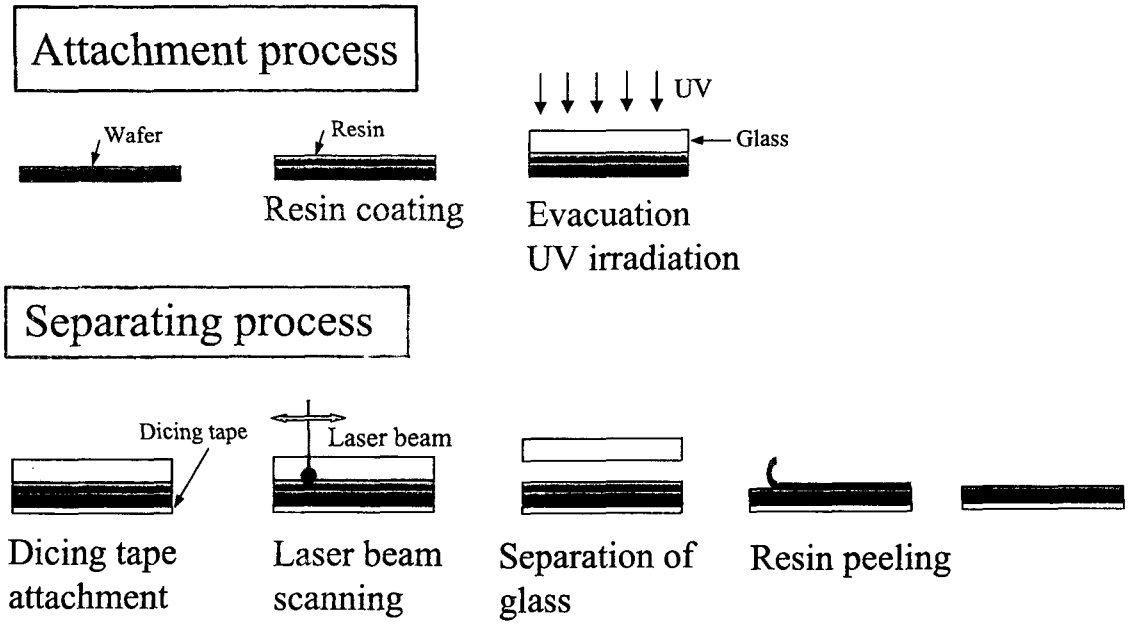
- Easy on, easy off
- Endurance

Structure of WSS

Various kinds of methods proposed

Supporting material	Adhesive	Separating	Minimum thickness	Φ12	Bump absorbability	Investment	Vender
PET	UV release tape	UV+peeling	50um	difficult	30um	no need	
Glass	UV release tape	UV	25um	possible	30um	need	Sekisui chemical
	UV Resin	laser	25um	possible	50um	need	Sumitomo 3M
	Wax	heat	25um	possible	<10um	need	?
Stainless	Magnet sheet	peeling	50um	possible	?	need a little	Sumitomo 3M

Example of GWSS in Sumitomo 3M

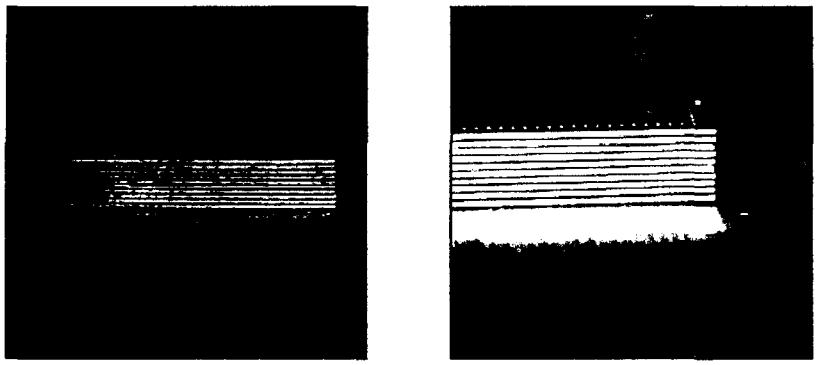


Wafer support system WSS

◆Development status of WSS

- Many support methods have been proposed.
- Among them, PET-support-method is available now.
- Methods using another support are under development.
- The hardship is the easy separation in practical cases.

DLS packaging technology in Seiko Epson



10 layers stacked package

15

Package structure

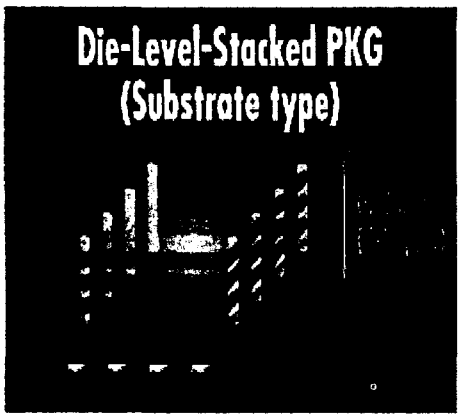
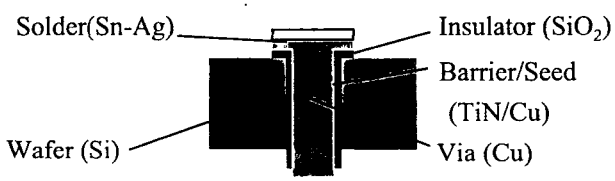


Image of Trial Package (Section View)



Structure of Through-type Electrode

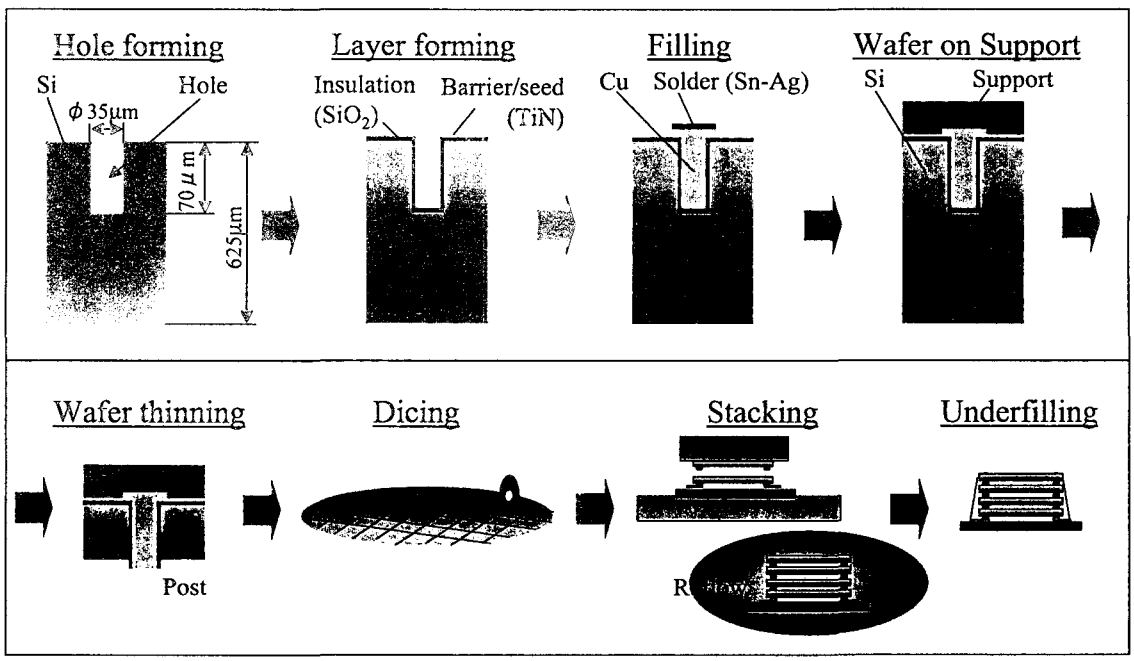
Sample Specification

Package	
Type	Substrate type
Size	5mm x 5mm
Thickness	0.65mm (typ)
Ball Pitch	0.75mm
Number of layers	4
Chip	
Thickness	50μm
I/O count	120
Via pitch	150um
Via diameter	35um

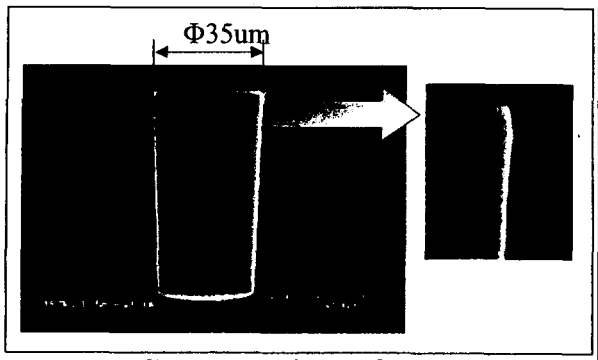
Features of DLS package in Seiko Epson

- Simple process
  - Less numbers of processes possible.
- Through type electrodes under Al pads
  - No area for vias is required.
  - No redistributing lines are required.
- Low cost

Process

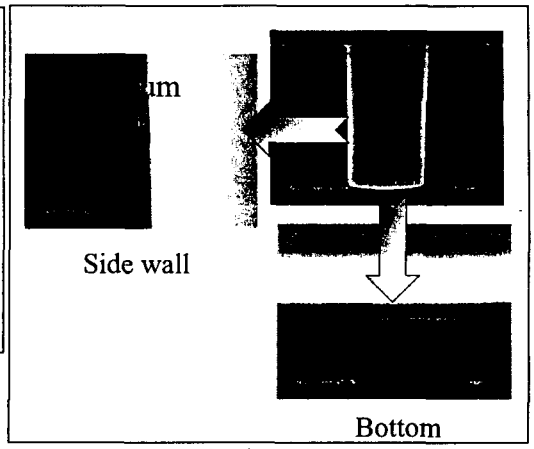


Formation of holes
Insulation and barrier/seed layer



Cross section of a via

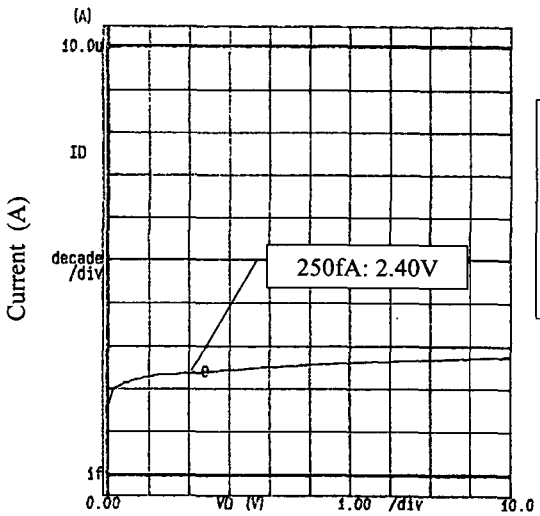
Via formation	RIE
Insulation	Plasma CVD



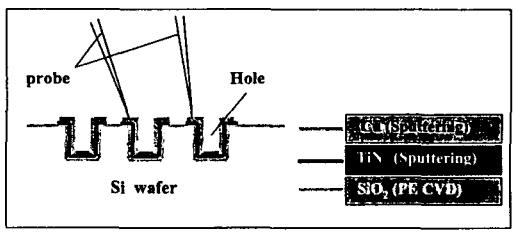
Insulation layer

- Scallop-free hole openings were achieved.
- High-speed etching was achieved.
- Adequate coverage was confirmed on sides and bottom of hole.

Leakage of Insulation Layer



Leakage of Insulation Layer



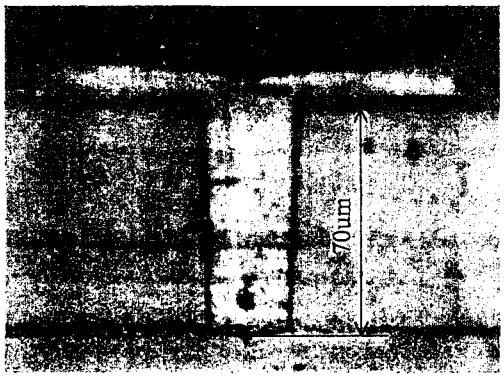
Leakage test method

- Leakage current between adjacent posts: order of several hundred (fA).

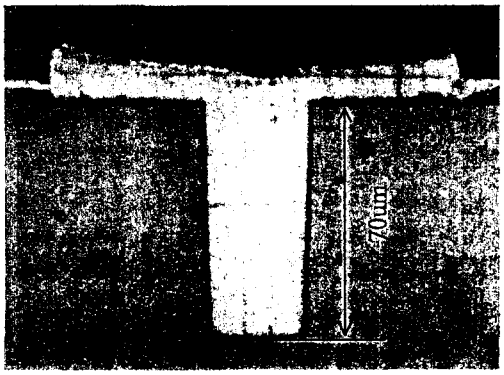
Copper plating for filling

- Filling results (6 inch wafer)
  - Φ25 to 40 um / Depth: 70 um via filling achieved
  - Filling achieved within 6-inch area (including center and edge)

Φ 25 um

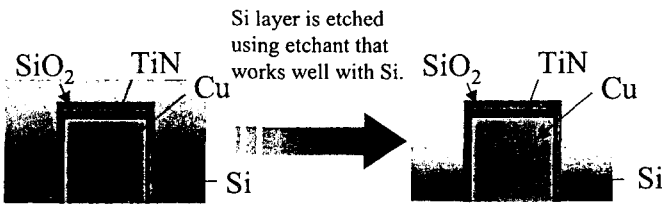


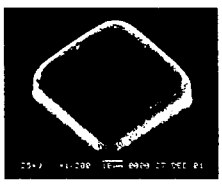
Φ 30 um



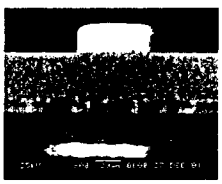
Thinning of wafer and formation of terminals on back surface

- Handling of thin wafers
  - In this case, two layers of protective tape are applied before grinding.
- Thinning and exposure of terminals
  - Back grinding
  - Spin etching





Terminals on back surface

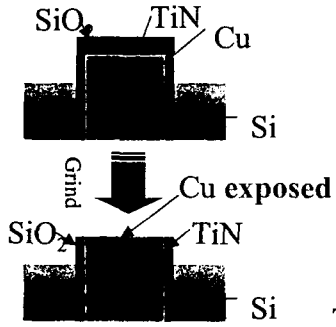


Terminals from side view

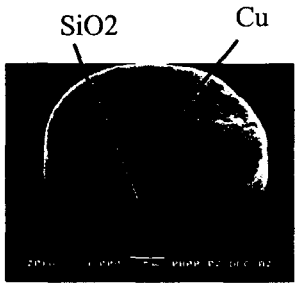
Formation of terminals on back surface

◆ Terminal polishing

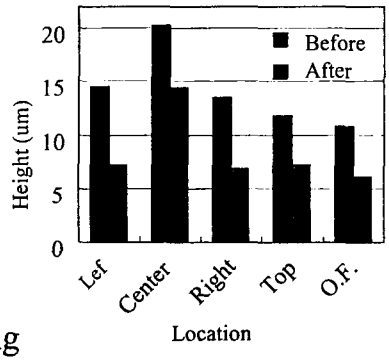
- Terminal surfaces covered with SiO2 are ground to expose copper.
- Polishing are used to form terminals.
- Copper surfaces formed by polishing were confirmed, and SiO2 was confirmed on sides.



Formation of terminals



Terminal after polishing



Post height before and after polishing

Stacking

◆Connection

- Sn-Ag is applied to terminals of active surface by plating
- Sn-Cu alloy junction
- Flux for both activation of Cu surface and pre-attachment of chips

◆Features

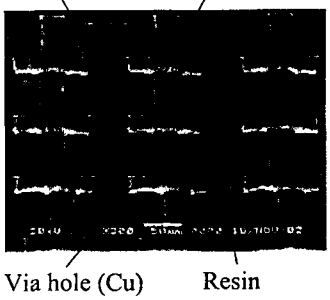
- Reflow process is available
  - No pressure
  - High productivity
- Flexibility of height differences of each terminals or chip warpage

Stacking

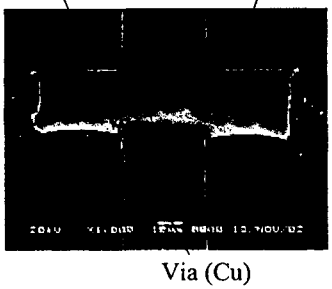
◆Stack by Reflow Process

- The reflow method starts by pre-pressing all of the chip layers, then soldering by heating the ambient temperature.
- Cu-Sn alloy confirmed at junctions

4 layers stacked package



Cross-section view



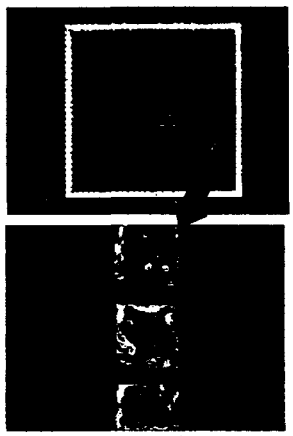
Cross-section view of junction

Cleaning and Molding

◆Cleaning Direct pass method

- Good for narrow gap
- No damage to thin chips and connections

No flux remains



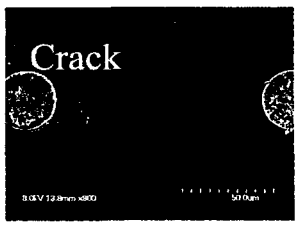
Chip surface after cleaning

◆Molding Vacuum filling method

- Adequate filling among chips

Optimization of resin is an absolute must.

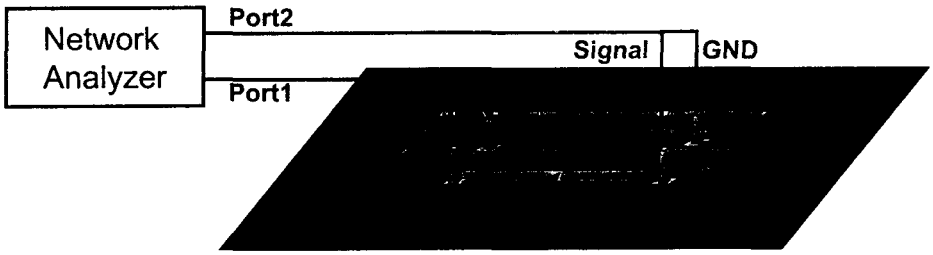
Hardening shrinkage causes crack of chip.



Chip surface after the cure

Electrical characteristics of through-type electrode

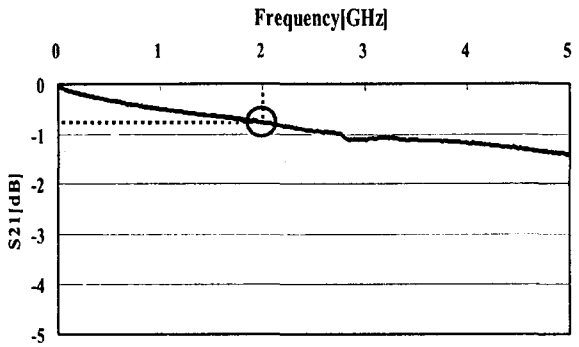
- Measurement of transmission characteristics
  - Transmission characteristics are indicated by S parameters (S21 and S12: transmission parameters)
  - Network analyzer is used for measurements

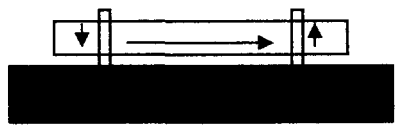


Measurement of transmission characteristics

Electrical characteristics of through-type electrode

- Measurement results
  - At 2 GHz, S21 = -0.813 dB
  - Estimated value per via is -0.4 dB or less



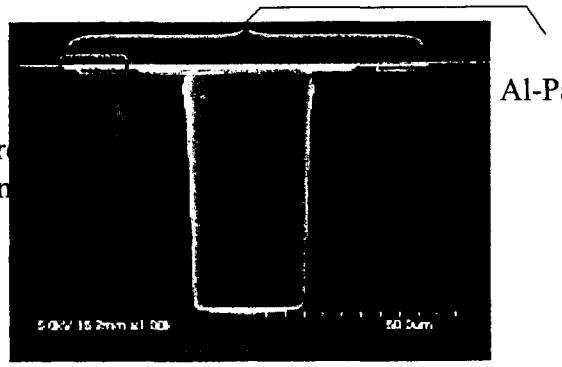


Per via
50 MHz to 5 GHz: -0.1 to -0.7 [dB]

Transmission characteristics measurement results

Testing of wafers after circuit formation

- Effects of process on transistors
  - Transistor operations were confirmed after process
- Formation of through-type electrodes under Al pads
  - Through-type electrodes can be formed under Al pads



Hole in Actual Wafer

Conclusion

- Results for trial packages in general
  - Confirmed ability to form through-type electrodes
  - Basic electrical characteristics were ascertained
- Basic technology was established
  - Formation of holes using dry process
  - Voidless copper plating and filling
  - Wet etching and formation of posts on back surface by polishing
  - 4 layer stacking of thin chip using reflow process

Issues for the Future

- Technical issues
  - Further refine various elemental technologies
  - Confirm and ensure reliability
  - Support technologies for wafer thinning
  - Confirm and further improve high-frequency characteristics
  - KGD confirmation methods
- Other issues
  - Study new business models