Multilayer thin film technology as an Enabling technology for System-in-Package (SIP) and "Above-IC" Processing

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Abstract

The continuing scaling trend in microelectronic circuit technology has a significant impact on the different IC interconnection and packaging technologies. These latter technologies have not kept pace with the IC scaling trends, resulting in a so-called "interconnect technology gap". Multilayer thin film technology is proposed as a "bridge"-technology between the very high density IC technology and the coarse standard PCB technology. It is also a key enabling technology for the realisation of true "System-in-a-Package" (SIP) solutions, combining multiple "System-on-a-Chip" (SOC) IC's with other components and also integrating passive components in its layers.
A further step is to use this technology to realise new functionalities on top of active wafers. These additional "above-IC" processed layers may e.g. be used for low loss, high speed on chip interconnects, clock distribution circuits, efficient power/ground distribution and to realize high Q inductors on chip.

1 Introduction

According to the latest International Technology Roadmap for Semiconductors (ITRS) [1], the scaling of the smallest feature size on chips is continued unrelentingly. Figure 1 illustrates this scaling trend with respect to the on-chip lithography trends. The observed trend confirms the so-called Moore's scaling law: Moore predicted that the number of transistors on a chip would double every 12 to 18 months. With each new generation of smaller devices at the wafer level, faster operating speeds can be achieved. This has a significant impact on how packaging and interconnection technologies are conceived and realised. Sizes have to be minimised, dimensions have to be chosen specifically to match required electrical characteristics.

Another consequence of Moore's law from the IC-packaging and interconnection engineers' perspective is that, for an unchanged circuit design, the IC will become smaller and the input & output (I/O) contact pads have to be fitted on a smaller die. This results in an increased I/O-"density". In the field of circuit-design, the so-called Shannon's law, states that the circuit architecture complexity (number of gates or memory bits on a chip) grows even faster in time than Moore's scaling law. Another empirical observation, the so-called "Rent's rule", states that the number of circuit I/O's increases exponentially with increasing circuit complexity. In combination, all these trends result in a significant increase in the I/O pad density on a chip. This by itself has a big impact on the interconnect and packaging technologies for the future, as these technologies can be seen as "geometry translators": from the (sub)-µm scale on the chip to the mm scale at system level.

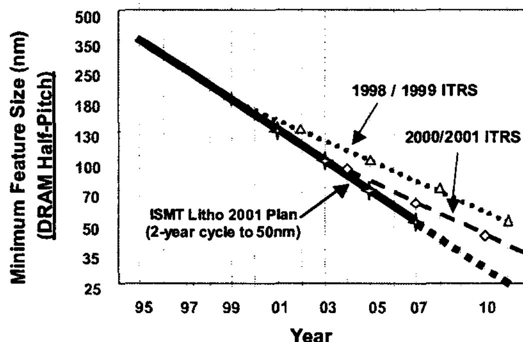

Fig. 1: Scaling trend in time of the minimum lithography dimensions, after ITRS [1].

The newest IC-technologies allow for incredibly complex circuit integration on a single die. This is often referred to as "System-on-a-chip", SOC, architectures. This approach is highly successful in integrating the major part of a system, in particular digital signal processing, on a single deep sub-micron CMOS technology. However, in most cases the SOC technology is not able to integrate the entire system on a single piece of silicon. The SOC chip still needs packaging and interconnection to other system

elements. A system (may) also consist(s) of many non-silicon parts, such as passive components, displays, sensors, antennas, connectors... Furthermore, within the IC-technology there is a growing divergence between different types of technologies. Besides the "mainstream" high-density logic CMOS technology, there are many different specific technologies for memory, analog, high voltage, RF, MEMS and electro-optical circuits. It is highly unlikely that all these functions can be integrated in a cost effective fashion in a single SOC Si-technology platform.
Although SOC cannot really offer a true single chip system, it can significantly reduce the size as well as the cost of a system or sub-system. In combination with high-density interconnection and packaging techniques it enables the realisation of a so-called "System-in-a-Package", SIP. Multilayer thin-film technology is a key enabling technology for the realisation of a SIP.

2 The interconnection gap

The main interconnection technology used in industry today is the so-called printed circuit board (PCB) or printed wiring board (PWB) technology. This technology is based on the lamination of a stack of multiple interconnect circuit layers. Each layer typically consists of a double sided metallised sheet of epoxy resin-impregnated glass-fibre cloth. These "double" sided "inner" layers are individually patterned using wet etching of the copper metallisation. Both sides of the layer are connected to each other by mechanically drilled and chemically metallised holes (buried via's). Several of these inner layers, interlaced with additional isolating layers of resin impregnated glass cloths, are finally laminated together in a hot isostastic press to form the final multilayer PCB boards. The different layers in the stack are interconnected through mechanically drilled holes that are chemically metallised (through via's). Wet etching is typically used to pattern the top metal layer.
The technology described above has been the major interconnect technology for the past 30 to 40 years. Evolution towards smaller feature sizes has been rather slow compared to the scaling frenzy in IC-technology. The smallest dimensions in this technology are now in the order of 100 μm line width and spacing, drilled via holes of 200-300 μm diameter with via-contact lands of 300-400 μm diameter.
In the past 10 years, a major advance in this technology has been brought about by the use of so-called "sequential build-up" technology (SBU). In this case additional resin layers and metallic layers are applied to the PCB board, after the "stack-up" lamination process, turning the process from a parallel to a more sequential process flow. For this technology, via holes are mainly realised using laser drilling, although photosensitive dielectrics and plasma etching of holes is also used sometimes.

An overview of the currently most advance SBU technologies, under development in Asia, is shown in Figure 2 [2]. For commercial products, the smallest line-widths available today are 75 μm. Via diameters are typically larger than 50 μm, their further shrinkage is limited by the materials used, the relatively thick SBU dielectric and the metallisation techniques used, which all limit the aspect ratio of the vias in SBU to about 1. The most significant limitation is however the size of the via metallisation pad. This size is minimally 100 μm larger than the via hole size. This difference is caused by the large tolerances on PCB substrates, caused by their relatively poor dimensional stability during processing.

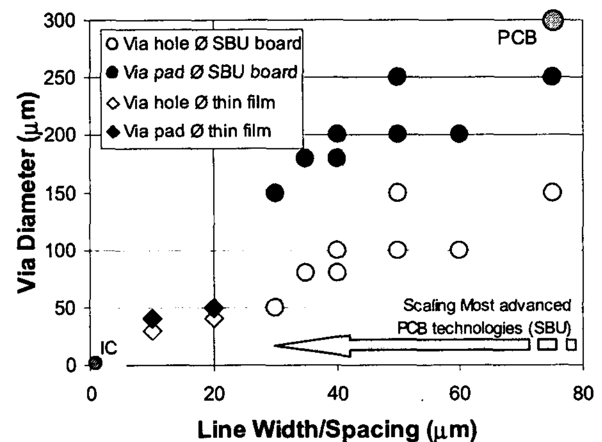

Figure 2: Illustration of the "interconnect gap" between the on-chip interconnect density and the most advanced PCB technologies, showing the scaling of minimal feature sizes of the most advanced SBU PCB technologies under development [2]. Multilayer thin-film technology is a "bridge" technology that may close this gap.

From Figure 2, it is clear that even when using the most advanced PCB SBU interconnection technologies under development, a large "interconnect gap" still exist with the on-chip interconnect technologies. Multilayer thin-film lithography based interconnection technology is required to bridge this "gap". Line widths and spaces can scale down to 5 μm dimensions, via hole diameters will be smaller than 40 μm and could be as small as 20 μm without major problems. A via metallisation pad, 10 μm larger than the via hole diameter is sufficient to account for any alignment and process tolerances. This makes thin- film lithography based interconnections an ideal bridge technology between the IC and the PCB dimensions.
The thin-film lithography based technologies are not intended for the realisation of large area interconnection boards, such as PCB's. This would result in low yield and high cost substrates. It is, however, the ideal technology for realising SIP devices, not larger in size than typically 3x3cm [3].

3 Multilayer thin-film technology

The key features of a multilayer thin-film technology are the use of wafer-like process steps and the use of thin-film planar 1-X lithography (Mask feature size is equal to the printed feature size, in contrast to reduction steppers where the features on the mask are reduced to smaller dimensons on the wafers). The basic elements of such an interconnect technology are a thin-film, high density metallisation technology and a thin-film, dielectric deposition technique, capable of realising very small via holes in the isolation layers to allow for high density interconnects between the different layers in the structure. An example of a cross-section through such a multilayer build-up is shown in Figure 3.

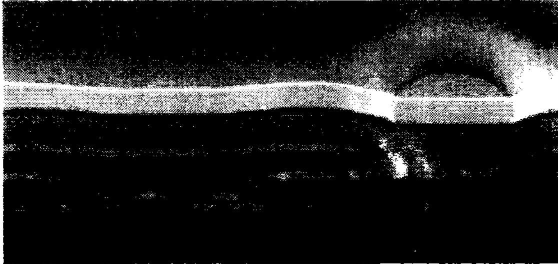

Fig.3: Cross-section through a multilayer thin-film structure, showing 2 µm thick copper conductor layers and 5 µm thick BCB dielectric layers (IMEC)

3.1 Metal interconnect lines

Different types of metals and different deposition and patterning techniques can be used. The main interconnect materials used today are Al and Cu. Deposition of the materials is typically performed using physical vapour deposition (PVD) or, in the case of Cu, by electroplating. The PVD layers are limited to thin layers of 1-2 µm; electroplating is more effective for thicker layers. Patterning is generally performed by wet chemical etching or, in the case of Cu, by semi-additive plating techniques. Wet etching has a limited resolution due to the unavoidable under-etching. Semi-additive plating has an excellent conductor width control through the use of a thick photo resist "mould". The Al metallisations can also be patterned with great accuracy by using dry etching techniques. Another metallisation technique is the use of evaporation and lift-off technology. This technology is typically used for materials that are difficult to etch on the wafer. It is also restricted to rather thin layers. A schematic comparison of the main metal deposition techniques is shown in Figure 4. For realising low resistive, high density interconnect lines, the semi-additive Cu plating technique is the preferred process. It can also be applied to other metals, such as Ni, Au, Ag and Co [4].

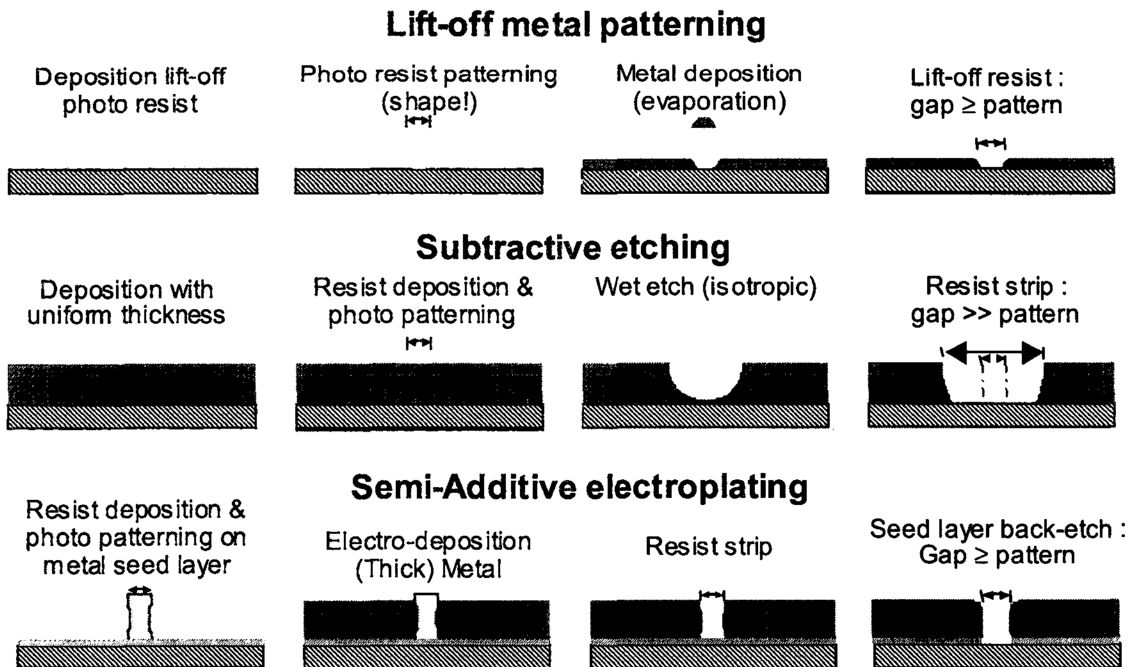

Figure 4: Process flow comparison for the main thin-film patterning and metallisation techniques. The semi-additive deposition technique results in the highest performance interconnect lines (resolution, resistance, cost).

3.2 Dielectric layers

In order to obtain a proper electrical performance of the interconnection layers, the isolation layers between the different metal interconnect layers have to be relatively thick layers, typically 5-10 µm. For good high frequency performance they also need to have a low k value. Typical dielectrics used are polymer spin-on dielectrics, such as polyimides and benzo-cyclobutene (BCB)[5]. These materials are preferably photo-sensitive, allowing for a high yield, fast, high density patterning process. Most materials available today are negative type photosensitive materials. Via openings down to 20 µm can be typically realised without specific problems.

3.3 Integration of passive components

While the on-chip integration increases, the relative area occupied by chips on boards (at the system level) is decreasing rapidly. The bottleneck for further size reduction is often determined by the size occupied on the board by passive components, such as resistors, capacitors and inductors. As a result, the integration of passive components in the interconnect and package technologies is receiving strongly increasing attention. Thin-film technology is well suited for the integration and miniaturisation of passive components. Complex materials can be deposited with high repeatability to form the highest quality resistor or capacitor layers. The thin-film lithography assures a high dimensional accuracy, enabling small tolerances and increased miniaturisation and, therefore, avoiding the need for "trimming" of resistor or capacitor values.

The electroplated copper lines, described above, are ideally suited for realising high quality inductors, particularly those required for high frequency applications. This is explained in more detail in Section 4.4.

4 Connecting high density IC's using thin-film technology

The problem of interconnecting a high I/O density IC to a standard PCB circuit board can be solved using an intermediate "interposer" substrate, schematically shown in Figure 5. The Interposer is a high-density interconnect substrate that can "translate" the on-chip fine geometries to the PCB-level coarse geometries. It also acts as a mechanical interposer, "absorbing" mechanical stresses that could occur between the die and the outside world.

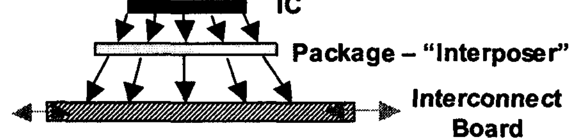

Figure 5:The package function as an "interposer" between the fine pitch chip I/O connections and the coarse pitch PCB-level contact pads

4.1 Wire bonding

The chip is typically connected to the interposer substrate by wire-bonding or flip-chip technology. As the contact pads are traditionally located around the perimeter of the die, the increasing I/O pad density on chips results in a need for a reduced I/O pad pitch. The most widely used interconnect technology used today is thermo-sonic Au wire bonding. Where a few years ago 100 µm pitch was seen as a lower limit for this technology, currently 60 µm pitch is in production and the estimates are that this technology will move down to 40 µm pitch by 2005. When using traditional PCB substrates, such small pitches cannot be maintained on the substrate side. This inevitably results in long interconnect wires, fanning out from the small on -chip I/O pitch to a coarse package-level pitch of typically 200 µm or more. Multiple rows of pads have to be used on the package level in order to avoid too large packages.

4.2 Flip chip technology

One way to overcome the wire-bond problems is the use of flip chip bumping technology. When directly bumping of the IC to the interposer is /foreseen, a flip chip bump pitch on the substrate, down to 40 µm, has to be envisaged. This cannot be achieved by SBU PCB technologies, but is well within the capabilities of thin-film lithography. As an example, in Figure 6 a thin-film on laminate technology is shown [6-8].

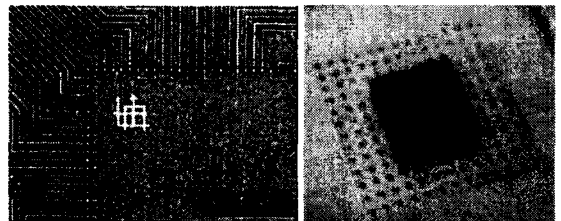

Figure 6: Example of a "thin-film on laminate" interposer substrate. Left: substrate detail showing 60 µm flip chip pads; Right: flip chip mounted die on laminate substrate (chip size = 5x5 mm). [8]

The thin-film technology can also be applied on the silicon wafer itself for rearranging the bond pads in a more sparse area array format. This redistribution

process is often referred to as a "wafer level packaging", WLP, technology. The cross section of such a thin-film build-up is shown in Figure 7. An application example is shown in Figure 8. The typical redistributed flip chip bump pitches will be 100 to 250 μm.

For a die with a low I/O density, such as memory die, this can result in a significantly larger pitch of 500 to 800 μm. In that case, preformed solder balls can be applied directly on the wafer, resulting in a truly "chip sized package" CSP that can be mounted directly on standard PCB boards.

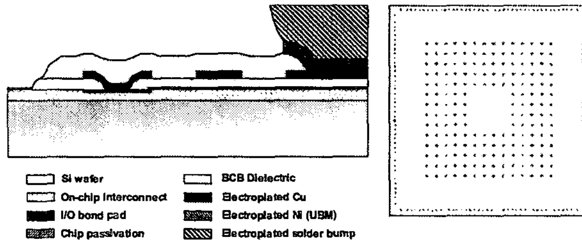

Figure 7: Thin-film interconnect pattern on chip, used for the "redistribution" op the peripheral I/O contact pads into an area array configuration. Left: schematic cross section, Right: typical redistribution layout.

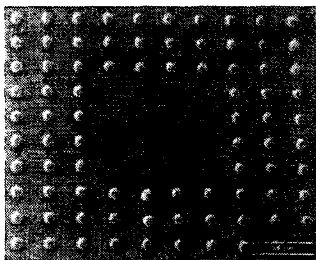

Figure 8: Photograph of a "redistributed" array of flip chip bumps on a Si-chip.

4.3 Multi chip modules

When using a thin-film interposer substrate, multiple die can be attached to the interposer substrate, using the high-density interconnection capabilities of the multilayer thin-film technology. An example of such a high density, high speed interconnect technology, developed at IMEC, is shown in Figures 9 and 10.

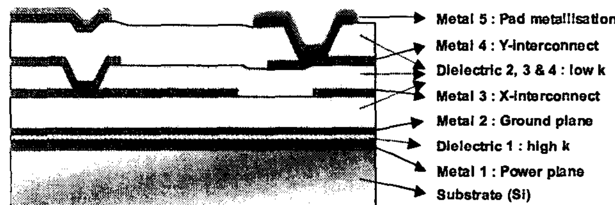

Fig.9: Schematic cross-section of a typical MCM-D interconnect module.[9-11]

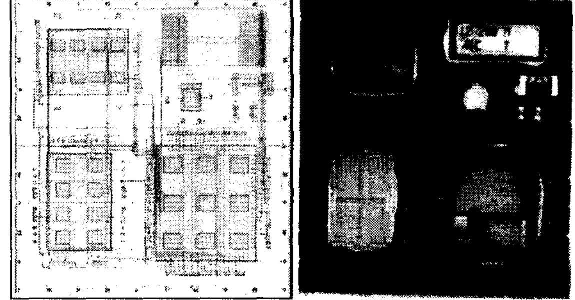

Fig.10: Example of an MCM-D module, measuring 2.5 x 2.5 cm. In this case, the chips are connected to the substrate using wire bonding. Left: interconnect layout substrate; Right: finished module. [11]

This technology is also referred to as MCM-D technology (D from deposited dielectric). Very high interconnect densities can be achieved using this approach. The typical build up consists of 5 metal and 4 dielectric layers. Power and ground planes are used to provide a good reference to the signal interconnect lines on the X- and Y-interconnect planes. The typical width and spacing of these interconnect lines is 10 to 20 μm. These layers are routed perpendicularly to each other, in order to minimise the electric coupling between the lines. Between the power and ground planes, a thin high k dielectric is used to integrate a large value decoupling capacitor (up to 1 nF/mm^2). The other dielectric layers use low k dielectrics with a typical thickness of 5 to 10 μm per layer. [3, 9-11]

One disadvantage of this technique is the requirement for additional packaging of the thin-film substrate. One approach that is under development at IMEC is the realisation of the multilayer thin-film technology on top of a laminate interconnect substrate, similar to the thin-film on laminate interposer technology shown in Figure 6. [6]

4.4 Integrated passives

Electronic systems also contain many non IC-components. Most prominent are the many resistor, capacitor and inductor passive components seen in most systems. Also these components do not shrink as fast as the IC-technology, resulting in their relative increased use of substrate area. In particular for high frequency circuits, integration of passive components can lead to a significant size reduction as well as to an improvement in performance. An example of an RF-MCM-D technology with integrated passives, developed at IMEC, is shown in Figure 11. Some application examples are shown in Figure 12. [12-16].

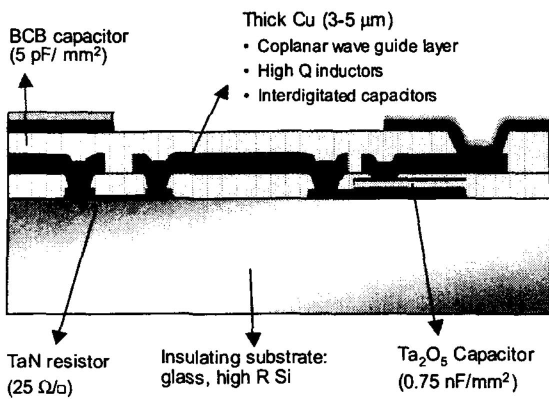

Fig.11: Schematic cross-section of an RF-MCM-D interconnect module with integrated passives as developed by IMEC. [16]

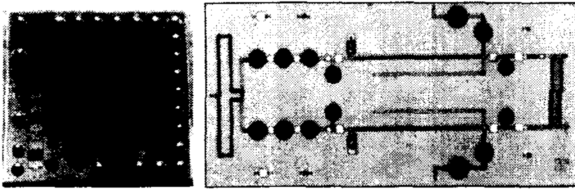

Figure 12: Examples of RF-MCM-D modules. Left: RF-section of a wireless front-end circuit showing a flip chip RF-chip on an glass RF-MCM-D substrate with 300 µm solder balls (CSP) for mounting on a PCB board (size = 7x7 mm); Right: Sub harmonic QPSK modulator at 7/14 GHz (size=8x17 mm). [16]

5 "Above-IC" processing

The flip-chip technology discussed above, in section 4.2, is performed on top of active silicon waters. The flip-chip redistribution layers, can also be considered an extension of the on-chip wiring layers. This "above-IC" technology allows for the realization of lines that are only 5 µm wide, 5 µm spaced and 5 µm thick. Though small for traditional package and interconnect technologies, these lines are very "fat" compared to the back-end of line (BEOL) interconnect layers and therefore less resistive. The MCM and integrated passives technologies described in 4.3. and 4.4. can be downscaled easily applied "above-IC", rather than on an intermediate substrate. This opens potential applications of these layers for realizing high-Q on chip Inductors, low resistance power and ground supply lines and fast on-chip interconnect lines.

5.1 High-Q on-chip inductors

For many high frequency rf-IC's, the poor quality factors of regular on-chip inductors is a limiting factor. This is due to the relatively high sheet resistance of the on-chip metallization and the losses in the semi-conducting silicon substrate. By placing the spiral inductor in the redistribution layer, the distance between the spiral and the lossy substrate is greatly increased. By using a thicker, electroplated Cu conductor, a much lower track resistance is obtained. A FIB cross-section of such an Inductor process is shown in figure 13. In this case a 10 µm thick copper layer and a 12 µm thick dielectric is used. Inductors with Q-factors above 30 up to 5 GHz where obtained over 20Ωcm Si CMOS wafers.[17]

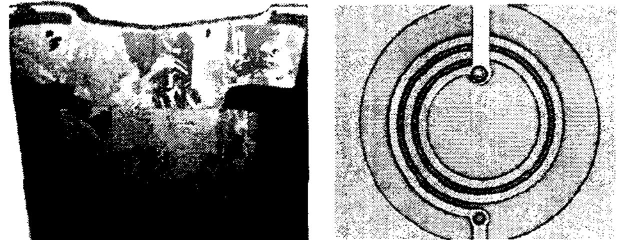

Figure 13: High-Q, 10µm thick Cu inductor processed on top of a CMOS wafer. Left : cross section contact inductor, Right : top view.

5.2 Fast on chip electrical wiring

The resistance of the electrical wires on the redistribution layer can be a factor 20 lower than the resistance of lines in the BEOL layers of the die. At the same time, the capacitance per unit length of these lines will not be significantly different, as they are basically "scaled-up" versions of the BEOL interconnect layers and also use low-k dielectric materials. The RC-delay of these "above-IC" lines will thus be more than an order of magnitude smaller than the on-chip interconnects.

Obviously, to be practical, two interconnect planes with perpendicularly routed interconnect lines will be required. As the wiring pitch on these layers will only go down to some 10 µm, the available wiring density will be relatively limited. This should however not be considered as a severe limitation for their applicability as they are only intended to be used for the longest global nets on the chip, such as interconnect lines between functional blocks on the die or lines distributing the clock circuit with high quality across the die.

The "above-IC" routing technology can be considered a "down-scaled" version of thin film multi-chip (MCM-D) technologies as they were proposed in the 90's and shown in figures 9 and 10. Many of the techniques developed for these technologies can be used for on-chip electrical connections. One example is shown in figure 14. In this approach, first a parallel power and ground plane are realized on top of the chip passivation. These planes form an integrated decoupling capacitor

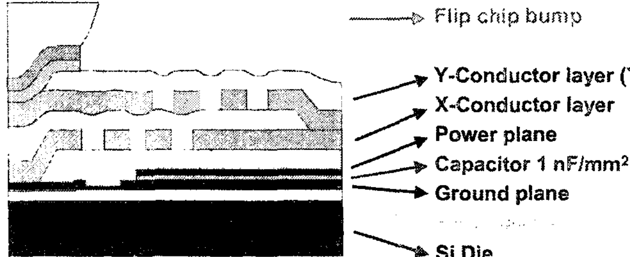

Figure 14 : Schematic cross-section "above-IC" processed interconnect layers.

(up to 1 nF/mm^2), a low resistive and inductive on-chip power and ground supply and provide a well-defined reference for the interconnect lines that are realized in two subsequent routing. This approach requires eight mask steps.

The interconnect lines in such a structure behave as lossy transmission lines.[9] These lines have less dispersion compared to RC lines, therefore enabling a higher speed performance as signal rise times are better preserved. As lines on chip are still relatively short, line termination is not required to avoid signal ringing up to high signal speeds. If the line impedance is matched to the output impedance of the driving circuit, the signal delay can be minimized to the signal delay time of the rlc line.

6 Conclusion

Interconnect and packaging technology scales down much slower than IC-technology. This results in an increasingly bigger "interconnect gap" between the advanced IC-technologies and the advanced PCB technologies. Multilayer thin-film technology, using 1X photolithography, is a key enabling technology for bridging this gap and realising so-called "system-in-a-package, SIP, solutions.

The interconnect problem between the IC-level and the "coarse" PCB level is handled by using a high density SIP interposer technology as schematically shown in Figure 16. Multilayer thin-film technology is the key technology for realising such SIP devices.

The "above-IC" thin film technology used for flip chip redistribution can be considered as an integral part of the on-chip wiring hierarchy. It can also be used to realize very high-Q on-chip inductors; a low impedance power and ground supply or very fast on-chip electrical interconnects.

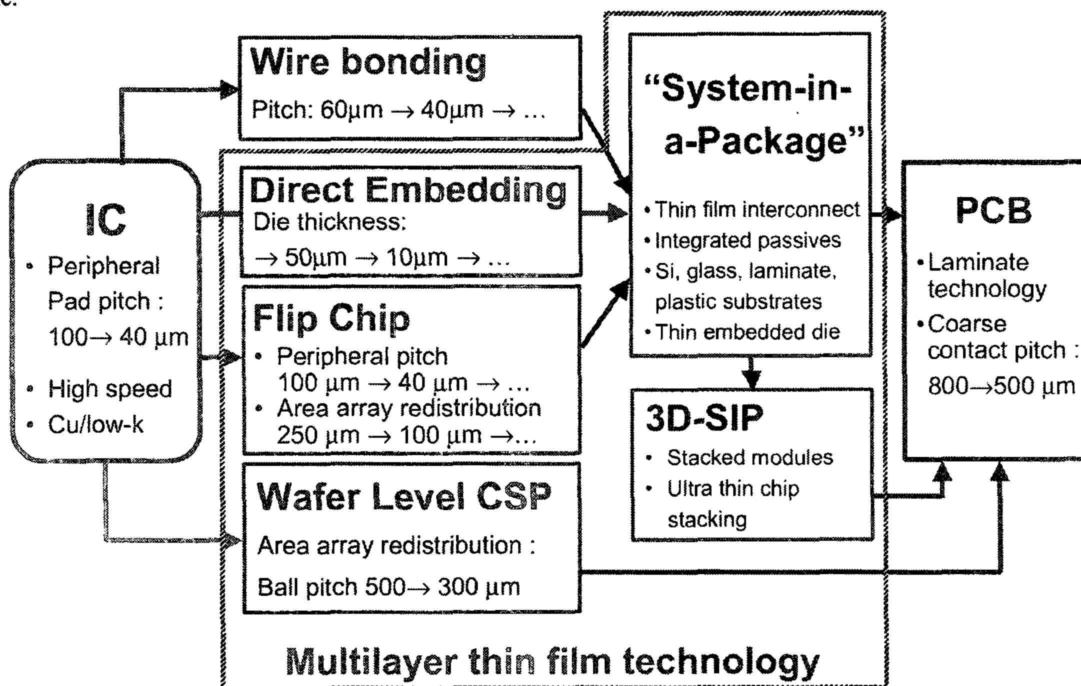

Figure 16: Schematic representation of the interconnect problem between high I/O density chips and standard laminate printed circuit boards. Multilayer thin-film technology with embedded passives is a key enabling technology for realising "System-In-a-Package"(SIP) "interposer" solutions.

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