Technologies for 3-D Assembly and Chiplevel Stack

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Abstract

Next Highly sophisticated communication generation of the Advanced Electronics and Imaging processing society will require a vast information volume and super high speed signal transport and information instruction.
This means that super high technology should be created for satisfying the demand. It's also required the high reliability of the communication system itself. It will be supported the new advanced packaging technology of the 3 Dimensional structured system and system integration technology. Here is introduced the new 3 Dimensional technology for IC and LSI packaging and Opt-electronics Packaging of ASET activity in Japan.

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Contents

1, Advanced packaging needs and Technology trend.

2, Electronic System-Integration Concept and ASET activity.

3, Research Target and its feature.

4, 3 Dimensional IC Packaging Technology R & D

5, 3D Opt-electronics Packaging Technology R &D

6, Wrap-up

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- Advanced packaging needs and Technology trend.

Technology Innovation Trend on Broadband Visual, Information and Computer Communication

Main Technology Driver

Ultra-High-speed Optical & Huge Instruction Communication

High-speed Optical Communication

PC Technology

i mode

Opt-electronics

Internet WWW

Visual Image Processing Computer

Com: Satellite Mutual Broadcasting & Seamless Communication

MS Windows

ARPA net : Ethernet

APPLE MAC

XEROX

Telecommunication innovation & Market Progress Potential Growth

1960 1970 1980 1990 2000 2010 Year →

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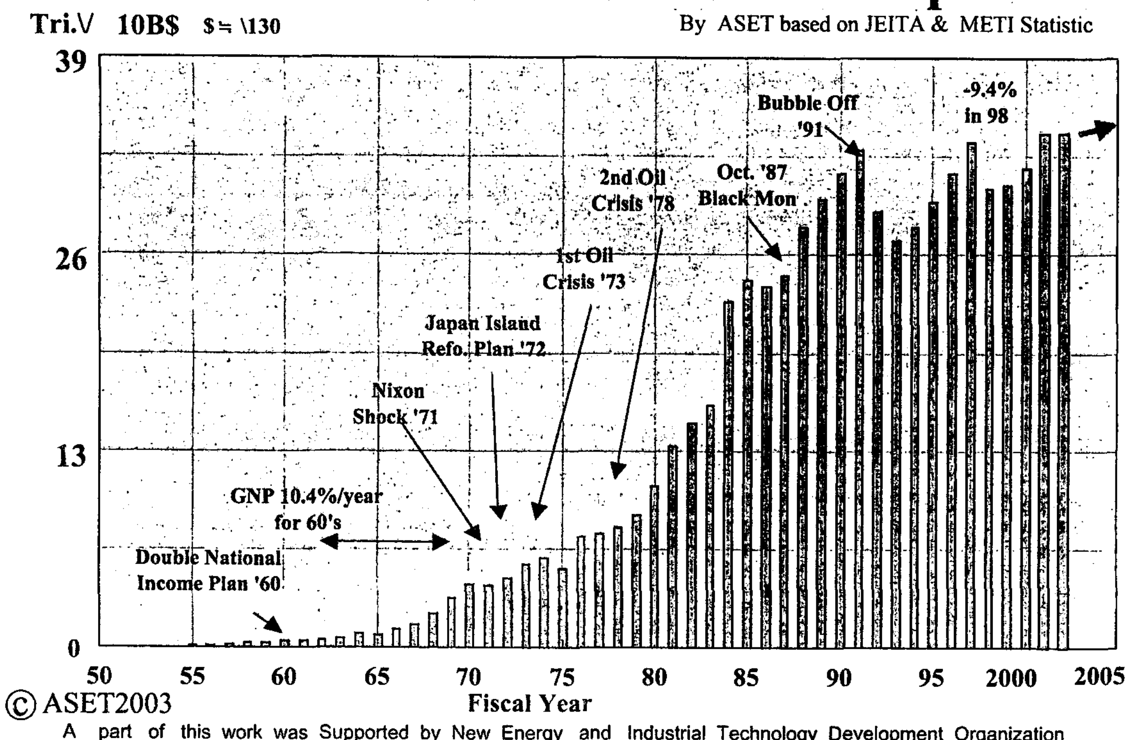
Electronics Production in Japan



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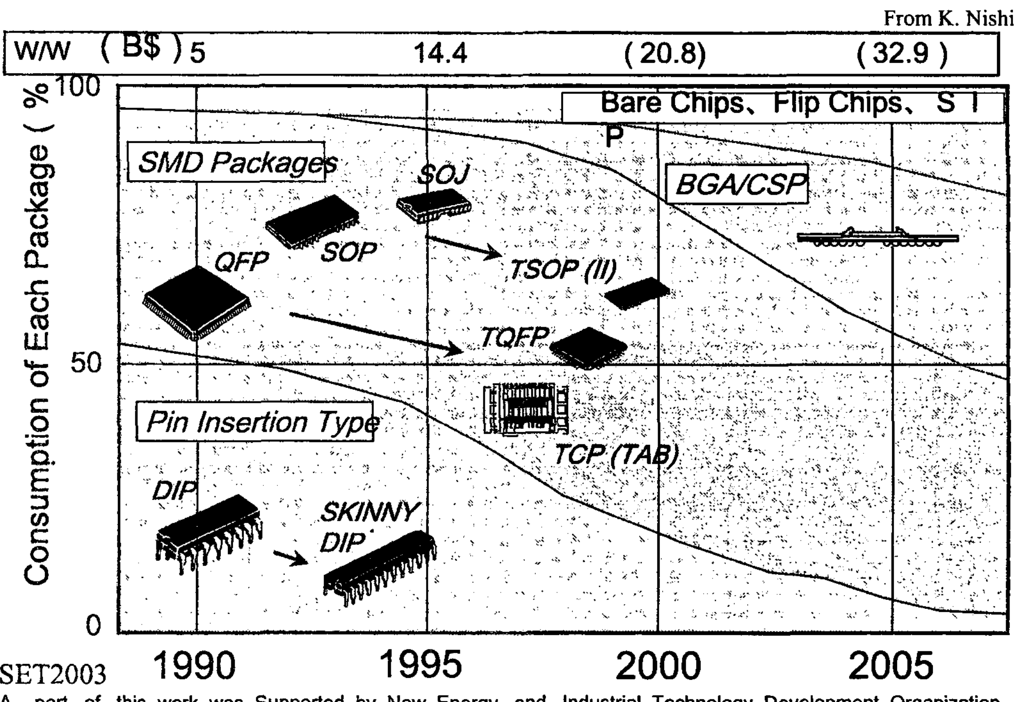
Consumption of Package Type

From K. Nishi



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Packaging Technology Trend

From K. Nishi

Smaller, Thinner, Lighter — *Systemize*

DIP QFP CSP 3D

Performance of Equipment

DIP — Audio Visual Equipment

SOJ, TSOP, SOP, TQFP, QFP — Calculator, PC, Memory Module

BGA — Mobile Phone, PC

CSP — Digital Video Camera, Digital Still Camera, Mobile Phone

SIP — Mobile Phone

1980 1985 1990 1995 2000 2005

Pin Insertion | *Surface Mount* | *Smaller and Thinner* | *Chip Scale* | *Area Array* | *System packaging*

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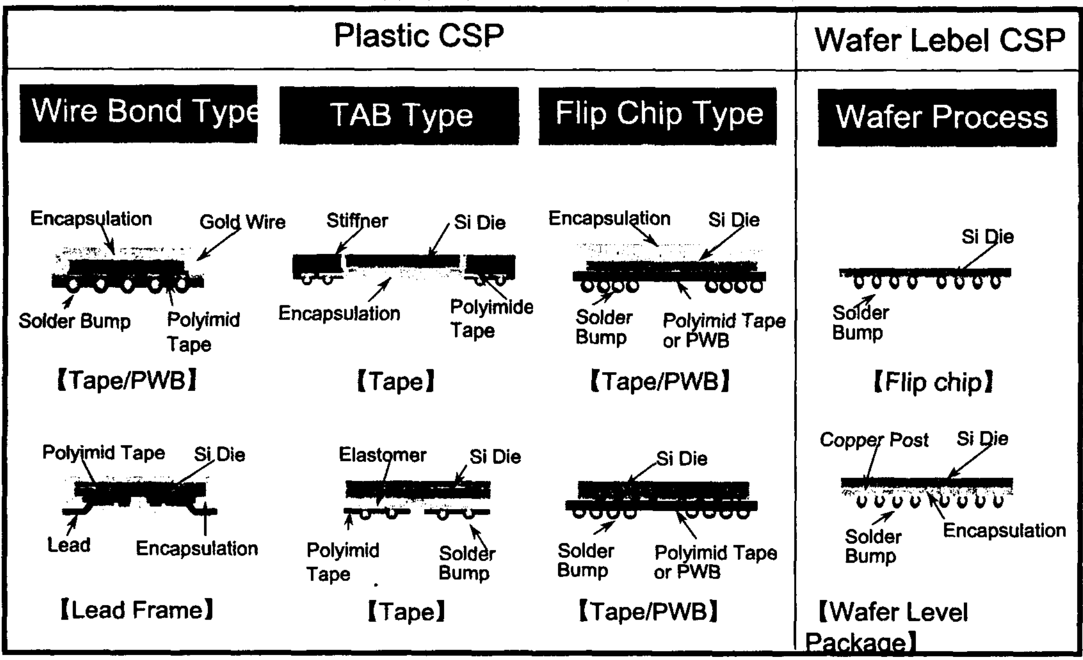
Various Types of CSPs

From K. Nishi



CSP=Chip Scale Package

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Various Types of SIP

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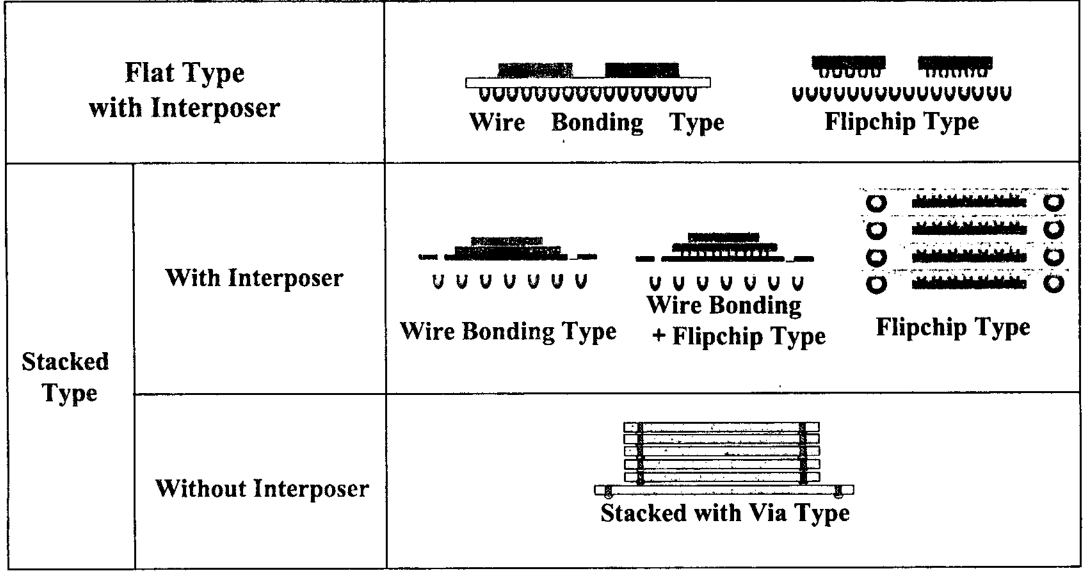

Flat Type with Interposer		Wire Bonding Type; Flipchip Type
Stacked Type	With Interposer	Wire Bonding Type; Wire Bonding + Flipchip Type; Flipchip Type
	Without Interposer	Stacked with Via Type

SIP=System in package

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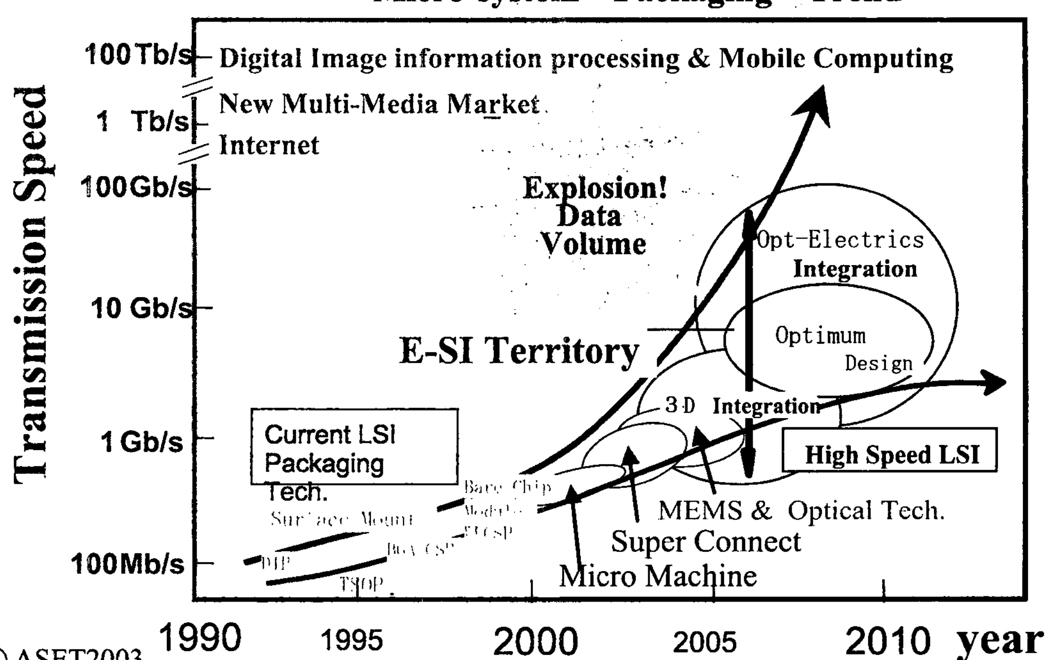
Electronic System Integration

- Micro-system Packaging Trend -



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Benchmarking of Strategic Activity

- U.S.A./E.U./S.E.A. Consortia -

	Organization	Research & Development
U S A	NIST (U.S.Depart.of Commerce)	mm wave,Laser, Opt-electronics ,Evaluation
	ARPA/ Sematech /MCC	Microelec .PKG,WLBI,CAD, Opt-interconnect .
	Georgia Tech.U.	MCM, Opt-electronics ,Packaging
	Arkansus U.	Ultra-hi-Speed-PKG Design(GHz)
	UCLA,Maryland U.	mm wave,Display, Opt-interconnect ,CAD
E U	IVF (Sweden U.)	Elec .S.I.
	ESPRIT (NETPACK,GOOD-DIE pj)	Semi-con.PKG,FC,CSP,MCM,KGD Appli ./Eval .
	Berlin Tech.U./ Izm	Elec .S.I.
	Bluetooth (Sweden)	Short-Distance Wireless Communication
	IMEC (Belgium)	LSI Design,Process,PKG,Training
S E A	IME (Singapore)	LSI Design,Process,Test,PKG
	GINTEC (Singapore)	PKG, Gov.Investing to the venture
	ITRI (Taiwan)	Semi-con.PKG to System Design & S.I.

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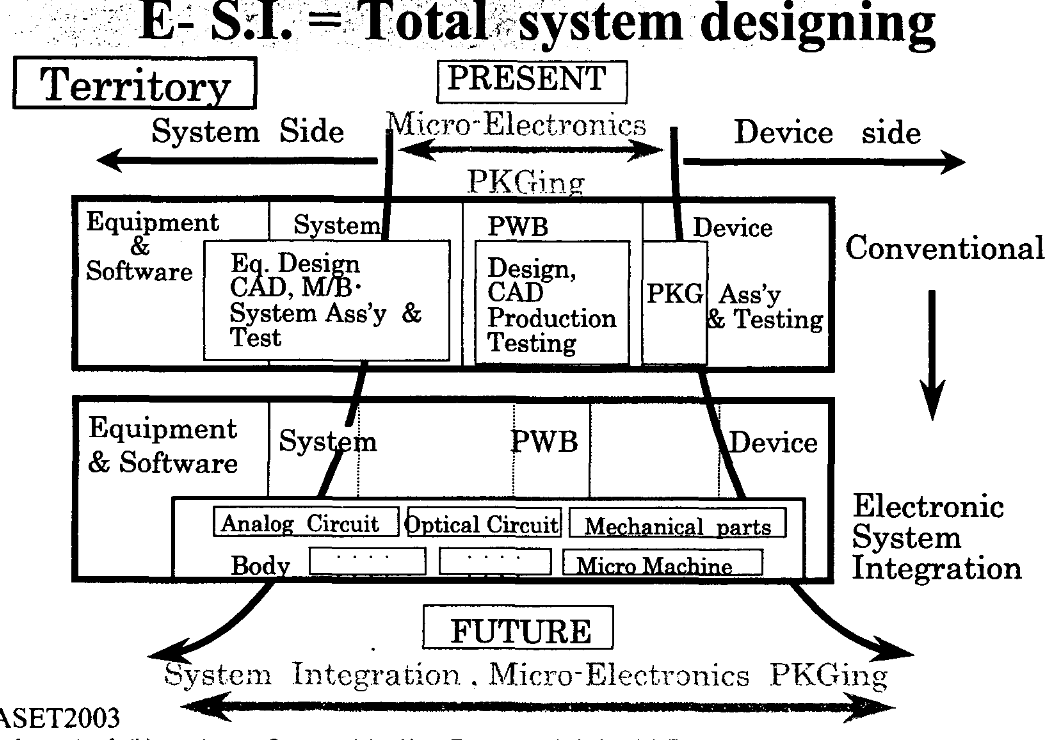
- Electronic System-Integration Concept and ASET activity .

E- S.I. = Total system designing



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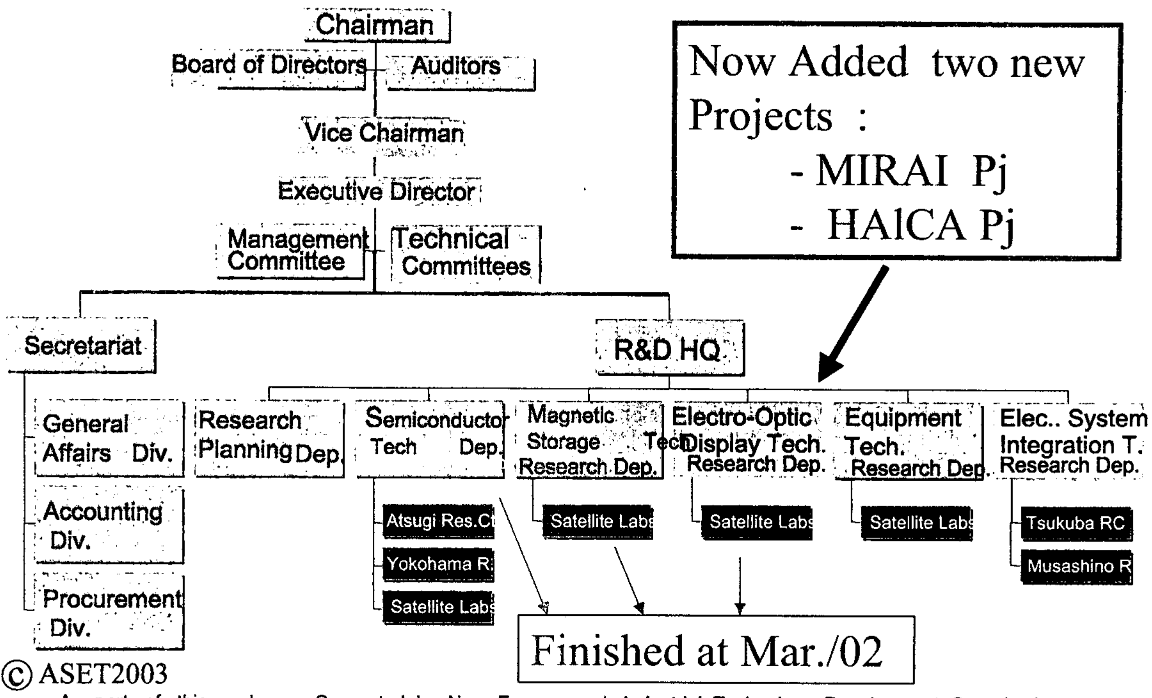
ASET Organization



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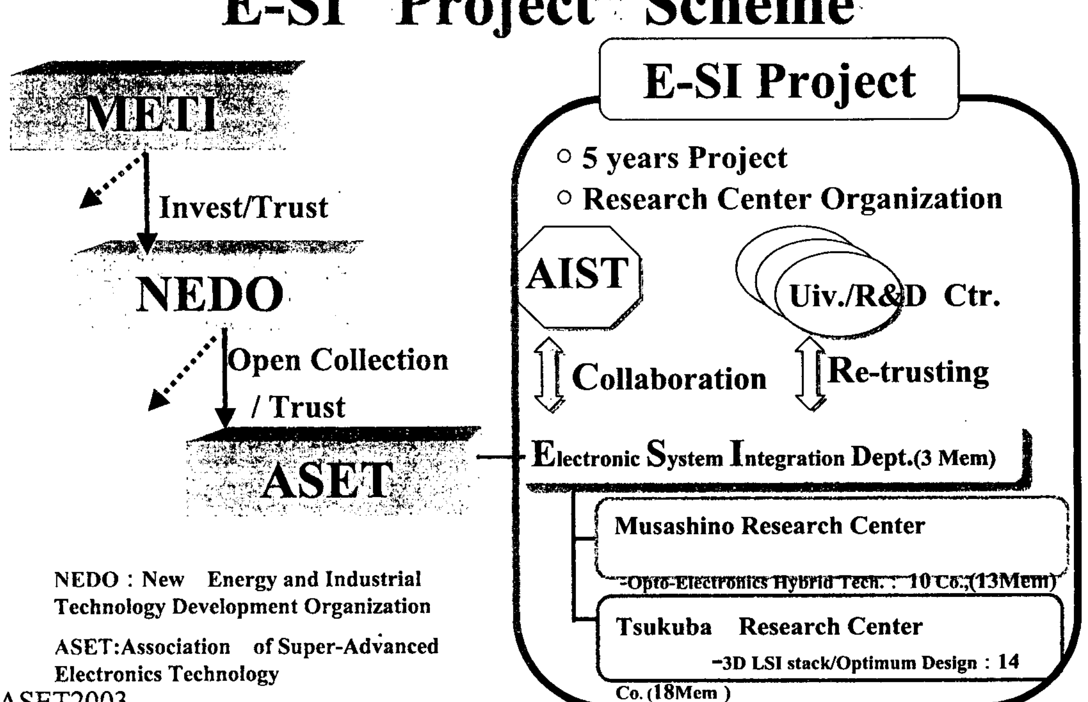
E-SI Project Scheme



NEDO : New Energy and Industrial Technology Development Organization

ASET:Association of Super-Advanced Electronics Technology

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ASET Member

April.2003

Fujitsu*	Advantest	DIC
Hitachi*	JEOL	JSR
Matsushita*	SPC	Sumitomo Chem.
Mitsubishi*	Nuflare Tech.	Mitsui Chem.
NEC*	Nikon	ASM JPN
Oki*	Ebara	Sumitomo Heavy
Sanyo*	*Komatsu*	Toyota Motor
Sharp*	TEL	Seiko Epson
Sony*	Anelva	NTT-AT*
Toshiba*	Ulvac	Denso*
Rohm*	Canon	Hitachi Cable*
SamSung Elec.	USHIO	Ibiden*
Intel	Gigaphoton	Shinko Elec.*
Obayashi	Hitachi High tech.	Taiyo Yuden*
Shimizu	Hitachi Kokusai Elec.	Toppan*
Taisei	Horiba	

* :E-S.I.

Spin out

- IBM JPN
- TI JPN
- Merck KGaA
- Merck Japan

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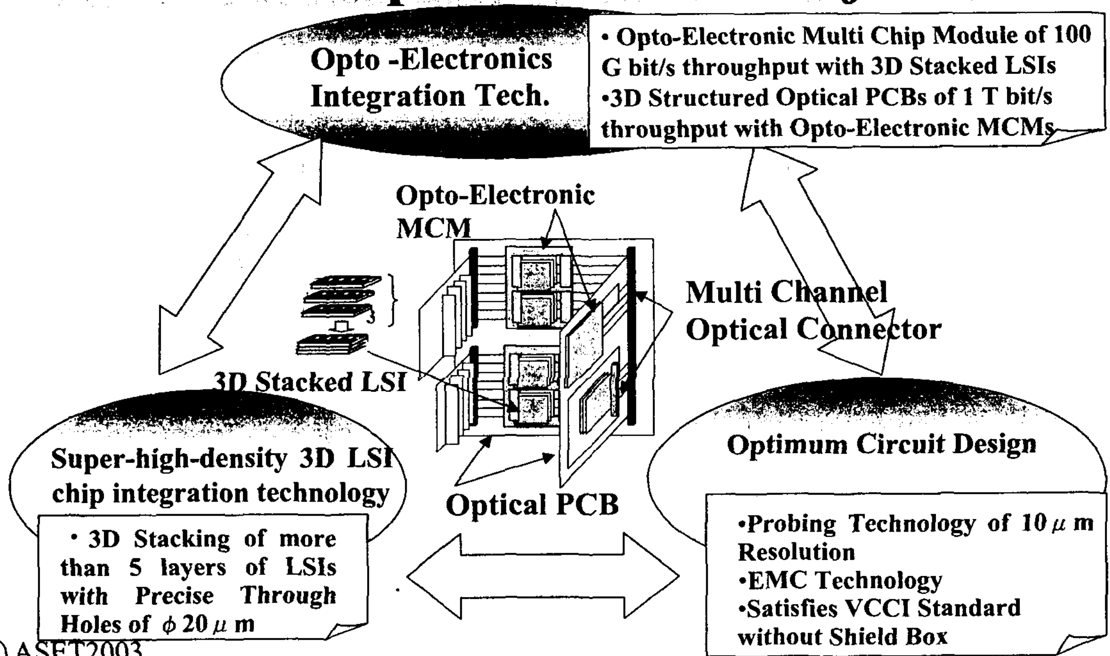
■ Research Target and its feature.

Relationship between Subjects



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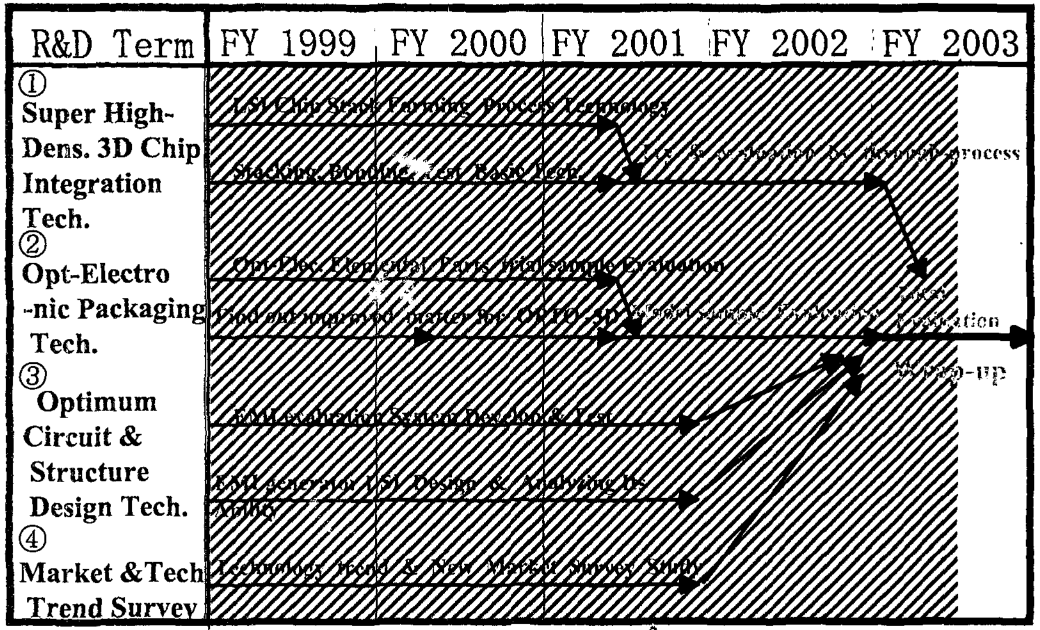
Super-high Density E-S I Researching Plan



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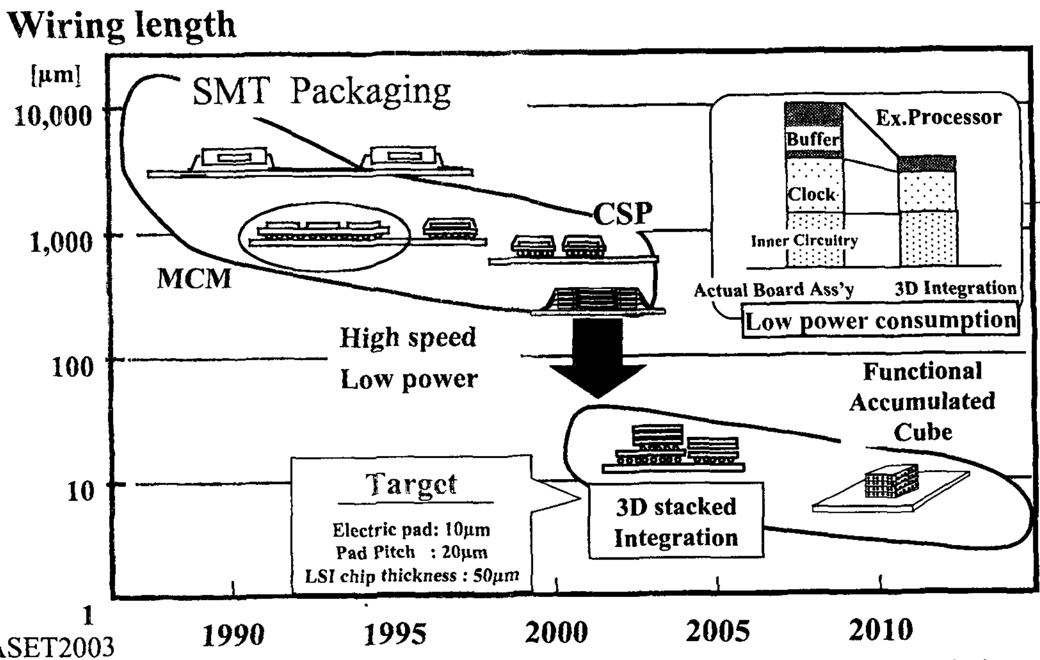
3D LSI Packaging Technology Target



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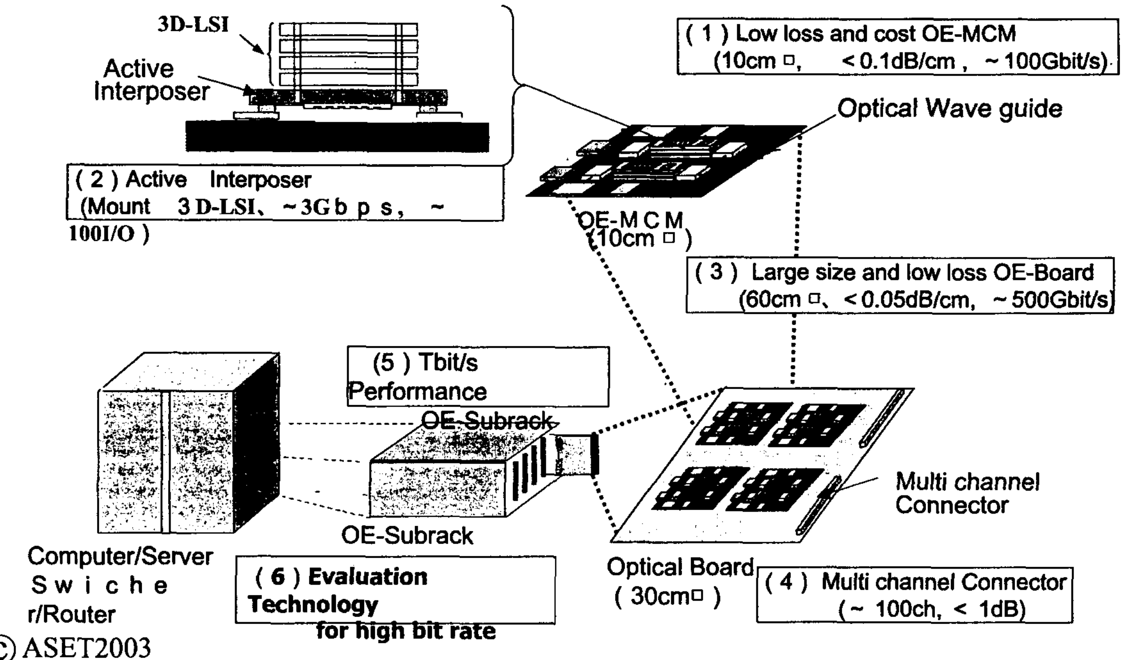
Opt-Electronics R&D Target



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Important Factors

3D Technology

Chip-Chip Distance [mm]: 100, 10, 1, 0.1, 0.01, 0.001

SOP/QFP | DIP

CSP

2D

Micromachine Center

PKG 3D

Chip 3D

Tru-Si

3D

Interconnection Pitch [μm]: 0, 20, 40, 60, 80, 100

Ultra-Fine Interconnection

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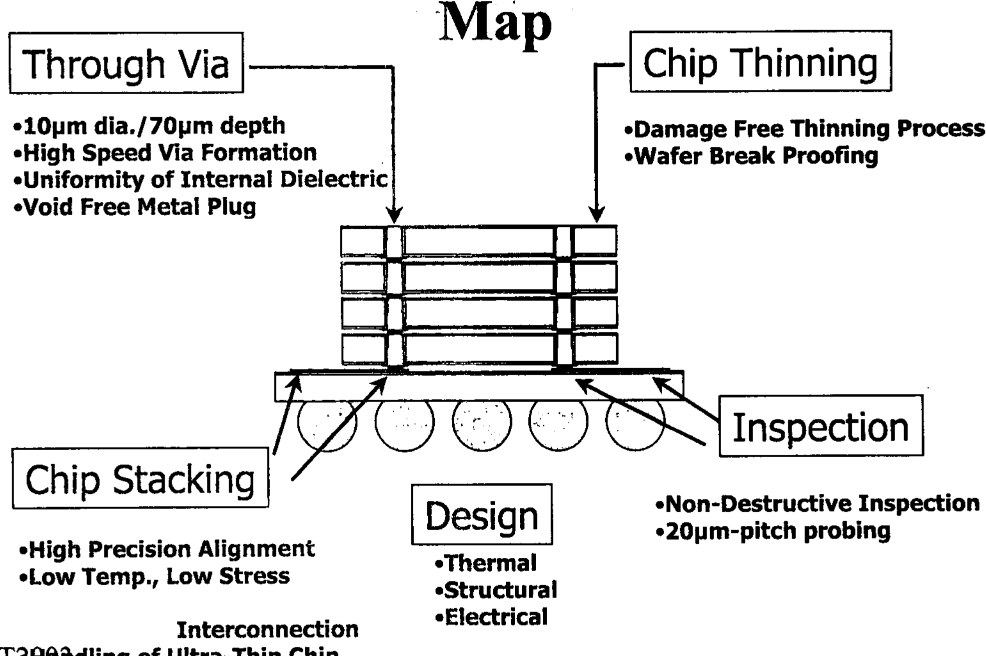
■ 3 Dimensional IC Packaging Technology R & D

3 D LSI Stacking Technology



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3D stacked LSI Via structure

Compared term	ASET	Tru-Si	Micro machine Center
Structure			
Via Pitch	20μm	? (>100μm ?)	(162.5μm) (3500via/mm²)
Chip-Chip Distance	~60μm	~60μm	~500μm
Process(Via)	RIE	ADP* (isotropic)	Electropolishing (n-type, (100))
Interconnection Method	Cu plating	Ex. Al Evp. Burried PI	Absorbing Melt metal

* ADP: Absorbed Down-stream Plasma

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3D LSI Stacked Technology Bench Marking

ASET

	3D-IC Stacked in Wafer form	3D stacked Chip stacked/thro. via	3D stacked Chip Stacked/Side Metal	3D stacked PKG Staced
Cross section view	Chip, SIO, 5μm, Si, 50μm, Via hole	Via hole, Chip, 50μ	Chip, Side Metal, 300~500μm	Interposer, Chip, Elec.Meta, 100~200μm
Stacked layer Num.	4	Min.5	4	2
Wire Length	o	o	×	×
Metal Slection	o	o	×	×
Applic-ability: Si	o	o	o	o
Applic-ability: GaAs	×	o	o	o
Applic-ability: Opt-device	×	o	o	o
Stability/Reliability	△	o	o	o
Process limitation	Have	None	None	None
Expected Yield	×	o	o	o
Challenged by	3D LSI national prj. (1981 ~ 1990)	ASET	USA Military	Many Co.

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Applic-ability: Opt-device	×	o	o	o
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Probing Technology

20μm pitch Comparison of Probe Card

Type	CanTilever	Membrane		Silicon Whisker
		Bump contact	TAB lead	
Structure	Epoxy resin Tungsten needle	Elastomer Bump LSI electrode	TAB lead	Si whisker
Surface Finish	W, ReW, BeCu	Cu/ Ni/Au, Ni Alloy	Ni Alloy	Au, Pd
Probe Manufacturing	Soldering	Photolithography		
Diameter	25～50	50～80	25～50	10～100
Minimum Pitch	40	65	40	40
Position Accuracy	±10	±5	±5	±5
Scrub Mark	15~20	1~5	20~25	1~5
20μm Advantage		No	YES	YES

Unit: μm

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Plasma CVD TEOS-SiO_2 Film

10μm

67μm

0.2μm

Barrier Metal /Seed Layer: CVD

Top

0.14μm

0.12μm

Bottom

Conformally deposited inside the via hole

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Dry Etching Process

• Purpose : Cu plug formation and grinding damage removal

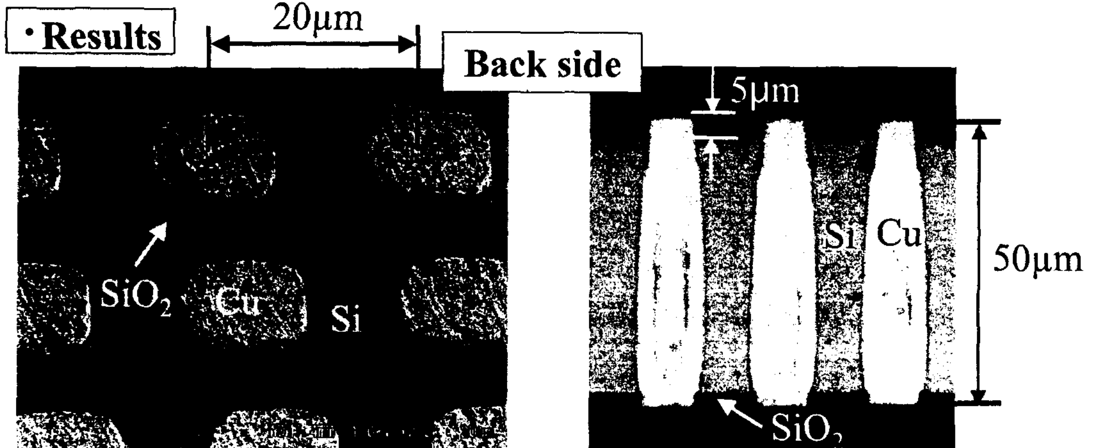

Fig. Cu plug form after back side dry etching

Cu plug formation for 20μm pitch Cu electrode

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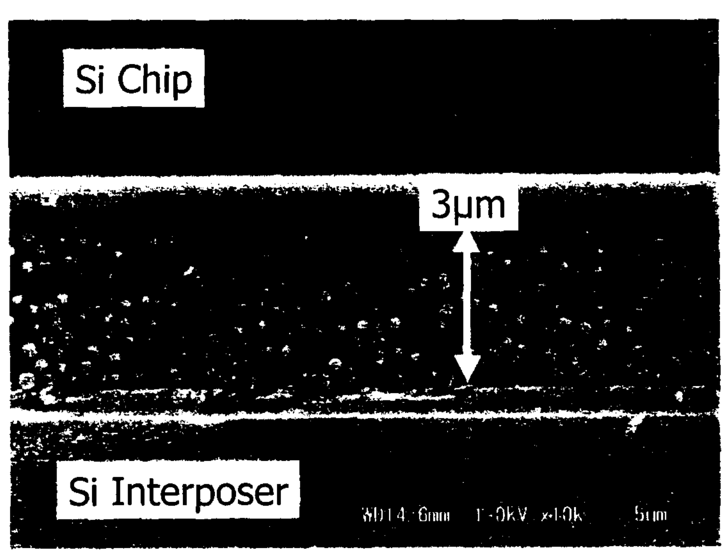
Cross-sectional View of Microthin Underfill



Cross-section of Si TEG-Interposer with Optimized-Filler Contained Resin

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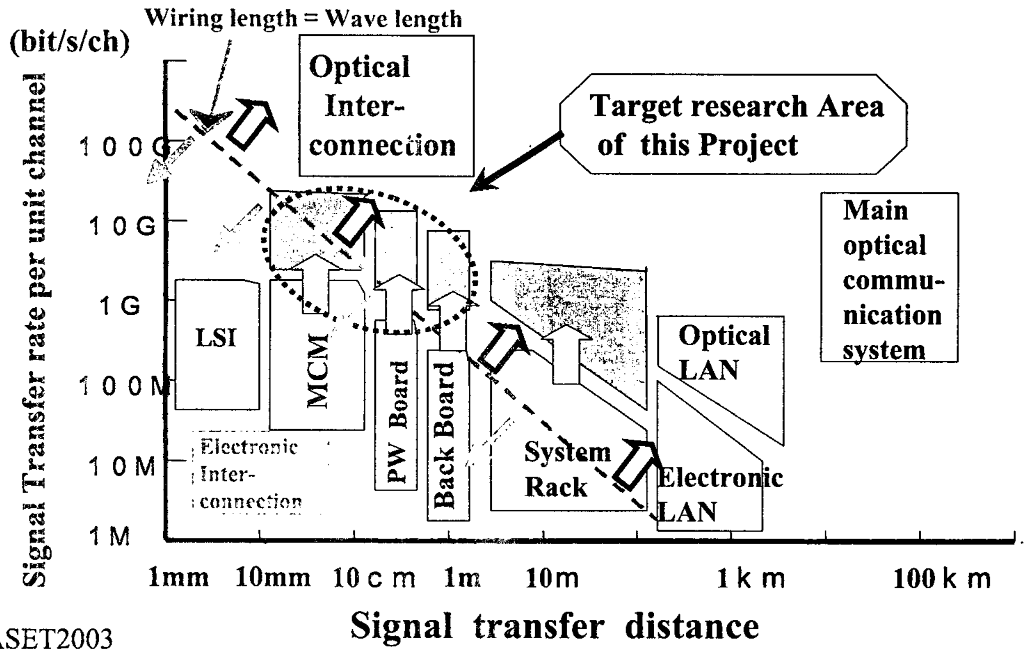
E-SI Target Opto-electro hybrid Integration



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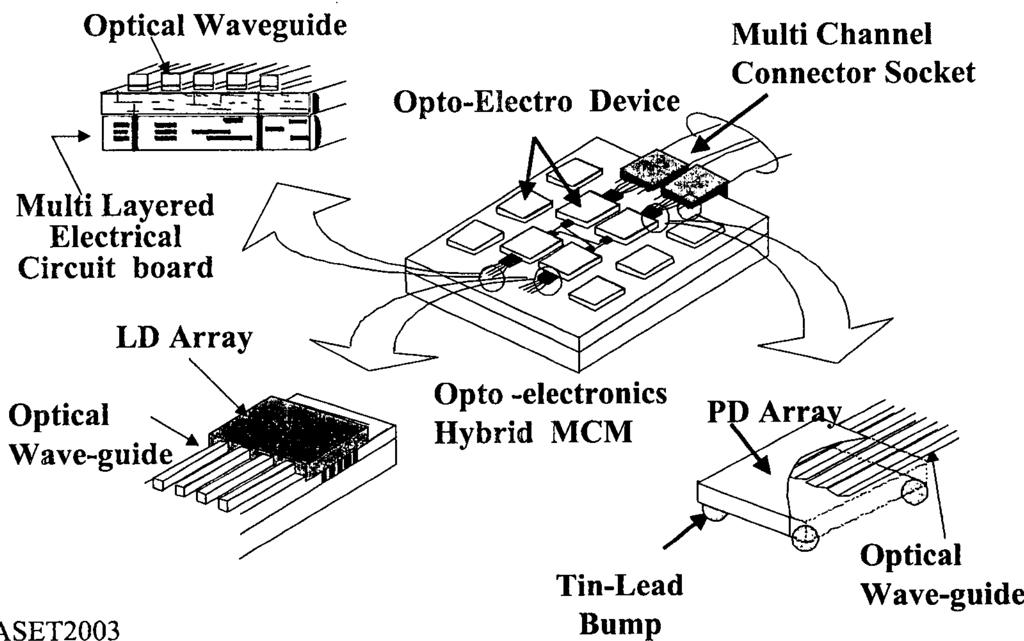
Opto-electronics MCM Technology Map



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Developments of OE-MCM

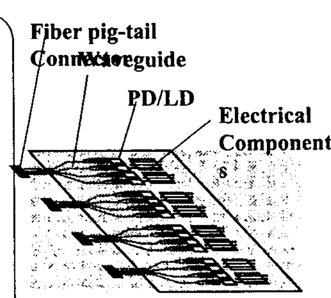
1)Trial model for OE-MCM with CWDM
Using 1.3μm Band 4λLD/PD array

2) High-precision optical alignment-free assembly
LD/PD mounting on organic substrate using the Liquid-asisted batch self-aligned assembly (AuSn→AgSn220℃)

3) OE-MCM introduced film-waveguide lamination
Alignment error 3.7μm (Ave) →Application to MM OE-MCM

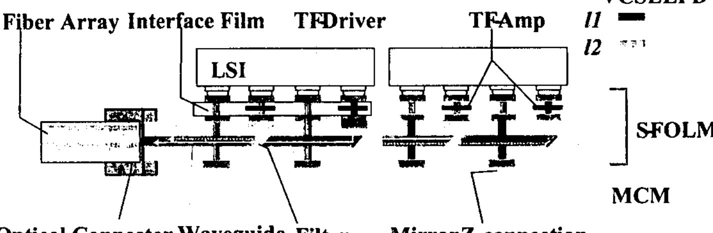
4) Waveguide using Photo-bleaching technology
Waveguide Loss of 0.6dB/cm

5) New concept of OE-MCM
Fundamental Research of Scalable film optical link MCM(SFOLM) for High-density MCM



Trial Model OE-MCM

Image of SFOLM



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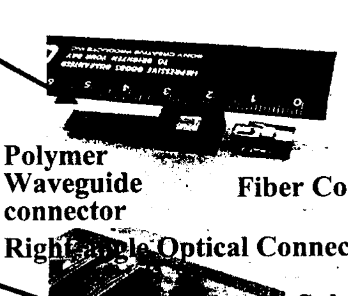
Developments of Multi Channel Connector

○Polymer Waveguide Connector for MCM
-Contact between Polymer Waveguide and fiber ferrule
-Trial connector model :8ch Polymer waveguide on Si.
Fiber connector :MT ferrule with locking fixture
-Connection Loss of 0.46dB (Ave.),
Loss increase of less than 0.56 dB after plug-in test of 100 times

○ Right-angle Optical Connector for Backplane
- Right-angle: fiber bending Radius of 10 mm
- Connector housing with Floating and Self -lock
Multi ferrule (8MT ×4 = 32ch)
-Loss < 0.5dB, Reflection >40dB(with matching oil)

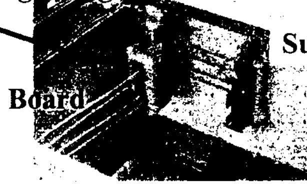
○Fiber Spring Assist Connector for Board
-Ferrule less Connector using micro spring for fiber physical contact (new type connector)
-Trial connector model :
Connector plug and Adaptor(6ch)
...dB, Reflection >38dB(without matching oil)



Polymer Waveguide connector

Fiber Connector

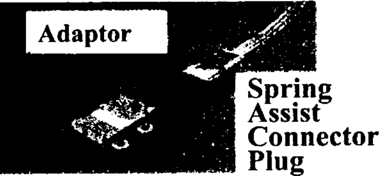
Right-angle Optical Connector



Subrack

Board

Back Plane



Spring Assist Connector Plug

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Developments of OE-Board

○Optical Fiber Board

・Fiber Board for OE-Subrack

- Assembling of newly developed, right-angled connector with small bending radius fiber.
- High density wiring design for an enormous amount of fibers (≒400) composing optical fiber board in back plane.

・High Density Wiring using High Δ and Thin Diameter Fiber

- Decrasing bending radius of wiring
  Wiring Limit:5→3mm
  Loss Limit :10→ 5mm

250 125 ⇨ 150 80

Conventional　　Thin diameter Fiber

○Fiber Coupling Using Self Written Waveguide

Less than 1dB at 0.5-mm fiber-to-fiber gap

600mm

Backplane

450mm

Optical fiber board assembled inside subrack

Optical fiber board on board

Photosensitive Resin

Fiber

UV Light

Fiber Gap 350μm

Coupling Loss dB

16 14 12 10 8 6 4 2 0

1023 480 272

Air Gap　#1 #2 #3 #4 #5 #6 #7 #8 #9 #10

UV Light Exposure Step #

Uncured Resin

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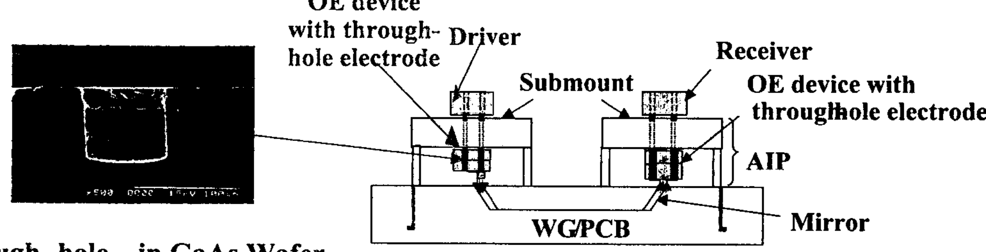
Developments of Active Interposer(AIP)

1)R&D Schedule for AIP

- Try Submount Type at the first stage, then move to ELO Type in the next stage.
- Application for MPU-to-memory data transfer

2) Submount Type AIP trial Model

- Design Submount Type AIP (Structure, Submount substrate, Assembling process)
- Processed VCSEL with through- hole electrode



Through- hole in GaAs Wafer

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Developments of 3D-OE Subrack Packaging

◇Optical Transmission Structure for Terabit perfomance

- Hybrid structure using Coarse WDM and parallel optical transmission (Example 2.5Gbps/ c h ,8λ,100ch→2T b p s)

◇Trial Model of 3D-OE Subrack

- Transmission Route : LD→MCM→ Coupler → Board →Backboard → Board → λ-Filter →MCM →PD
- OE-MCM: 2.5Gps 4λarrayed LD × 4 mounted on MCM substrate with build up Polymer waveguide (Collaborate with NTT)
- OE-board & Backplane :Optical fiber boards and Fiber bending right-angle connectors assembled on electric printed-board
- Design Total loss budget

OE-Rack Appearance

Right-angle Connector

Optical Backplane

Inner Packaging

Board

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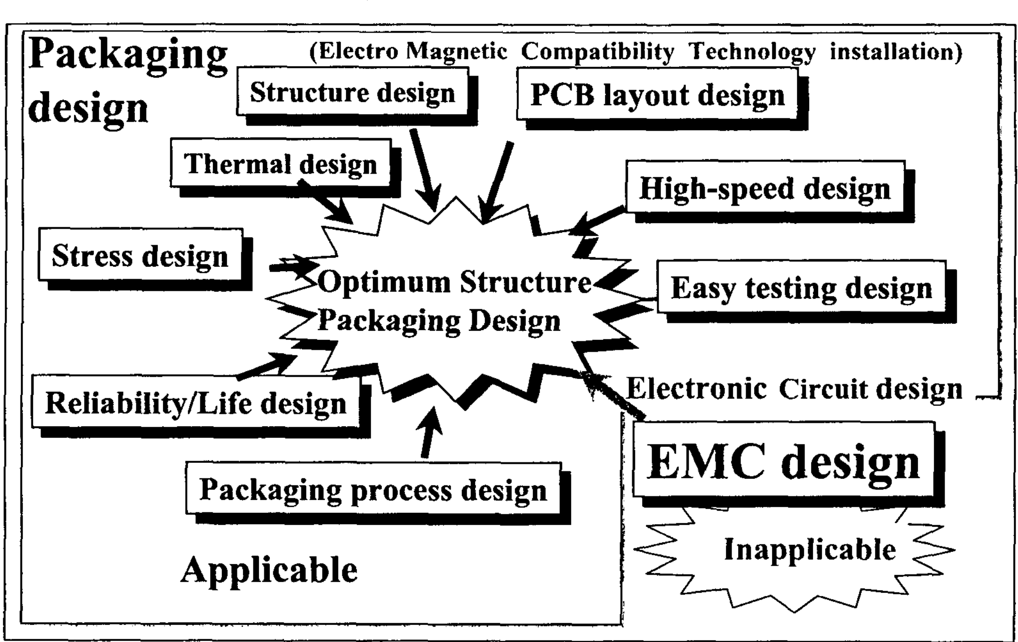
■ High-End Packaging Design Technology R &D

E-SI Key factor Technology



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Trend of Magnetic Probes

Target Region (Freq. Response & Spatial Resolution)

Frequency Region for EMC Regulation

Gerhard Mercator Univ.

Maryland Univ. DC SQUID (Each freq. component cannot be distinguish

MO device (Tokyo Univ.

NEC

PCB Type Loop Coil sensor (High sensitivity)

J.J. device (Kyushu Univ.)

MI sensor (high sensitivity)

MR、GMR sensor (Low sensitivity)

M I device (Tohoku Univ., Nagoya Univ.)

Hall effect sensor (low sensitivity)

FG sensor (High sensitivity)

MO sensor (Shimazu, Nouritsu Kaihatsu Univ.)

Neocera

SQUID Microscope (Ultra-high sens.)

IBM,SII,etc.

SQUID magnetometer (Ultra-high sensitivity)

LSI ← MCM ← PCB

Frequency Range: 1GHz, 1MHz, 1kHz, 1Hz

Spatial Resolution (μm): 1, 10, 100, 1000

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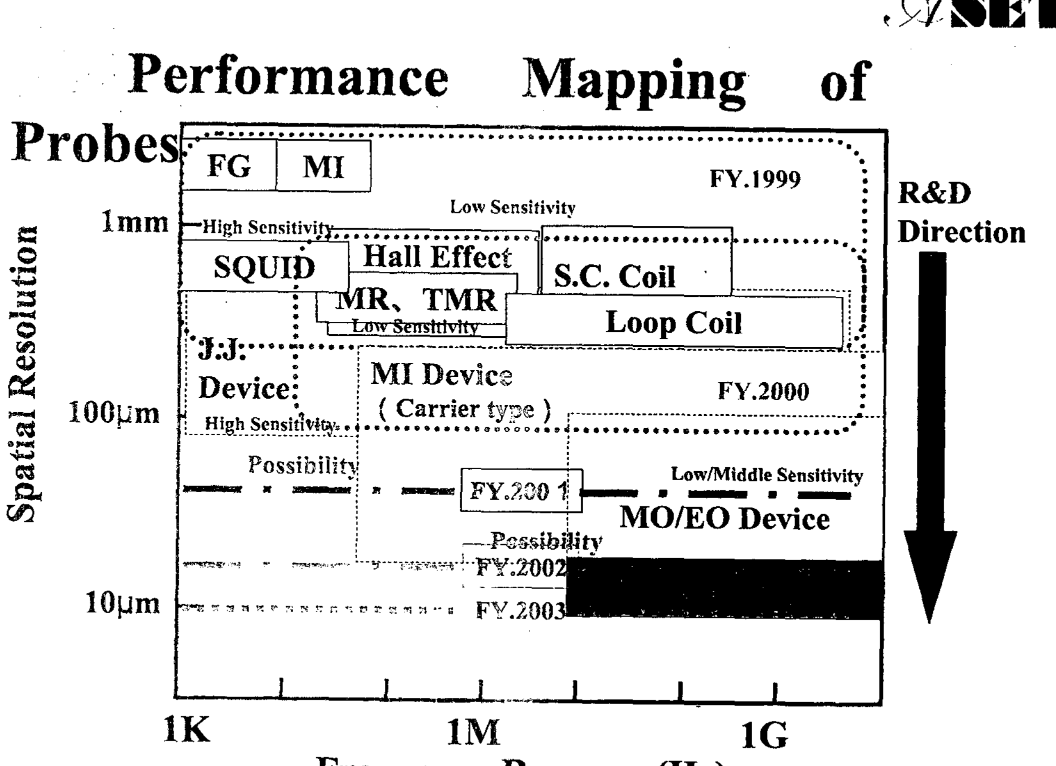

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Development of Evaluation Technology

○**Measurement System for Optical Skew and BER**

-System applying commercially-available measuring equipment

- BER measurement correspond to less than 10^{-20} within 5 minuites by Q-monitor Method

- 10-ps Optical Skew resolution between 2 channels by phase comparison

○**Optical Responses Simulation**

- New and easy simulation method for LD skew analysis with parameters extracted from DC response and step response

1
1E-10
BER 1E-20
1E-30
1E-40
0 10 20 22.0 25.3 30
Q (dB)

Relationship between values of measured Q and bit error rate

Measured
Ib = 2.4mA Ip = 2.0mA
Simulated

Simulated optical responses

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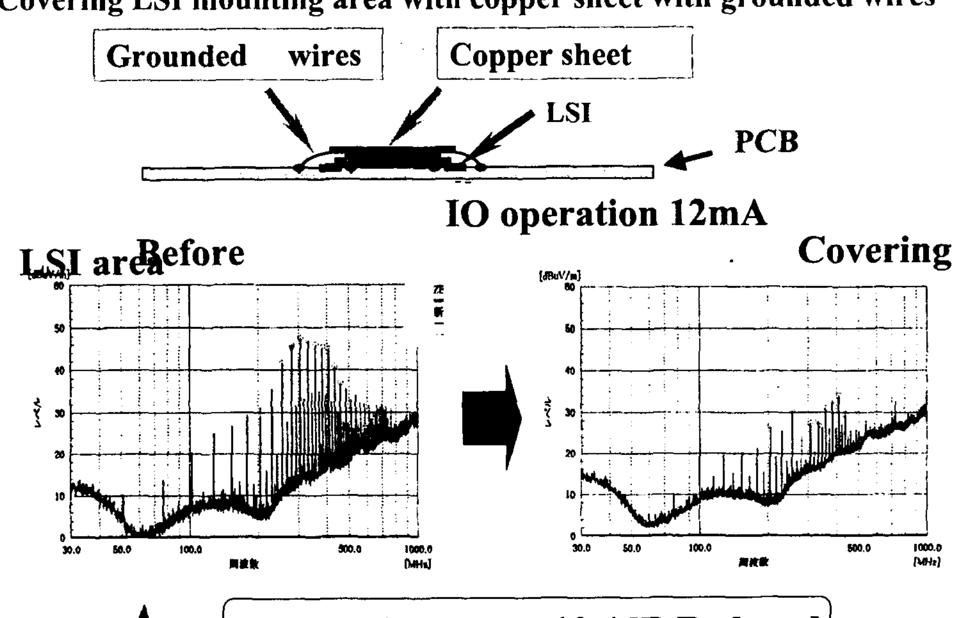
EMI Reduction on PCB with LSI -2

Covering LSI mounting area with copper sheet with grounded wires



★ **Peak Emission 13.4dB Reduced**

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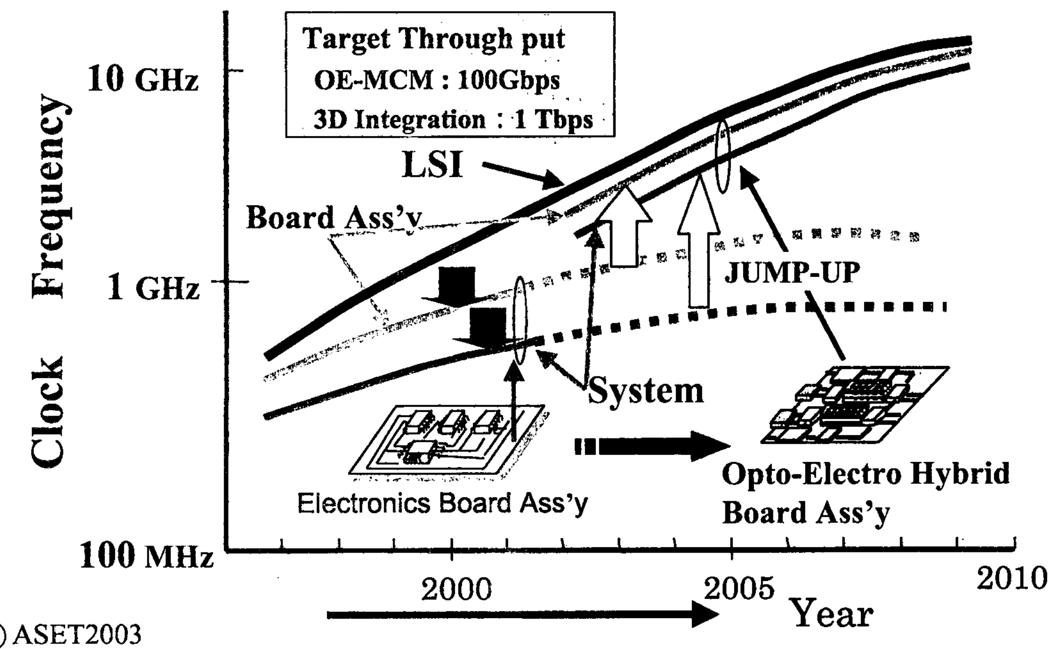
▪ Wrap-up
Opto-Electronics Hybrid Integration Effect



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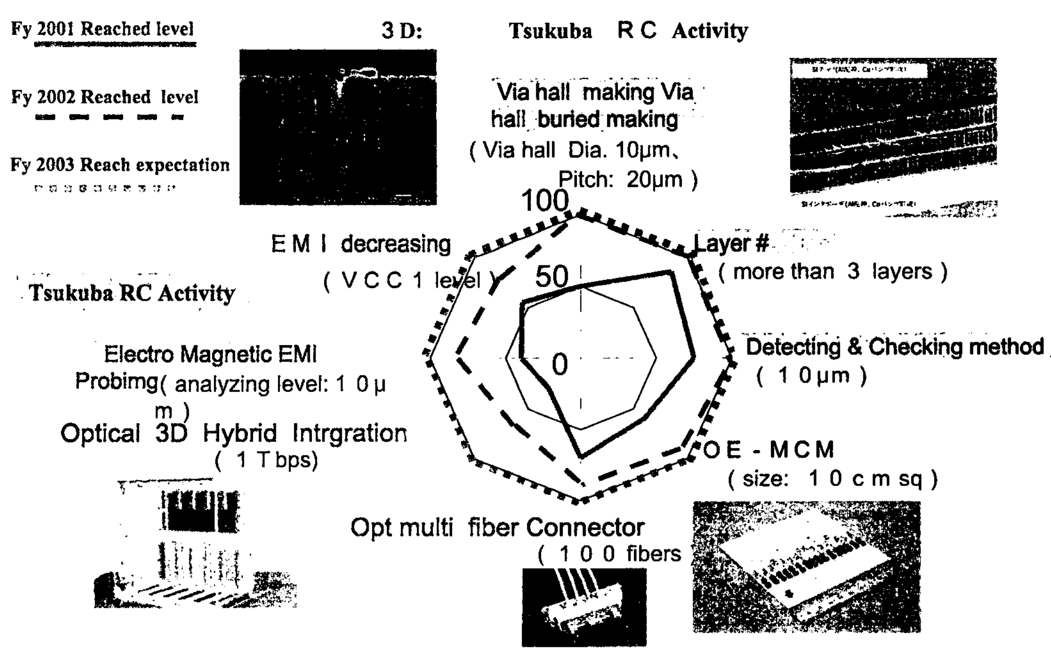
ASET Target & It's Activity Reaching Level



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System Buildup Method

	Board Mount	SoC	SiP
	PKGs, PCB	Single Chip	Chips
Pros.	• Inexpensive • Well Experienced	• Elec. Properties • Low Power	• High Density • Small Die, High Yield • Small Investment
Cons.	• Large • Slow • Power	• Large Die • Complicated Process • Scalability • Investment	• 3D Technology • Chip Compatibility • KGD

Key Technologies of SiP

- **3D Chip Preparation**
- **Wafer/Chip Thinning**
- **Ultra-Fine Interconnection**

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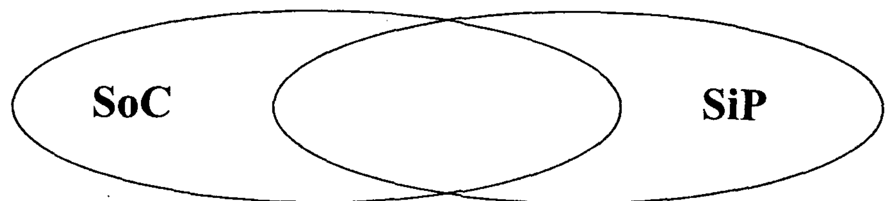
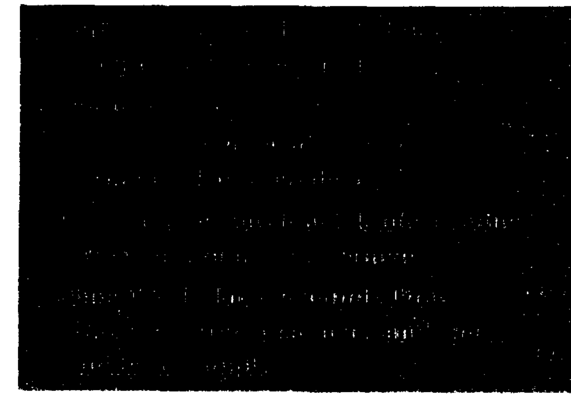
SoC & SiP



- **Resembled process LSI & Hybrid packaging**
  -Memory & Logic LSI
- ***Most Latest Process***
  - Finest patterning merit
- **Mass production/Minimum kind**
  - A big amount of product
- **Long R&D Turn around Time**
  - Next generation core product



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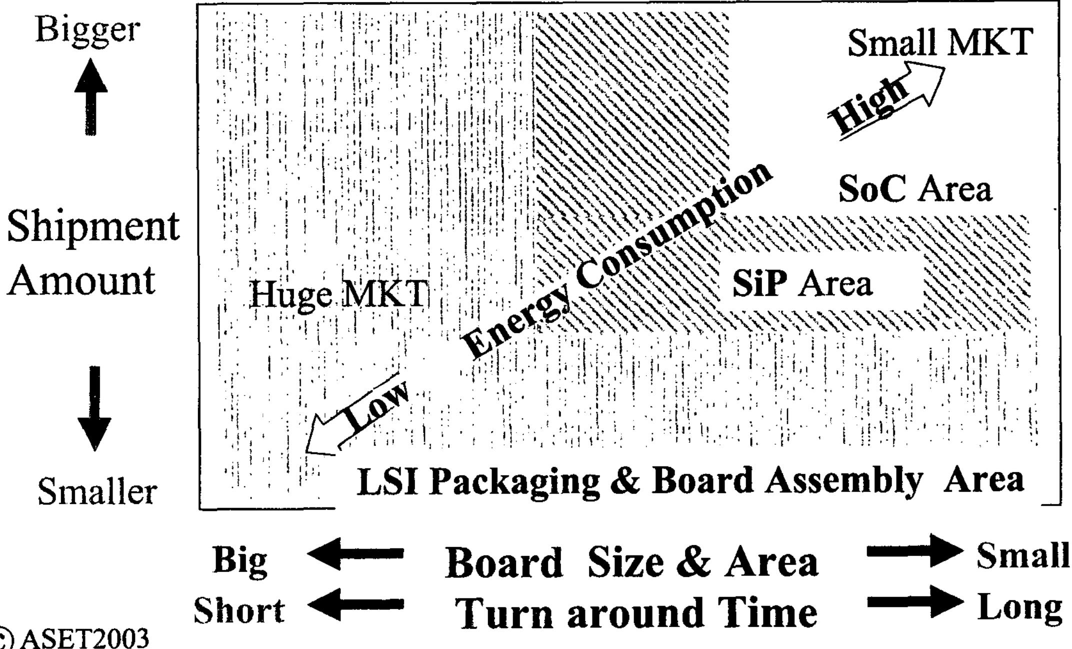
Market Aspect for Board Assembly, SiP & SoC



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SiP Target Area

10mm
1mm
100μm
10μm
1μm
100nm
Design Rule

Board Assembly
•Fine Wiring
Module
Package
SiP
•Chip size Shrink
•Shorter the wiring length
Global Wiring
IC Chip
V&ULAI Chip

10μm 100μm 1mm 10mm 100mm 1000mm
Wiring Length

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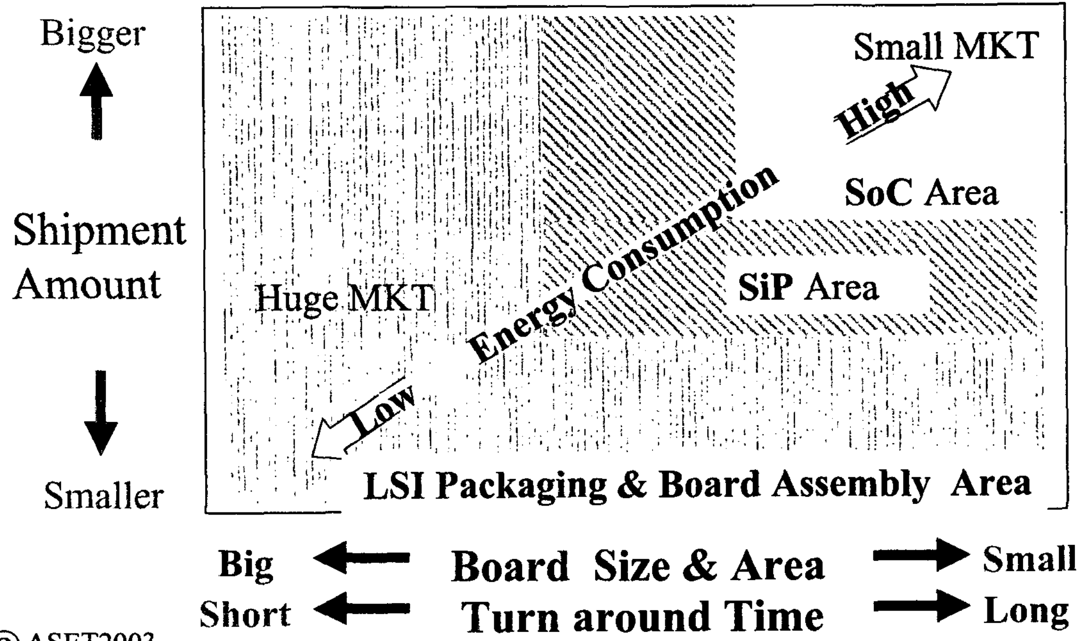
Market Aspect for Board Assembly, SiP & SoC



Big ← Board Size & Area → Small

Short ← Turn around Time → Long

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SiP Target Area

Design Rule: 10mm, 1mm, 100μm, 10μm, 1μm, 100nm

Board Assembly

•Fine Wiring

Module

Package

SiP

•Chip size Shrink
•Shorter the wiring length

Global Wiring

IC Chip

V&ULAI Chip

Wiring Length: 10μm, 100μm, 1mm, 10mm, 100mm, 1000mm

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Thank you for your attention !

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