

ISMP 2003
The 2nd International Symposium on Microelectronics and Packaging

Low Temperature Bonding and its Applications in Microelectronics

September 24-25, 2003
COEX Conference Center, Seoul, Korea

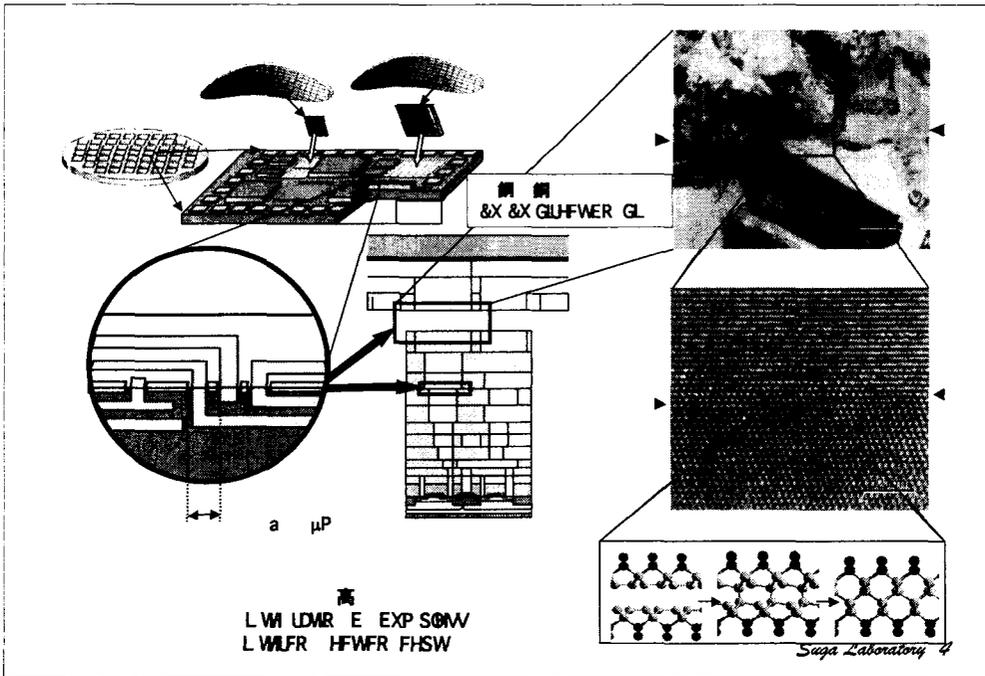
Tadatomo Suga
The University of Tokyo

Outline

- Background
- Room temperature bonding: Surface Activated Bonding (SAB)
- Applications of SAB
- Bumpless interconnect

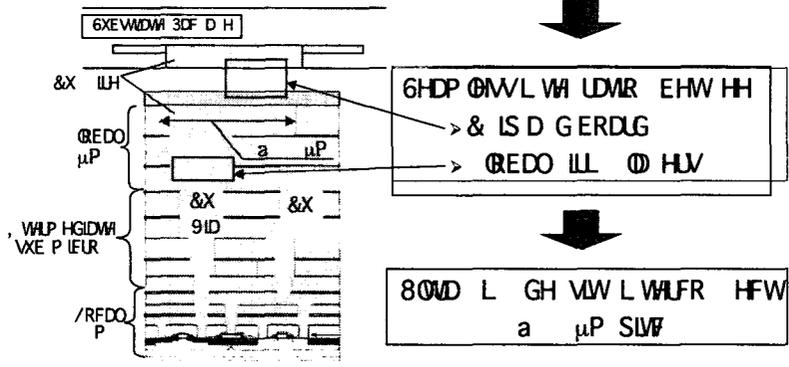
Suga Laboratory &

Bumpless Interconnect & Surface Activated Bonding (SAB)



6 WWP /6, E R GL

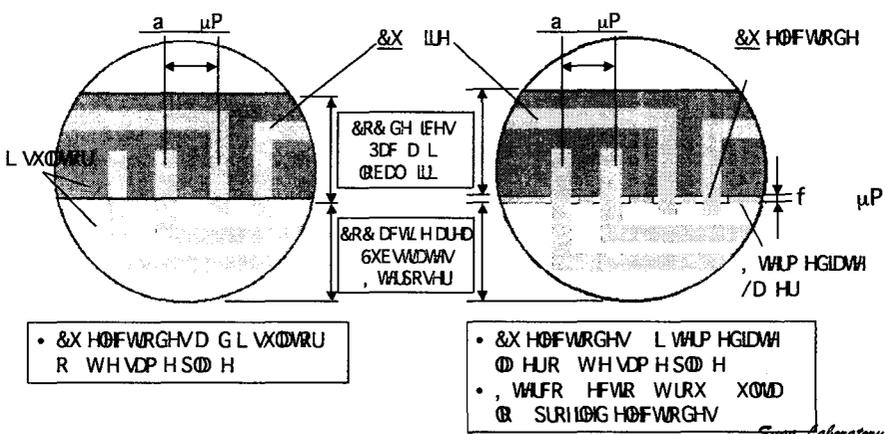
5HTXILHP H WIRUV WWP /6,
 > 0LHGVL DO6L3
 > L VSHHGVL DQMD VP LVMR
 > L VL DQ LVA LW



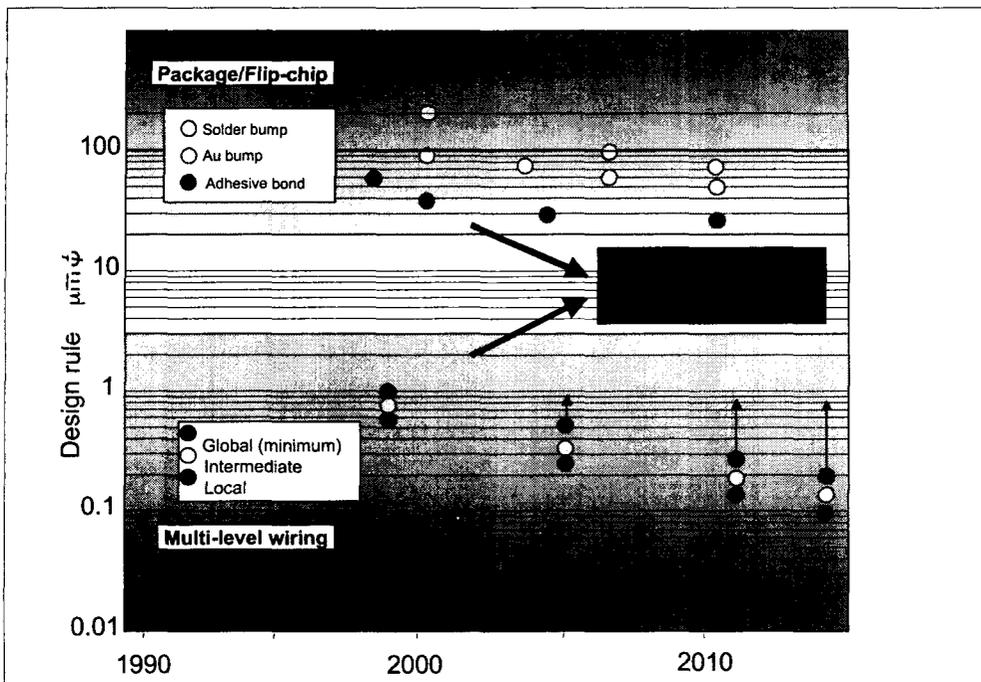
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XP S ØMVL WLF R HFV FR FHSW

, WLF R HFV R LVRXWEXP S Ø H HØFVRGHV

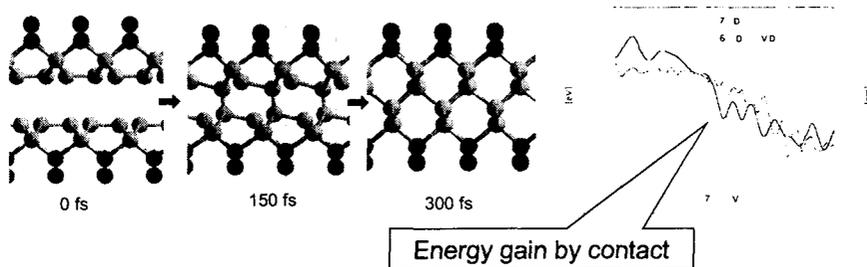


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What is bonding?

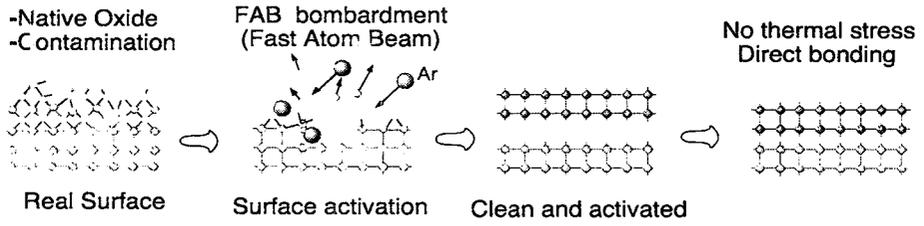
Contact of diamond (001) surfaces



- Any high temperature reaction necessary
 - Room temperature bonding is possible, if
 - Surface activity is ensured Native oxide and contamination have to be removed.
 - Ultimate contact is ensured surface roughness <1nm or plastic deformation

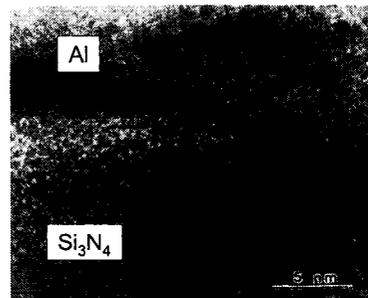
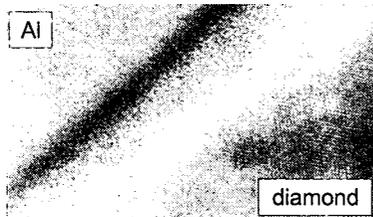
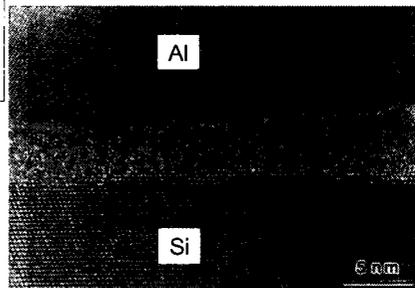
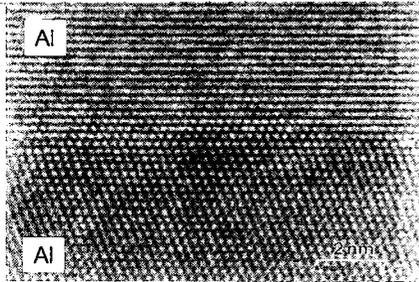
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Surface Activated Bonding (SAB)



- Room temperature process
- Direct bonding without intermediate

Surface Activated Bonding (SAB) for metals



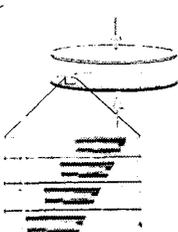
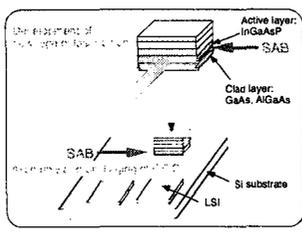
dpt lqpl dnr enq annrhrf

- wond sgd rt qe bd snl r ax qpl nulrf sgd m shud nwtd
 - lmad l lq ch slmm R A(
 - aqpl cnv mnenwtd k xdq ax cdend slmm
 - clret rlmmax gd slmf bnmudnslmm kannrhrf (
- Bnns bs snl r nmndrf gandhrf rt qe bdr
 - ek snlrr R A(
 - ok rsh cdend slmm
 - rnesdhrf ax gd slmf bnmudnslmm kannrhrf

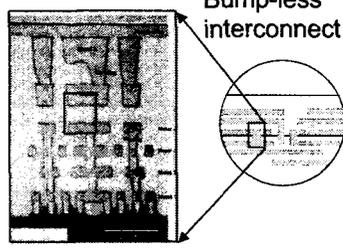
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Applications of SAB

Hetero-junction E/OE integration

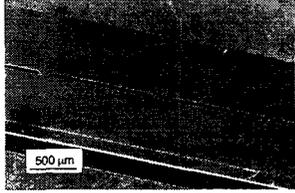



Bump-less interconnect



Low temperature with low damage

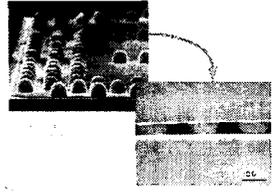
**Metal clad for build-up PWB
Safty-vent parts for Li battery**



MEMS package
Wafer scale bonding



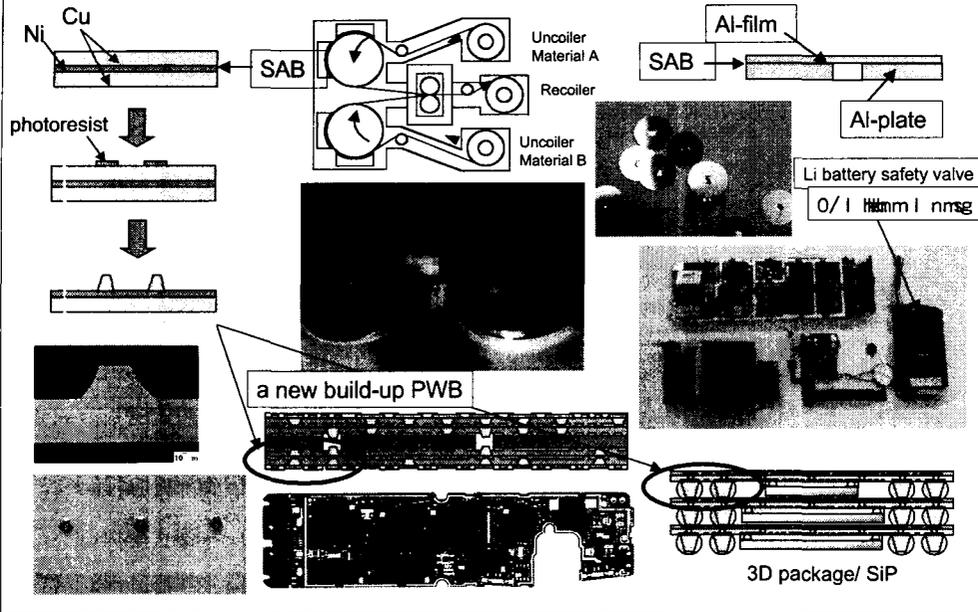

**Stacking dissimilar devices
High density interconnect**



SAB laminates

Metal-metal
Metal-polymer(LCP)

Applications of SAB metal laminates

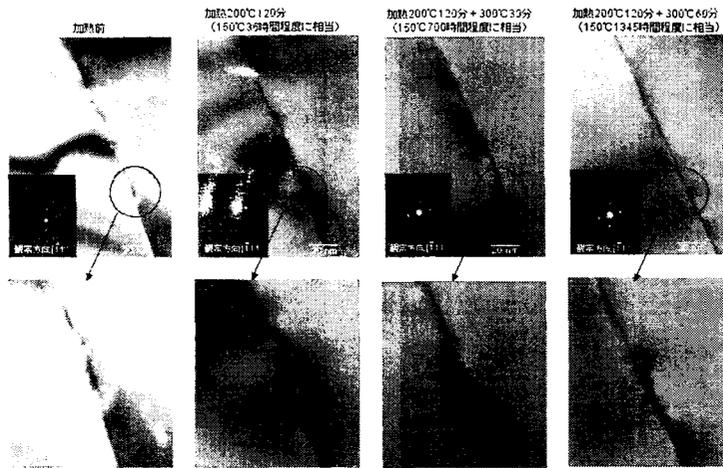


Cu-Cu bumpless interconnect

on 3 μm pad - 100,000 pins

Relaxation effect of interface structure by annealing

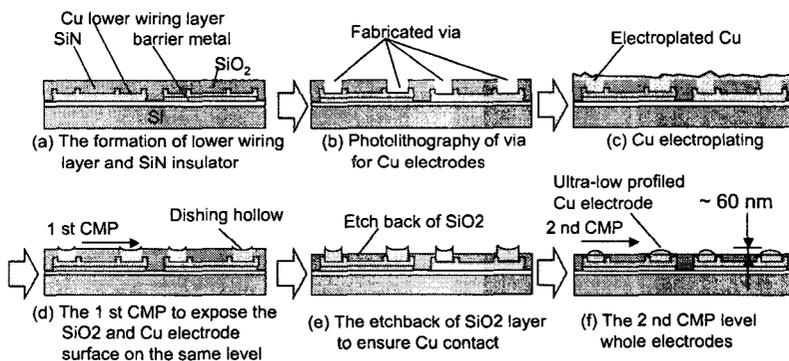
- Bonding: vacuum 1.0×10^{-4} Pa, load 50 kgf/16 mm²
- Annealing 200°C 120min + 300°C 0/30/60min
- Strain relaxed, voids disappear, and waviness of interface reduced



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XP S @W/WXFWXUH) DEUFDMR SURFHW

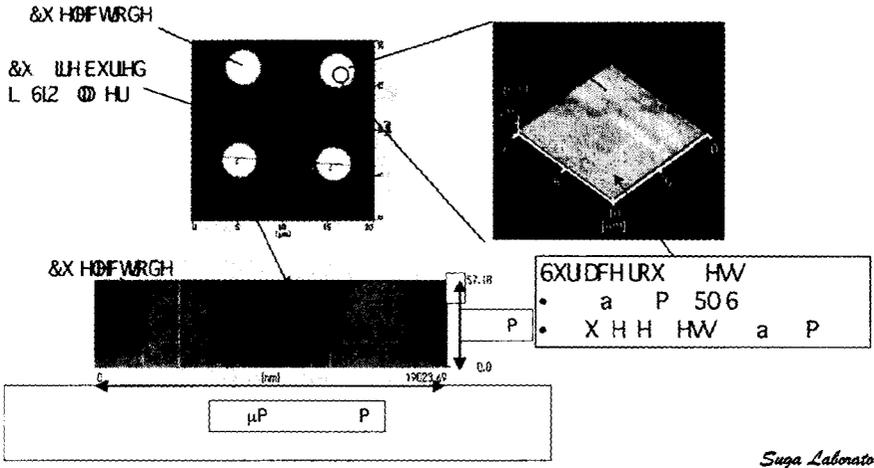
> XDOGDP DMFH H SURFHW DVDSSQHG
> 7 H HL WRI DOHOFWRGHV P



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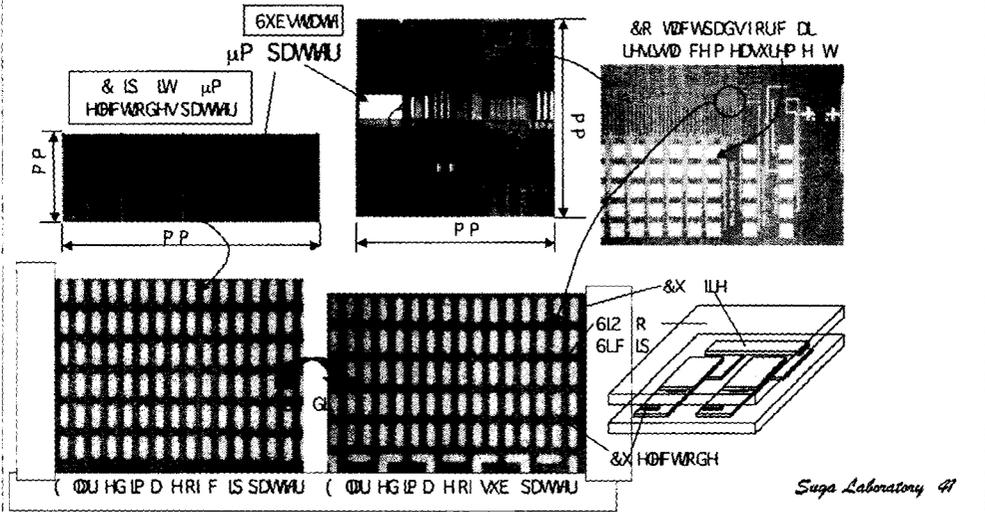
XP S ØM/WØFVXUH)DEUFDMR SURFHV

)O IP D HVRI &X µP HØFVGRHV/DI WU&O3



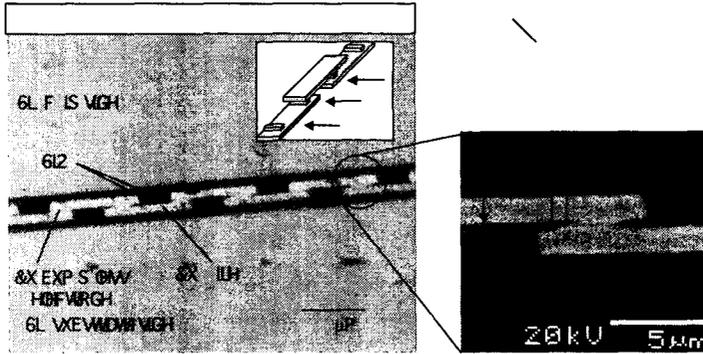
XP S ØM/WØVW H IFØI RØI WØFVXUH

SL VRI µP HØFVGRHV SL V P P -



PH WDFXUDF

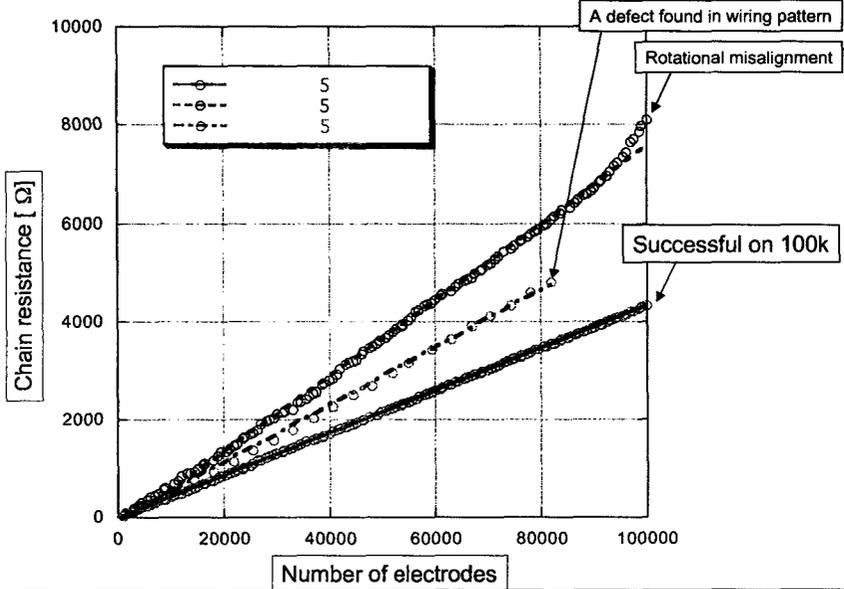
> OLVDD PH WL ± μP



&LRVWFVR IP D HRI ER GHG μP EXP S QW HGFVRGH V

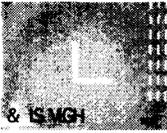
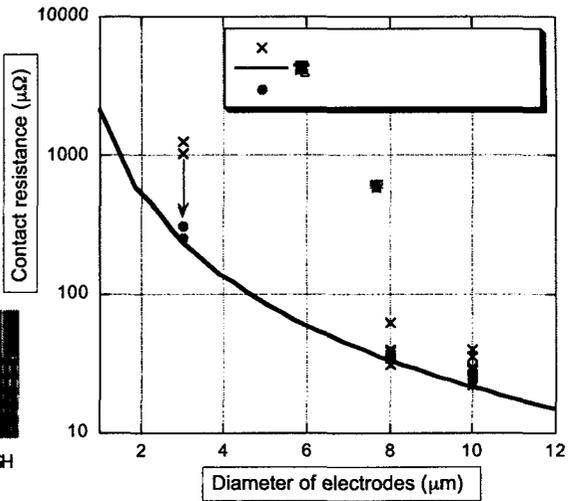
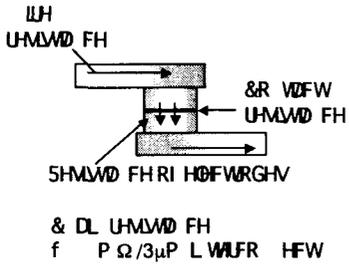
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SHXOV (QFVIEDOL WUFR HFVR



&R VDFWUHMΛVD FH

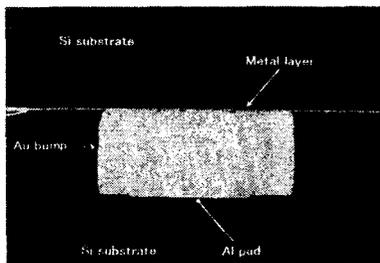
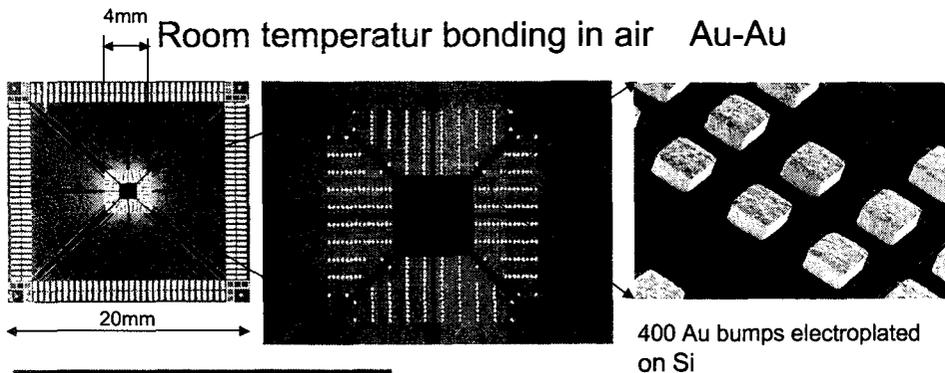
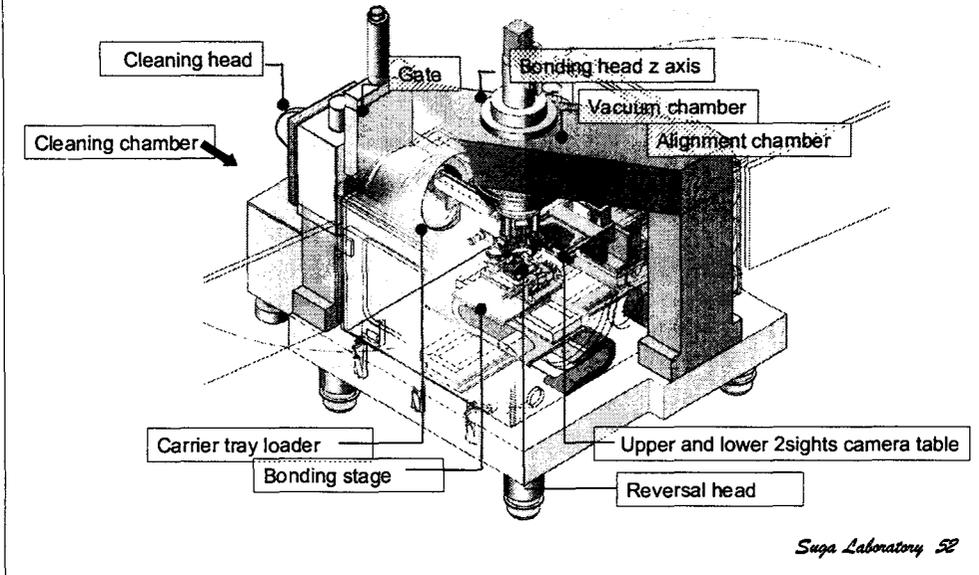
> &R VDFWUHMΛVD FH $\mu\Omega$ Θ H Θ



SAB room temperature bonding

in air
Au-Au bump

SAB-COC Bonder

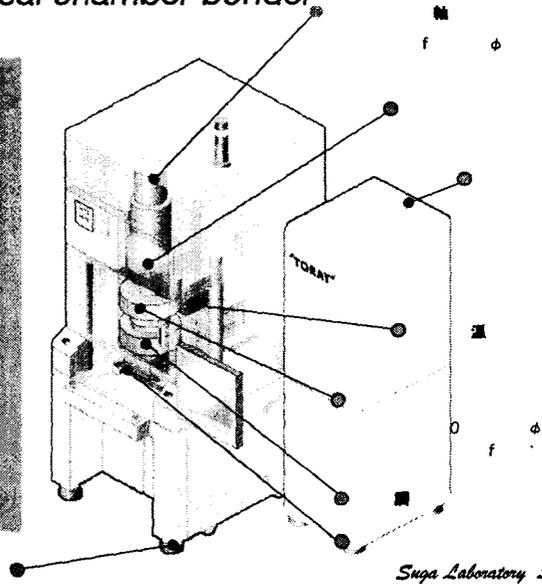
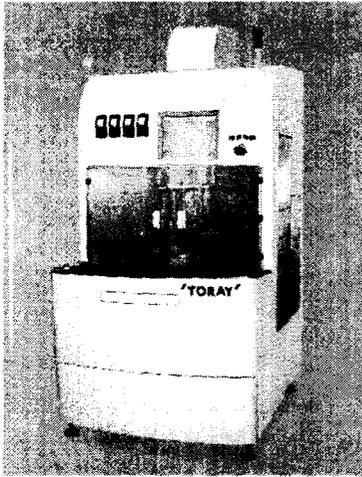


■ Au-Au can be bonded even at room temperature in air if the process parameters are optimized.

■ Important factors:

- Parallelism of chip to substrate
- Surface roughness of bumps

SAB local chamber bonder



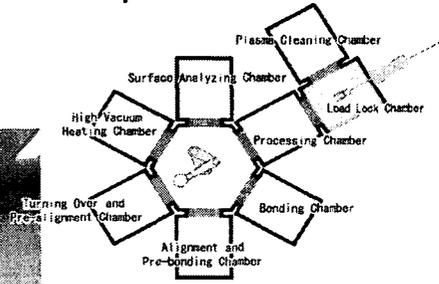
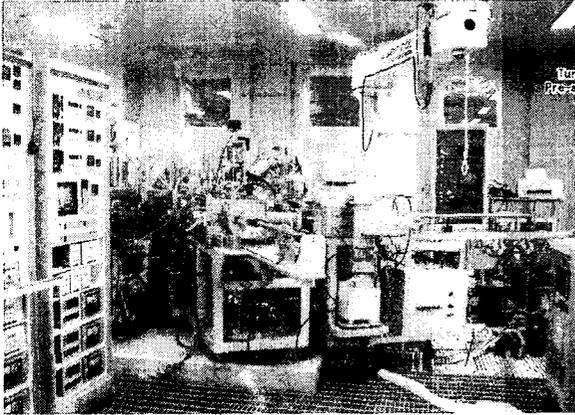
Suga Laboratory 55

SAB wafer bonding

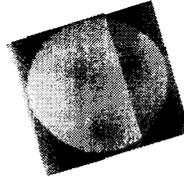
MEMS Packaging

R A v edqanædq

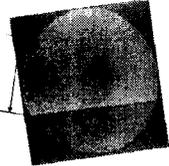
To bond 8' wafer
with alignment accuracy of $\pm 0.5\mu\text{m}$



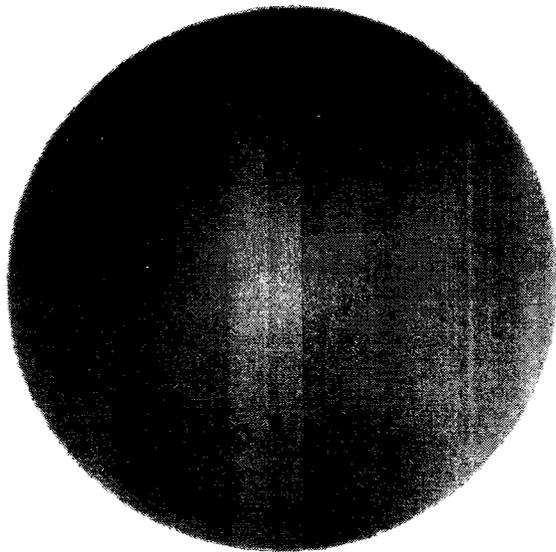
Surface activated bonding of 8' Si wafers at room temperature



Contact with 50N on the wafer 0.16 MPa



Cold rolling with 5kN/20cm \times 25kPa \cdot m



IR image of 8'-Si/8'-Si (30s:30s) bonded at room temperature

Suga Laboratory 59

oollb smmneR A

Development of new type of laser diode

Active layer: InGaAsP

SAB

Clad layer: GaAs, AlGaAs

Assembly and packaging of DEIC

SAB

Si substrate

LSI

Bonding hetero-semiconductors
Opto-electronic integration

Suga Laboratory 60

Fabrication of GaInAsP laser on GaAs by SAB

n - InP Sub. (100), 350µm

Etched out - HCl

W: 250µm

L

Electrode Au/Pt/Ti

Wavelength 1.3µm

Electrode Au-Ge-Ni

Polishing, D=100µm

n - GaAs Sub. (100), 350µm

SAB

p - InGaAs cap, 0.2µm

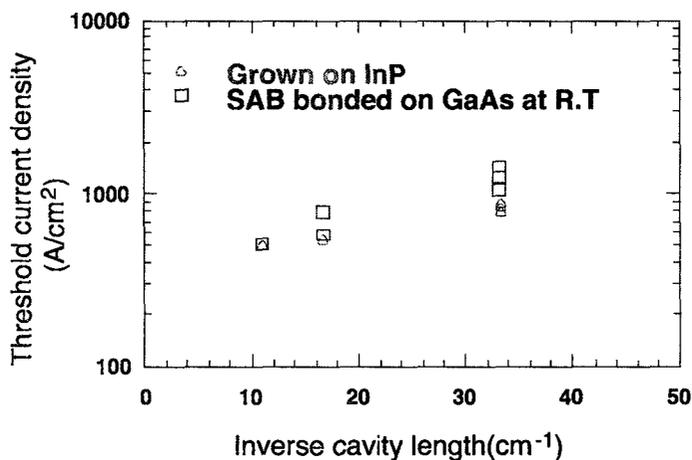
n - InP, 1.5µm

Active layer(QW)

n - InP, 1.5µm

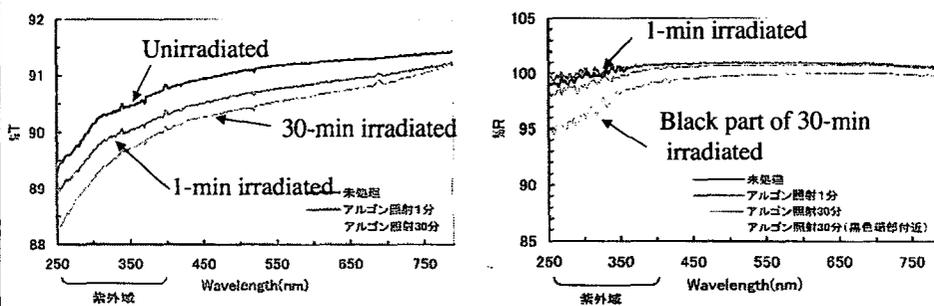
U-Tokyo, Suga-Lab

InP Laser bonded on GaAs by SAB



U-Tokyo, Suga-Lab

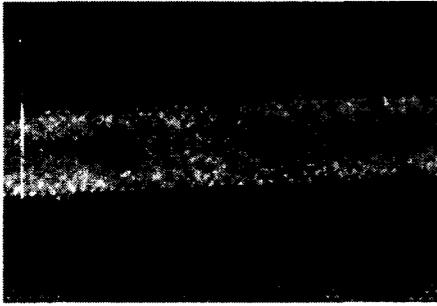
Transmission (Left) and Reflection (Right) spectra for Quartz samples before and after 1 and 30 min irradiation using a low energy ion beam of 80 V and 3 A.



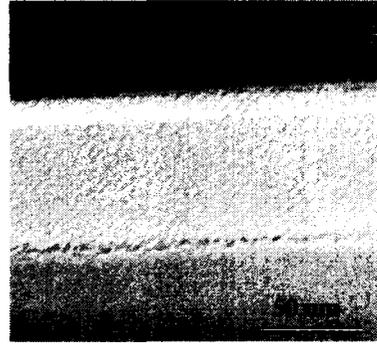
No characteristic absorption is found in transmission and reflection spectra over the ranges from UV to near infrared regions (200-2000 nm). However, transmission spectrum declines with increasing irradiation time. Significant reflection declination is observed on the black part of edge of 30 min irradiated sample.

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Interfaces bonded at room temperature
using UV transparent intermediate



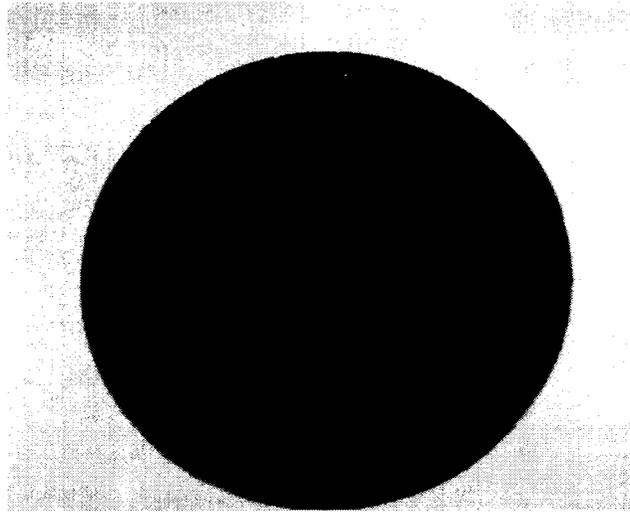
Si / Si



Quartz / Quartz

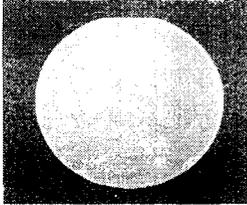
Suga Laboratory 69

h aN Rh edqanncmf s qnl sdl odq st qd

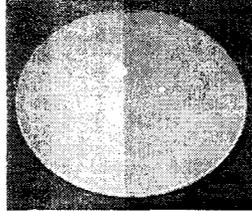


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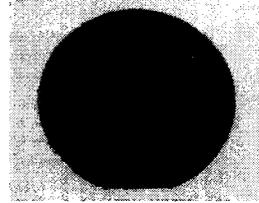
Quartz to Quartz



Fused Silica



Quartz to Si



Perspective of SAB

Chip on chip/ Chip on wafer

with ultra-high density of bumpless interconnect

MEMS packaging by stacking Si and non-Si wafers

EcoDesign

Institute for advanced Micro-System Integration (IMSI)

Consortium founded in 1998 for collaboration with University of Tokyo

- Development of GHz system packaging
- Room temperature bonding for ultra-high density interconnect
- Environmentally conscious design for packaging



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Research Center for Advanced Science & Technology
Nanometer-scale Manufacturing Science Lab.
Micro-system Integration and Packaging Lab.*

cooperation with

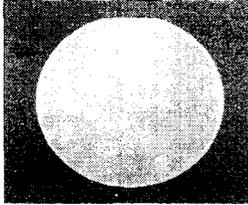
Institute for advanced Micro-System Integration (IMSI)

Prof. Dr. Tadatomo Suga

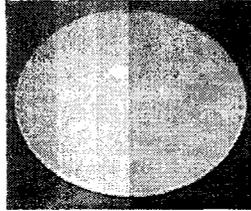
Associate Prof. Dr. Toshiro Itoh
Associate Researcher Dr. Naoe Hosoda (NIMS)
Assistant Researcher Mr. Ken'ichi Kataoka
Associate Prof. Dr. Matiar Hawlader
Prof. Dr. Katsuya Okumura
Prof. Dr. Jun Fujimoto (Asia-EcoDesig Project)
Assistant Researcher Mr. Kazuhiko Nakamura
Secretary Ms. Natsuko Kawamata



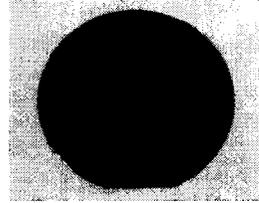
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Fused Silica



Quartz to Si



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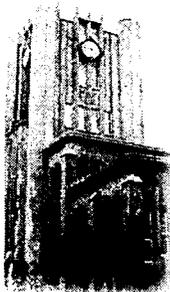


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