A CMOS Macro-Model for MTJ Resistor of MRAM cell

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Abstract

Recently, the magneto-resistive random access memory (MRAM) is considered as a great application of magnetic material because of its prominent potential for a non-volatile and high-speed memory [1]. The development of CMOS macro-model for MRAM cell is an essential part to enhance efficient MRAM architectures without a matured MRAM process. This paper proposes a novel CMOS circuit for emulating voltage-dependent characteristics of MTJ resistance and its applications in the MRAM core parts. Fig 1. shows typical resistive characteristic curves with regard to the applied voltage range of ±500[mV].

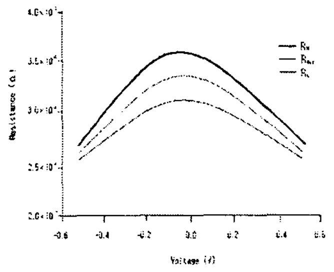

Fig.1. MTJ resistance characteristic curves according to the supply voltage

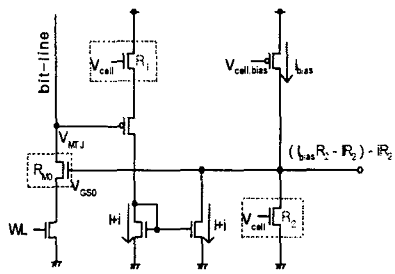

Fig.2. Macro-model for voltage-dependent MTJ cell

Fig.2. shows the proposed macro-model for a MTJ resistor taking the MR ratio variations into account. The feedback circuit senses V_{MTJ} to control the gate voltage of the emulation transistor. The turn-on resistance of the transistor is

$$R_{M0} \cong \frac{1}{A+\alpha_1 V_{MTJ} - \alpha_2 V_{MTJ}^2} \quad \text{where } \alpha_1 \text{ and } \alpha_2 \text{ are design parameters.} \qquad (1)$$

In conclusion, the MTJ resistor R_{M0} in equation (1) can show basically the 1st-order approximated characteristics in Fig.1.

References

[1] M. Durlam.ct. al., "Nonvolatile RAM Based on Magnetic Tunnel junction Elements." ISSCC Digest of technical Papers. Pp 130-131. Feb. 2000