

고전류스트레싱이금스터드뎀프를이용한ACF플립칩파괴기구에 미치는영향 (HighElectricalCurrentStressingEffectsontheFailureMechanismsof Austudbumps/ACFFlipChipJoints)

김형준, 권운성, 백경욱
KAIST 재료공학과 나노패키징 및 접속연구실
E-mail: hikim76@kaist.ac.kr

Abstract: In this study, failure mechanisms of Au stud bumps/ACF flip chip joints were investigated under high current stressing condition.

For the determination of allowable currents, I-V tests were performed on flip chip joints, and applied currents were measured as high as almost 4.2Amps (4.42×10^4 Amp/cm²). Degradation of flip chip joints was observed by *in-situ* monitoring of Au stud bumps-Al pads contact resistance. All failures, defined at infinite resistance, occurred at upward electron flow (from PCB pads to chip pads) applied bumps (UEB). However, failure did not occur at downward electron flow applied bumps (DEB). Only several mΩ contact resistance increased because of Au-Al intermetallic compound (IMC) growth. This polarity effect of Au stud bumps was different from that of solder bumps, and the mechanism was investigated by the calculation of chemical and electrical atomic flux. According to SEM and EDS results, major IMC phase was Au₅Al₂, and crack propagated along the interface between Au stud bump and IMC resulting in electrical failures at UEB.

Therefore, failure mechanisms at Au stud bump/ACF flip chip joint under high current density condition are: 1) crack propagation, accompanied with Au-Al IMC growth, reduces contact area resulting in contact resistance increase; and 2) the polarity effect, depending on the direction of electrons, induces and accelerates the interfacial failure at UEBs.

1. INTRODUCTION

Due to downscaling of package dimensions, size of bumps has been reduced, but current densities at bumps are increasing. Moreover, increased current density induces new failure mechanism, such as electromigration phenomena in flip chip packages. Recently, many researchers have been investigated the electromigration phenomena in solder flip chip and solder flip chip showed strong polarity effects by the direction of electron flow. However, few studies were performed on the current handling capability of Au stud bumps/ACF (Anisotropic Conductive Film) flip chip.

Bertolino [1] et al. reported Au-Al electromigration phenomena at Au/Al thin film diffusion couple. According to the results, the polarity effect on intermetallic compounds (IMCs) growth was not observed up to 1019 A/cm² current density condition. However, the test temperature was too high, about 400 ~ 500°C, compared to the chip operating temperature. Krabbenborg [2], and Passagrilli[3] investigated failure of Au wire bonding chip under high current density conditions in the range of 10⁴ ~ 10⁵A/cm². They observed that the growth of Au-Al IMCs and failure pads depended on the direction of electron flow but the detailed explanation about the polarity phenomena was missed.

Au stud bumps/ACF flip chips are used for some flip chip packages, such as SAW device packages. Therefore, it is necessary to investigate the characteristics of ACF flip chip joints using Au stud bumps.

In this paper, the current handling capability of Au stud bumps/ACF flip chip joints is examined, and the failure mechanisms, focused on polarity effect, after current stressing are also investigated.

2. EXPERIMENTAL

2-1. Test vehicle

Test vehicles consisted of Si test chips and FR4 boards for four-point probing. Test chips had peripheral-array Al pads, and the pad pitch was 300 μm . Thickness of Al pad was 1 μm . Au stud bumps were formed using a K&S 4522 manual wire bonding machine. 2N gold wire (99% Au and 1% Pd alloying) of 25 μm diameter was used for Au stud bumping.

Test boards had patterned Cu/Ni/Au trace for measuring contact resistance of each stud bumps. Test chips and boards were interconnected using ACFs. The bonding pressure was 160 N (3.64 N/bump) and ACF curing was performed at 190°C for 30 sec. The assembled test vehicle (Au stud bumps/ACF flip chip) is shown in Fig. 1.

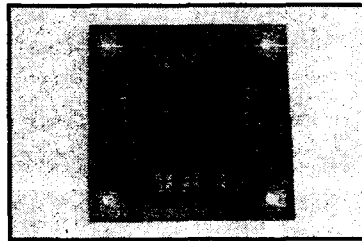


Fig. 1. Top-view of a test vehicle.

2-2. Current stressing test

The schematic diagram of test equipment used for current stressing test is shown in Fig. 2. The maximum allowable current was decided by performing bias-stressing test on a pair of Au stud bumps. Therefore, the determined current, 4.2 A, which could supply current density of $4.42 \times 10^4 \text{ A/cm}^2$, was applied at current stressed bumps. In addition, in this experiment, constant bias was provided for supporting constant current density condition. The cross-section of test vehicle is shown in Fig. 3. During current stressing tests, test vehicles were placed on a hot plate at 110°C, and temperature near tested bumps was monitored using an adhesive-type thermocouple. The measured temperature at tested bump side was maintained at $170 \pm 3^\circ\text{C}$.

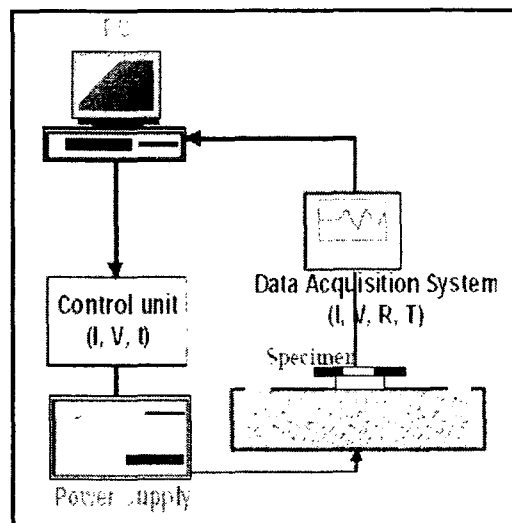


Fig. 2. A schematic diagram of test equipment for current stressing test.

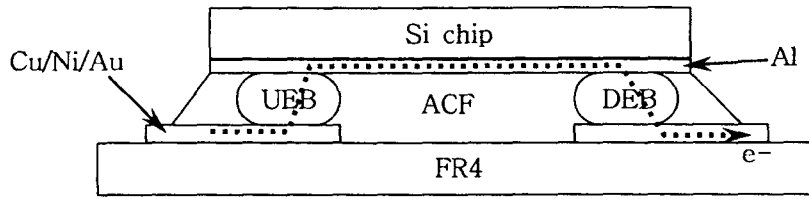


Fig. 3. A schematic cross section of a test vehicle during current stressing.

The degradation of Au stud bump/ACF flip chip joints was observed by *in-situ* monitoring of contact resistance changes and the failure was defined at infinite resistance. After current stressing, some test vehicles were cross-sectioned, and SEM, EDS, and WDS were used to investigate Au/Al IMC layers and failure interfaces. In addition, plain-view of failure sites was examined by separating chips from FR4 substrates.

3. RESULTS & DISCUSSION

3-1. I-V test (Bias stressing test)

The bias stressing test was performed to examine the maximum allowable current ranges under current stressing conditions. Fig. 4 shows a typical test result when bias was stressed at a pair of Au stud bumps/ACF flip chip joints. The current increased linearly till 2 V, however, abrupt decrease of current was observed at about 2.25 V due to the burning of PCB trace. Therefore, the maximum allowable current was about 6 A, and the applied current for a stressing test should be maintained at lower than 6 A.

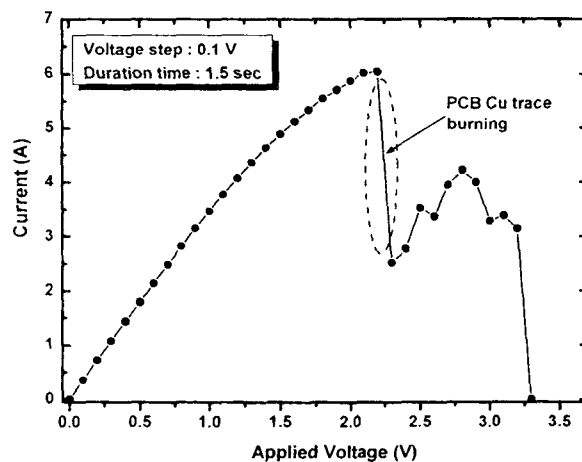


Fig. 4. A typical result of I-V test (bias stressing) at Au stud bumps/ACF flip chip joints.

3-2. Failure analysis

Fig. 5(a) shows the resistance changes of flip chip joints under constant current density of 4.42×10^4 A/cm². The resistance increased slightly just before failure and sudden failure occurred. However, the measured resistance included line resistance elements which were caused by PCB trace, and Al metallization, therefore, the contact resistance changes of UEBs, DEBs, and neighboring bumps were measured as shown in Fig. 5(b). According to the Fig. 5(b), the abrupt increase of resistance, shown in Fig. 5(a), originated in open circuit failure at UEBs. However, at DEBs and neighboring bumps, only several mΩ increases were measured, and electrical failure did not occur.

Fig. 6 shows cross-section SEM images of stud bump flip chip joints after electrical failure. As shown in

Fig. 6, severe contact degradation occurred at UEBs, and different types of failure phenomena were observed. It implied that there were several causes which affected contact degradation. Hence, the following can be suggested as possible causes of degradation.

- Au-Al IMCs formation
- Crack and propagation, accompanied with Au-Al IMC formation, along the Au/IMC interface
- Al or Au depletion due to electromigration under high current density and polarity effects

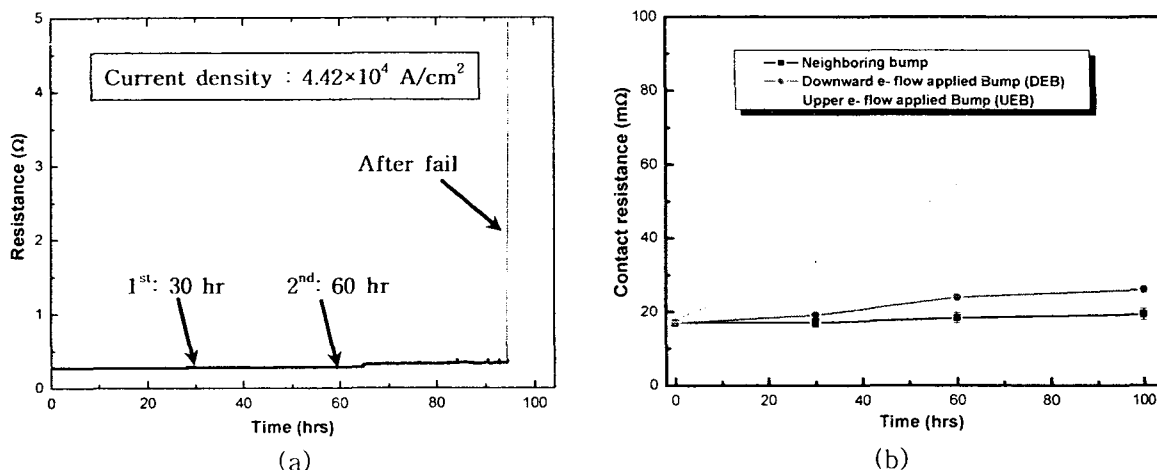


Fig. 5. (a) *In-situ* monitored resistance change curve under current density of 4.42×10^4 A/cm². (b) Contact resistance changes of neighboring bump with no current stressing, DEB, and UEB after 30 hours, 60 hours, and fail of current stressing.

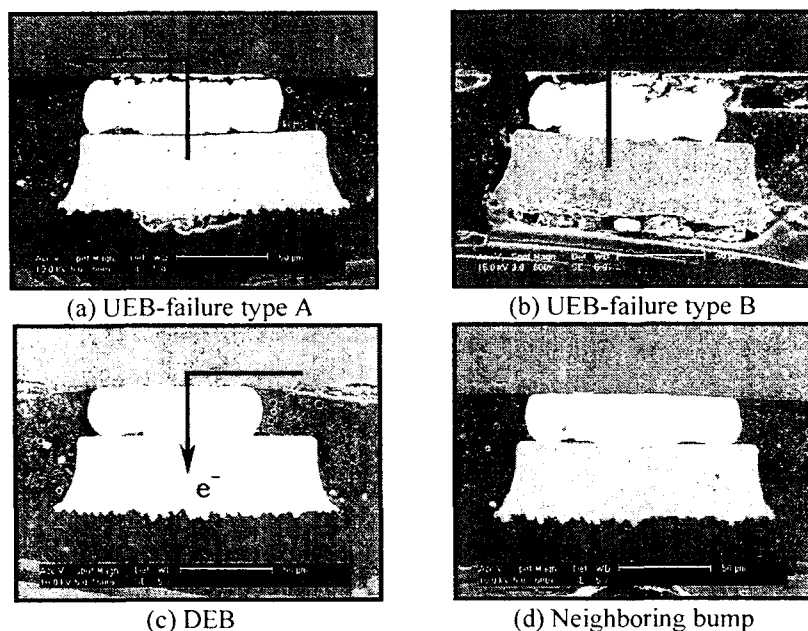


Fig. 6. Cross-section SEM images of (a) UEB-failure type A, (b) UEB-failure type B, (c) DEB, and (d) neighboring bump without current stressing after failure occurred.

Au-Al IMCs formation

At test temperature, about 170°C, Au-Al IMCs could form easily, and Au₅Al₂ and Au₂Al IMC phases were identified by EDS analysis at Au stud bumps and Al pads interface. Philofsky [4] reported that Au₅Al₂ phase had the largest rate constant, and Au₂Al was the 2nd. Moreover, the total amount of Al which could join the interfacial reaction was limited compared to that of Au. Therefore, Au-rich IMCs were expected as final IMC

phases and, the results of EDS analysis, Au₅Al₂ and Au₂Al, were acceptable.

The electrical resistivity of Au, Al, and their IMCs was given in Table 1, and IMCs had higher resistivity than Au or Al. Therefore, more joule heating could be generated when IMCs present at the interface due to higher resistivity. However, IMCs growth of only several μm could not be the major cause of abrupt resistance increase shown in Fig. 5(a). Resistance could be calculated using the next formula.

$$R = \rho \left(\frac{l}{A} \right) \quad (1)$$

(ρ : resistivity, l : IMC thickness, A : Area)

If we assumed that layer-type Au₅Al₂ IMC formed with 4 μm thickness, the theoretical resistance increase calculated using the given equation was only 10 ~ 20 mΩ. Consequently, IMC formation was not a main cause for abrupt resistance increase.

Table 1. Electrical resistivity of Au, Al, and their IMCs.

Phase	Electrical resistivity (μΩ·cm)
Al	3.2
AuAl ₂	7.9
AuAl	12.4
Au ₂ Al	13.1
Au ₅ Al ₂	25.5
Au ₄ Al	37.5
Au	2.3

Crack propagation along the Au/IMC interface

Although IMC formation itself did not have much influence on the resistance increases, it could not be ignored. Kirkendall voids formation along the Au/IMC interface is well-known phenomena, and they cause crack formation and propagation. Furthermore, Mori et al. [5] reported that the volume change during IMCs formation induced irregular and poor bond at bonding interface and these imperfections assisted crack propagation. In accordance, the side effects of IMCs formation, such as kirkendall voids formation and volume differences, caused crack propagation resulting in an effective contact area decrease. Finally, when cracks spread over all the contact area, abrupt resistance increase could occur. Failure type A of Fig. 6(a) is well-corresponding to this degradation mechanism.

Al or Au depletion due to electromigration and polarity effects

As shown in Fig. 6(b), severe contact degradation at UEBs was observed, and the shape of failure site was tangled. Presumably, it implied that Al or Au metals moved at bonding interface of UEBs by the electron flow. However, no failure was observed at DEBs. These phenomena could be verified by the results of dot-mapping, in Fig. 7. Al metallization near the UEB and Au were depleted and moved by the electromigration effect because the reported effective charge (Z^*) of Al was ranged from -30 to -12 and that of Au was about -8.5 [6]. Minus value of Z^* means that the direction of migrating atoms is same as that of electron flow. As shown in Fig. 7(b), Al line remained at bump edge but it was consumed by interfacial reaction at bonding interface. However, in neighboring bumps, even at bonding interface, Al remained without joining reaction. Therefore, it was thought that applying current at Au/Al bonding interface accelerated interfacial reactions. Consequently, the contact resistance of DEBs was slightly higher than that of neighboring bumps (shown in Fig. 5(b)).

Chen et al. [7] calculated atomic flux (J) at Sn/Ni and Ni/Sn interface to explain the polarity effects by the direction of electron flow. The total atomic flux (J_t) is the sum of chemical atomic flux (J_{chem}) and electrical

atomic flux (J_{elec}).

$$J_i = J_{chem} + J_{elec} = -\frac{D_i N_i}{RT} \left(RT \frac{\partial \ln N_i}{\partial x} + F Z_i^* E \right) \quad (2)$$

(D_i : diffusion coefficient, N_i : mole fraction, T : temperature, R : gas constant, x : IMC layer thickness, Z_i^* : effective charge, F : Faraday constant, and E : Electric field)

To apply the above equation to Au/Al interfacial reaction, followings were assumed.

- Effective charge of Au and Al are -8.5 and -22, respectively.
- Au_5Al_2 IMC formed with about 2 μm thickness

The mole fraction can be obtained from the Au-Al phase diagram. Electric field can be calculated using resistivity and thickness of IMC layer. Finally, calculated chemical and electrical atomic fluxes are listed in Table 2. In accordance, total flux of Al and Au at UEB interface were -224.88 J/mol- μm and -137.62 J/mol- μm as shown in Fig. 8, respectively. It means that Al and Au will move away from UEBs, therefore, metal depletion is observed at UEBs. However, at DEBs, opposite phenomena will be occurred and Au and Al atoms move to DEBs. That is, Al atoms accumulated and no metal depletion was observed at DEBs, and cumulated Al was consumed by joining the interfacial reaction at bonding interface. A schematic diagram of total atomic fluxes of Al and Au at UEB and DEB is shown in Fig. 8.

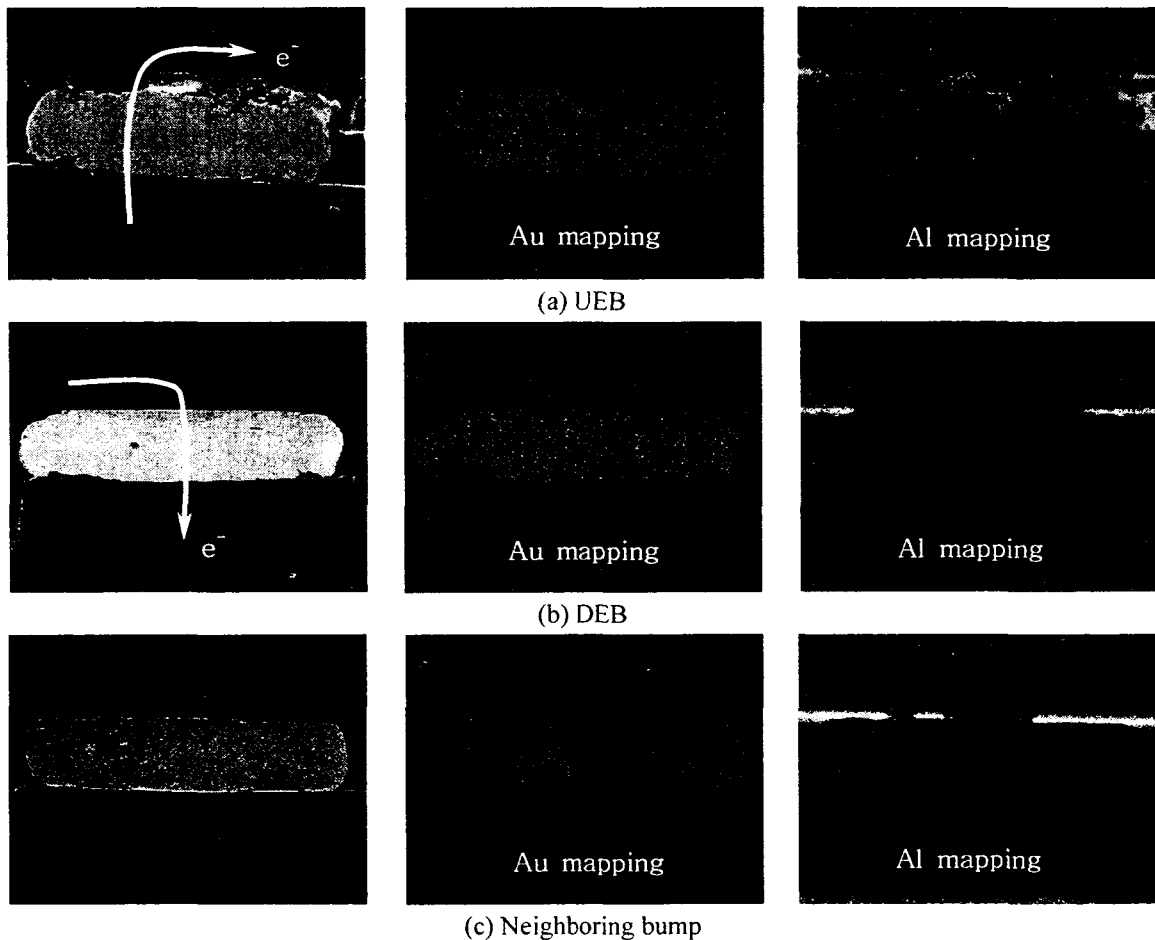


Fig. 7. Dot-mapping images of (a) UEB, (b) DEB and (c) neighboring bump.

Table 2. Calculated chemical and electrical atomic fluxes.

	Au flux into Al (J/mol- μm)	Al flux into Au (J/mol- μm)
Chemical	-25.76	-64.62
Electrical	-111.86	-289.50

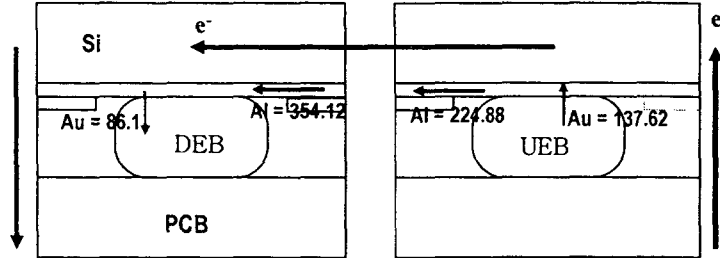


Fig. 8. A schematic diagram of total atomic fluxes of Al and Au at UEB and DEB bumps during current stressing.

4. Conclusions

The current stressing test was performed on the Au stud bumps/ACF flip chip joints and failure mechanisms were investigated.

1. The polarity effects caused by the direction of electron flow were confirmed. Moreover, due to the direction of atomic flux, metal depletion and interfacial degradation failure were observed.
2. Small contact resistance increase was induced by Au/Al IMCs growth, and crack propagation was the major cause of abrupt resistance increase.
3. Comparing the results of dot-mapping between DEBs and neighboring bumps, applying current at Au/Al interface accelerated interfacial reaction

5. acknowledgement

This work was supported by the Center for Electronic Packaging Materials (CEPM) of the Korea Science and Engineering Foundation.

6. references

- [1] N.Bertolino, J.Garay, U.A-Tamburini and Z.A.Munir, "High-flux current effects in interfacial reactions in Au-Al multilayers", *Philosophical Magazine B*, Vol. 82, No. 8, 2002, pp. 969-985
- [2] B.Krabbenborg, "High current bond design rules based on bond pad degradation and fusing of the wire", *Microelectronics Reliability*, Vol. 39, 1999, pp. 77-88
- [3] C.Passagrilli, "Au wire bonding in plastic packages: Reliability improvements for high temperature (200°C) and high current applications", *Advancing Microelectronics*, March/April, 2003, pp. 25-27
- [4] E.Philofsky, "Intermetallic formation in gold-aluminum systems", *Solid-State Electronics*, Vol. 13, 1970, pp. 1391-1399
- [5] M.Mori, Y.Fukuda, Y.Kizaki, A.Iida, and M.Saito, "An investigation of stable bonding for Au-Al solid phase diffusion bonding techniques", *Electronics and Communications in Japan, Part 2*, Vol. 82, No. 2, 1999, pp. 11-19

- [6] P.Shewmon, *Diffusion in Solids 2nd edition*, Pennsylvania, TMS, 1989
- [7] S.-W.Chen, C.-M.Chen, and W.-C.Liu, "Electric current effects upon the Sn/Cu and Sn/Ni interfacial reactions", *Journal of Electronic Materials*, Vol. 27, No. 11, 1998, pp. 1193-1198