IMAPS Korea 2003 Conference

Advanced Packaging Technologies in Japan

IMAPS Japan
Nagano Institute of Technology

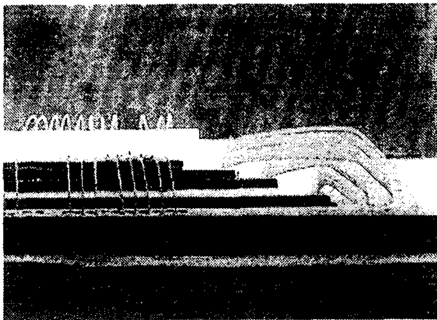
Dr.S.Denda

November 14, 2003 in Seoul

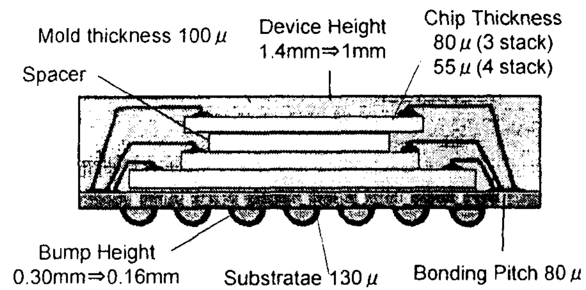
Advanced Packaging Technologies Currently Remarkable in Japan

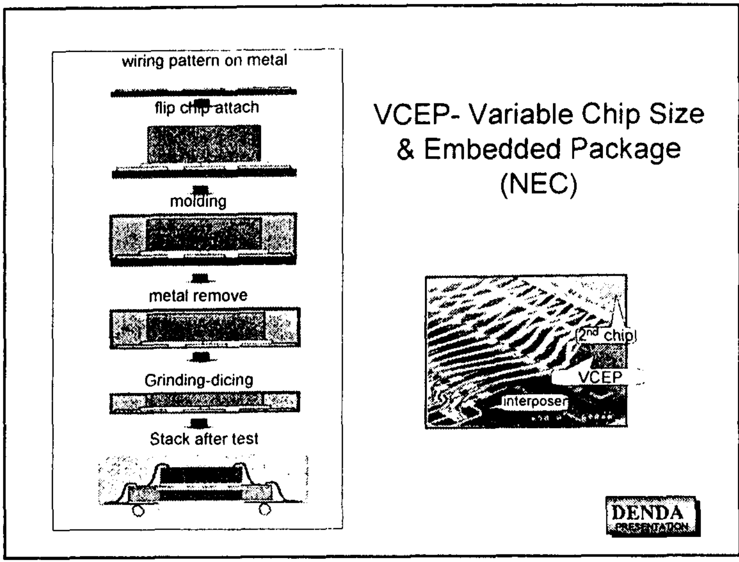
- High Frequency Package
- High Density Packaging
- Thin Silicon Wafer Processing
- Lead Free Soldering
- RFID-IC Tag

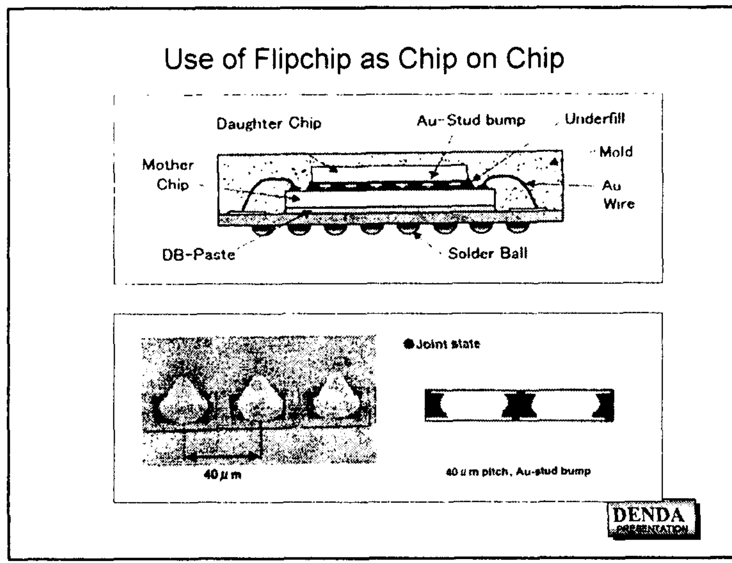
Typical Chip Level Stacking Device (4 chip stack by Sharp)

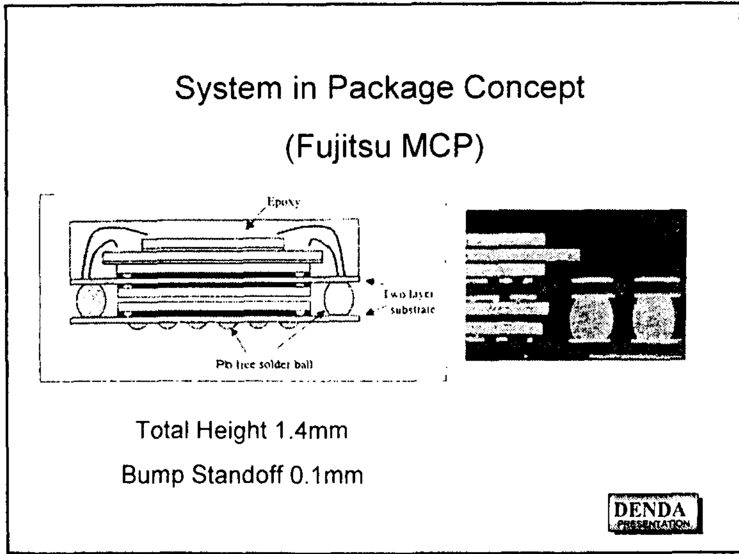


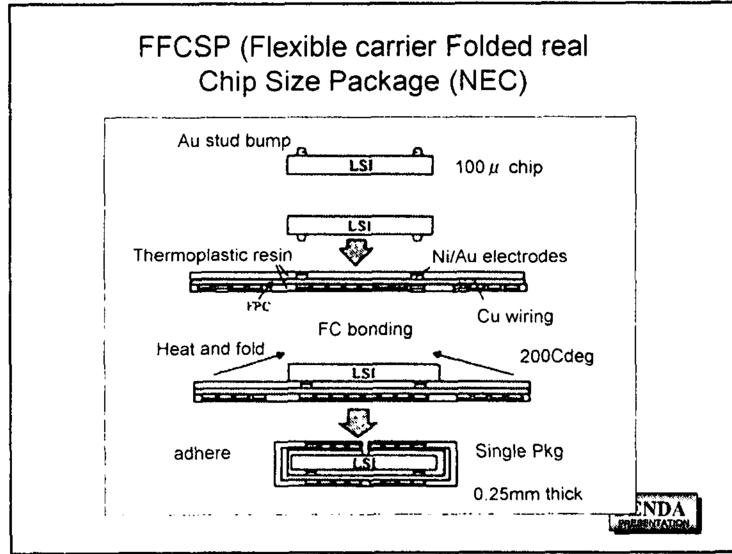
Requirements for Chipstack Device



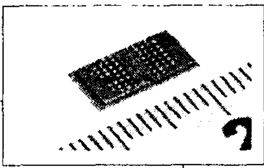

VCEP- Variable Chip Size
& Embedded Package
(NEC)
wiring pattern on metal
flip chip attach
molding
metal remove
Grinding-dicing
Stack after test
2nd chip
VCEP
interposer
DENDA

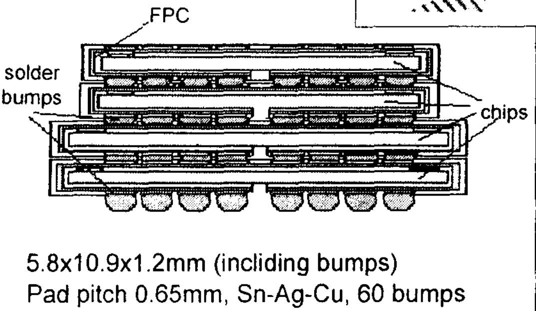

Use of Flipchip as Chip on Chip
Daughter Chip
Au-Stud bump
Underfill
Mold
Mother Chip
Au Wire
DB-Paste
Solder Ball
●Joint state
40μm
40μm pitch, Au-stud bump
DENDA


System in Package Concept
(Fujitsu MCP)
Epoxy
Two layer substrate
Pb free solder ball
Total Height 1.4mm
Bump Standoff 0.1mm
DENDA


FFCSP (Flexible carrier Folded real
Chip Size Package (NEC)
Au stud bump
LSI
100μ chip
Thermoplastic resin
Ni/Au electrodes
FPC
Cu wiring
FC bonding
Heat and fold
200Cdeg
adhere
Single Pkg
0.25mm thick

4 chip stack FFCSP

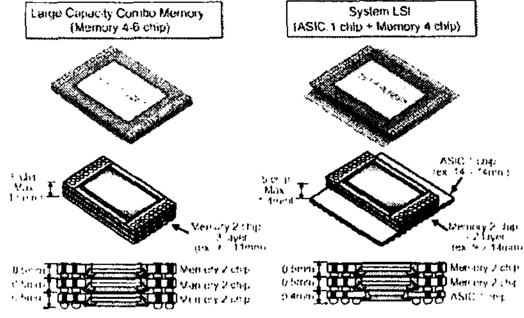




5.8x10.9x1.2mm (incliding bumps)
Pad pitch 0.65mm, Sn-Ag-Cu, 60 bumps

DENDA PRESENTATION

Package Stack Device (Sharp)

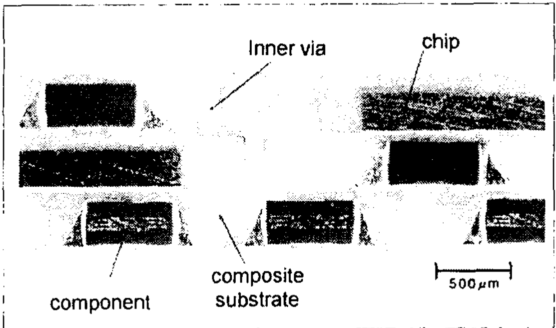


Stack after test , flexible combination, passive component, system packaging

DENDA PRESENTATION

Embeded Chip Substrate SIMPACT (Matsushita)

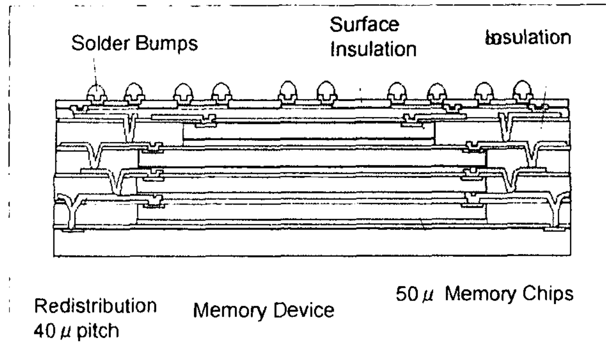
System in Module using Passive and Active Components embedding Technology



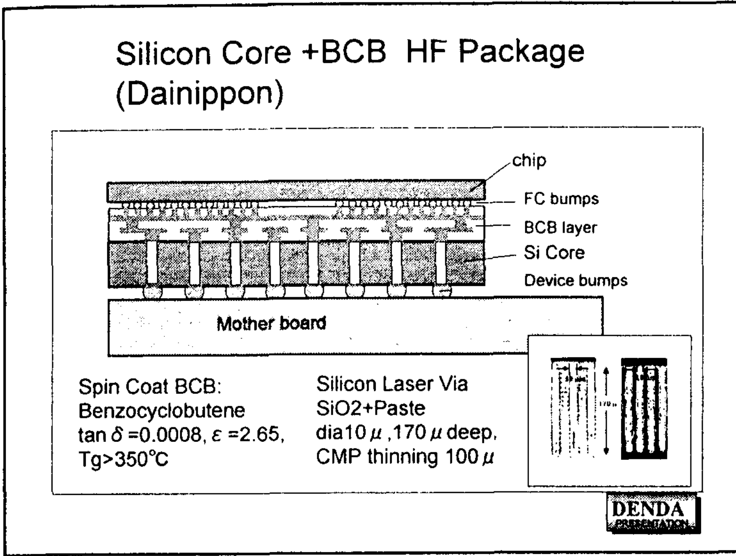
- Thermo setting resin and ceramic powder
- No deform via filling material

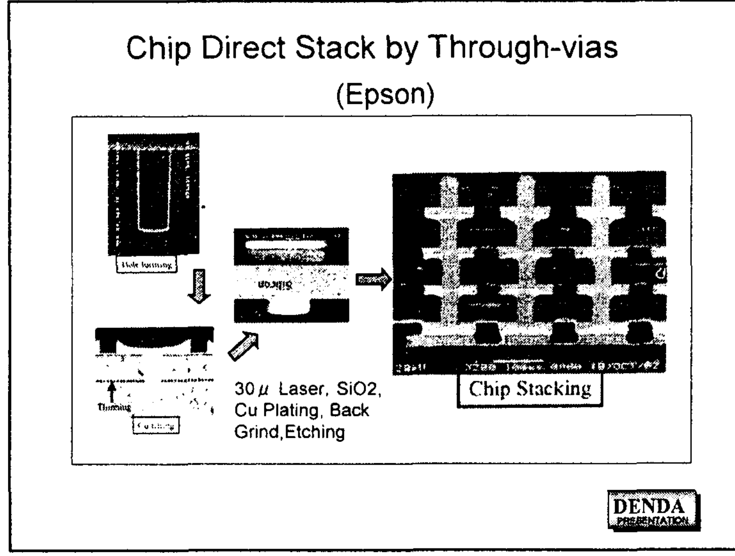
DENDA PRESENTATION

Chip Scale Module (Fujitsu)



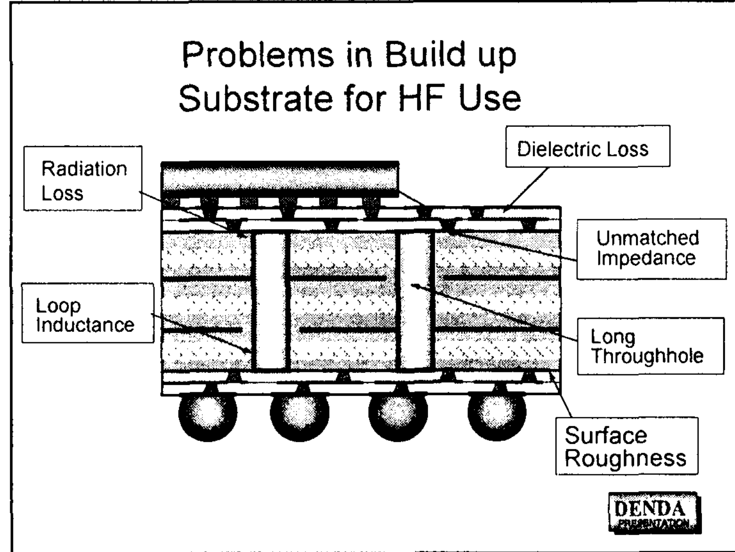
DENDA PRESENTATION



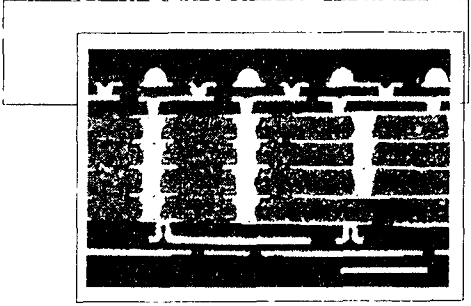


Factors for High Frequency Package Substrate

- Small signal attenuation
  - ⇨ small ε and small $\tan\delta$
- Signal delay
  - ⇨ decreasing ε ,L, C
- Crosstalk between wirings
  - ⇨ line structure
- Impedance matching
  - ⇨ substrate design



All IVH Core Build up Substrate (Kyocera)



(2-5-2)

LCP+PI, 50u

IVH pitch 250u, BU via 155u

High Density with Buildup and
High frequency with Core

Insulation Materials for HF Package

Material	ε	tan δ
Epoxy	4.7	0.02-0.007
Polyimide	3.1-3.8	0.01-0.002
Liquid Polymer LCP	3.0	0.003
Porous Polyimide	2.2	0.0024
Low Temp Ceramics LTCC	7.8	0.0003
Closed Pore Ceramics	4.2	0.0007
PTFE Polytetrafluroethylene	2.1	0.0003

Thin Film PI Interposer (NEC)

MLTF Metal-Layer Thin-Film Packaging

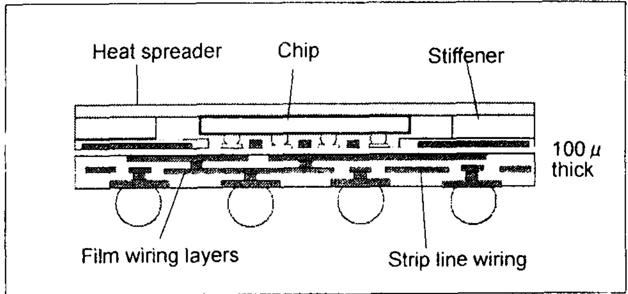
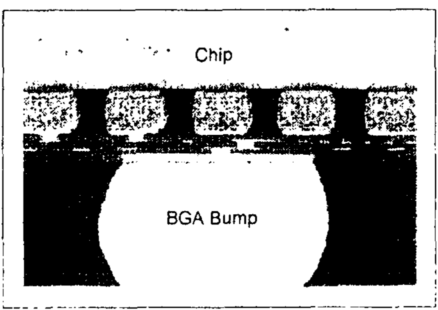


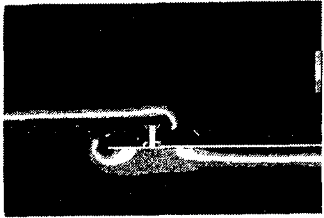
Photo sensitive PI, ε =3.1, tan δ =0.002, Cure at 350C, 2500 FC Pad, 1296 BGA Pad, via/land=40/60 μ, L/S=10 μ -20 μ.

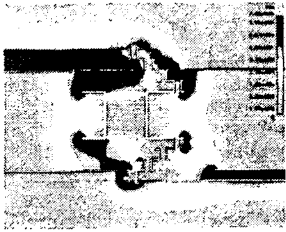
MLTF Package Cross Section



HF Package Substrates

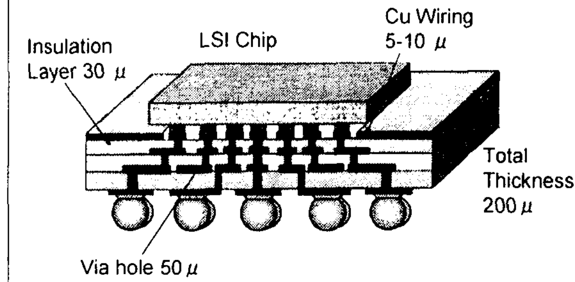
Electromagnetic Field Analysis





Thin Film 4 Layers　　Build up 4-2-4 Layers

PI Tapestack Coreless Substrate (Toppan)



Real to Real Production, L/S=/1515 μ

Increasing Thin Chip Application

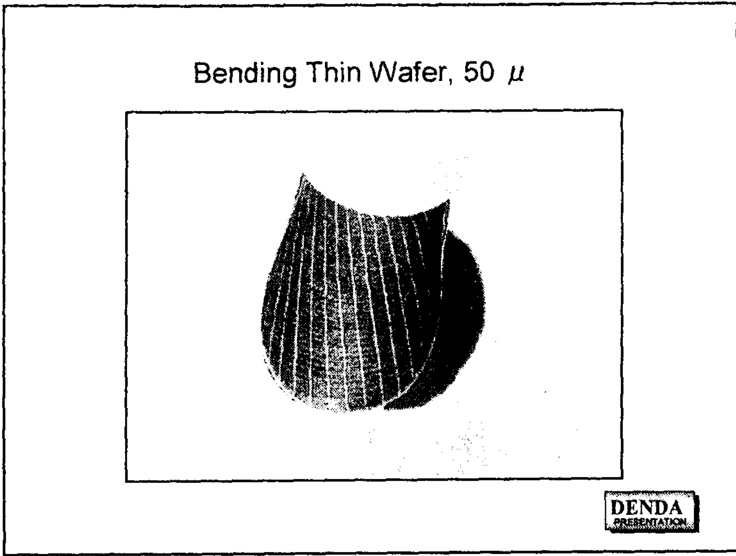
Backgrind
150mm Wafer: 350 μ
200mm Wafer: 500 μ ⇒280-350 μ
300mm Wafer: 750 μ ⇒280-350 μ

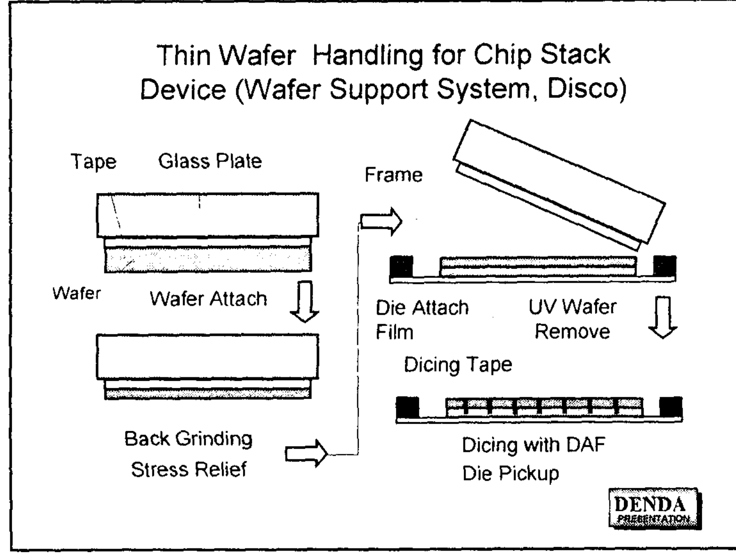
0.5mm Thick BGA: 140 μ
4 chip stack:85 μ
SD Memory Card : 70 μ
PTP: 50 μ
IC card:50 μ
3D Wafer stack: 50 μ
RF ID, IC tag: 30 μ
SiP stack device: 25~50 μ
Experimental: 10 μ

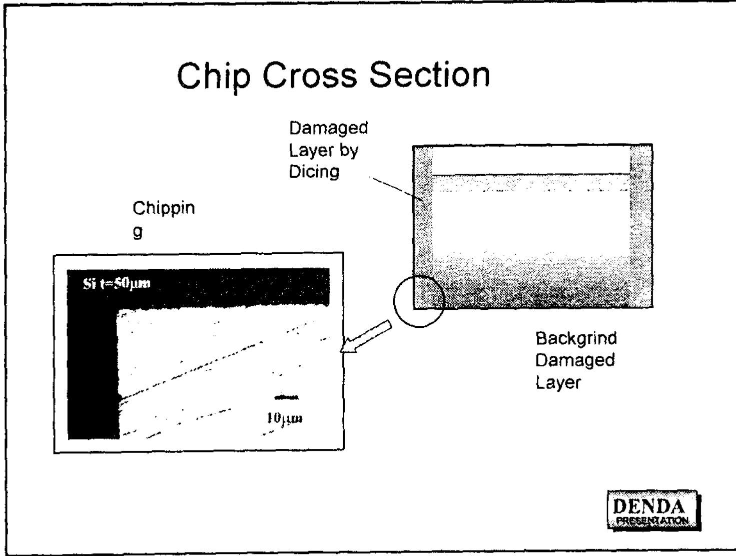
More Thin Chips Required

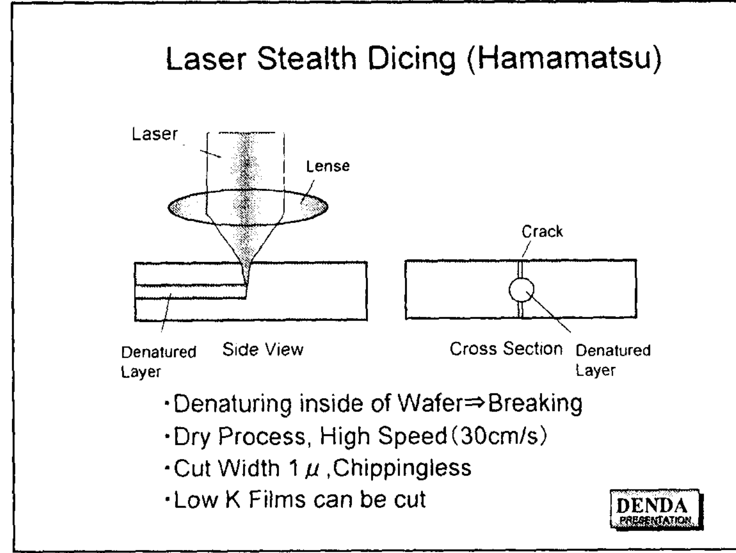
Problems with Thin Silicon Wafers and Chips

- Wafer warp (bend) due to CTE difference
- Warped thin wafer is hard to handle
- Dicing thin wafer is not easy
- Backgrind adhesive tape is hard to remove
- Chips are likely to break in die pickup, die bonding and wire bonding

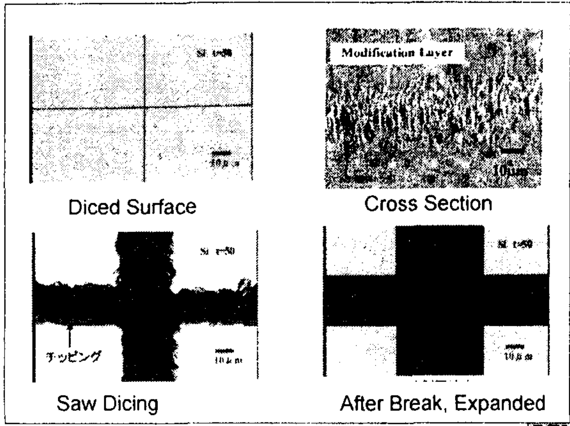

Bending Thin Wafer, 50 μ
DENDA
PRESENTATION


Thin Wafer Handling for Chip Stack
Device (Wafer Support System, Disco)
Tape
Glass Plate
Wafer
Wafer Attach
Back Grinding
Stress Relief
Frame
Die Attach
Film
UV Wafer
Remove
Dicing Tape
Dicing with DAF
Die Pickup
DENDA
PRESENTATION


Chip Cross Section
Damaged
Layer by
Dicing
Chippin
g
Si t=50μm
10μm
Backgrind
Damaged
Layer
DENDA
PRESENTATION

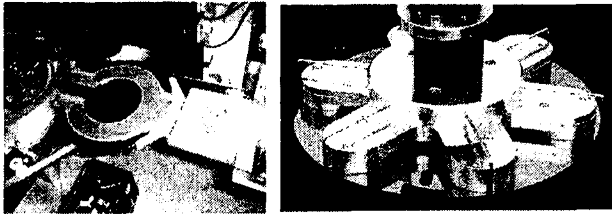

Laser Stealth Dicing (Hamamatsu)
Laser
Lense
Crack
Denatured
Layer
Side View
Cross Section
Denatured
Layer
・Denaturing inside of Wafer⇒Breaking
・Dry Process, High Speed(30cm/s)
・Cut Width 1 μ ,Chippingless
・Low K Films can be cut
DENDA
PRESENTATION

Stelth Dicing



DENDA PRESENTATION

Handling of Thin Wafer (Harmotec)



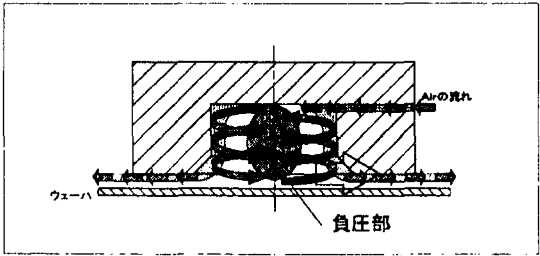
Folk Tool

Circle Tool

8 inch, 50 μ Wafer Transport

DENDA PRESENTATION

Handling of Thin Wafer (Harmotec-Kumade)



Bernui Head Produces Negative Pressure , Noncontact Handling

DENDA PRESENTATION

Lead Free Solder

Components, Tmax 240℃

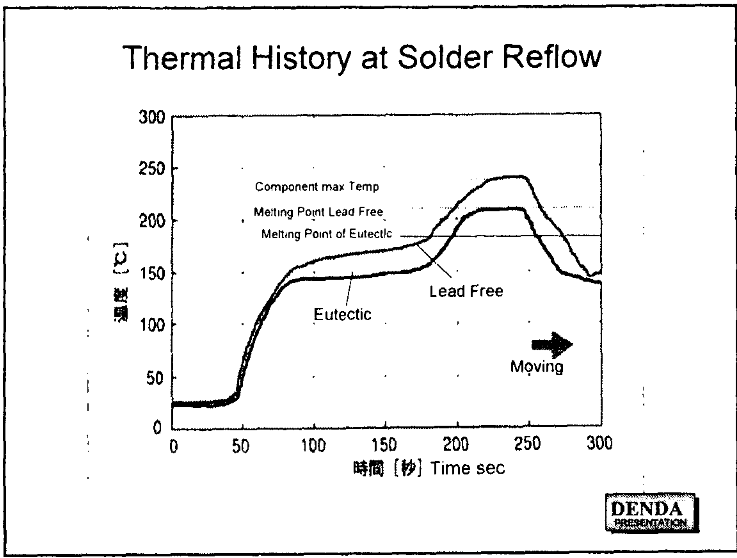
Furnace Temp max+30℃

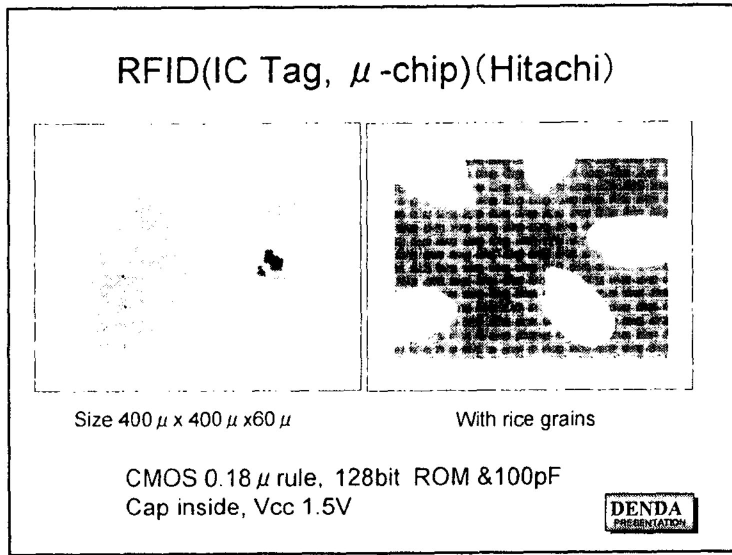
Sn-39Pb Eutectic

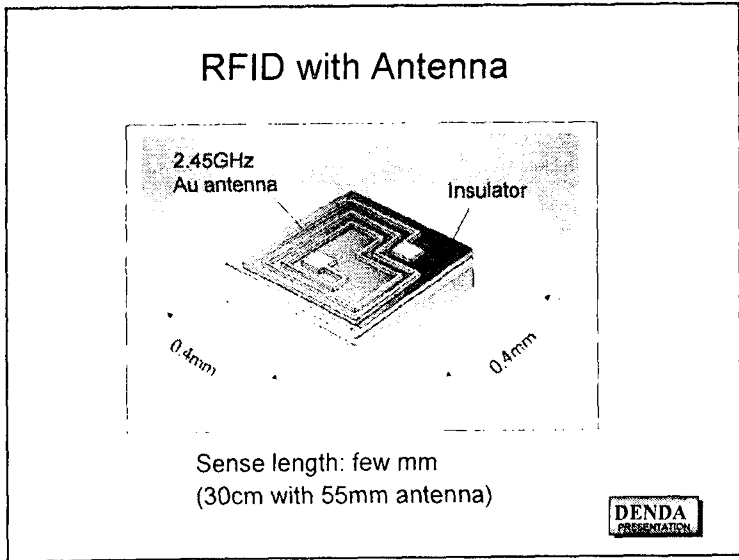
183℃

Alloy	Melting point	Notes
Sn-3Ag-0.5Cu	217℃	・Reliability ・High Cost with Ag ・Components Tmax ・Video Camera-Sony
Sn-8Zn-3Bi	190℃	・Medium Reliability ・Conventional Equipment ・N2 Atmosphere ? ・PC-NEC
Sn-3.5Ag-0.5Bi-8In	196℃	・Reliability ・In Cost ・Conventional Equipment

DENDA PRESENTATION


Thermal History at Solder Reflow
300
250
200
150
100
50
0
温度 [℃]
Component max Temp
Melting Point Lead Free
Melting Point of Eutectic
Lead Free
Eutectic
Moving
0
50
100
150
200
250
300
時間 [秒] Time sec
DENDA
PRESENTATION


RFID(IC Tag, μ-chip)(Hitachi)
Size 400 μ x 400 μ x60 μ
With rice grains
CMOS 0.18 μ rule, 128bit ROM &100pF
Cap inside, Vcc 1.5V
DENDA
PRESENTATION


RFID with Antenna
2.45GHz
Au antenna
Insulator
0.4mm
0.4mm
Sense length: few mm
(30cm with 55mm antenna)
DENDA
PRESENTATION