Design and Measurement of SFQ OR Gate that is Composed of a D Flip-Flop and Confluence Buffer

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We have designed and measured a SFQ(Single Flux Quantum) OR gate for ALU (Arithmetic Logic Unit). We have done simulation and layout by using WRspice, XIC and Lmeter. This OR gate circuit is a combination of Confluence Buffer and one D Flip-Flop. When two data enter a same time, Confluence buffer does butter action. A role of D Flip-Flip is expelled a data when clock is entered into D Flip-Flop. For a measurement of OR gate operation, we attach three DC/SFQ, three SFQ/DC and one RS Flip-Flop to OR gate. SFQ pulse.is generated from DC/SFQ circuit and entered in OR gate. DC/SFQ circuit is used data and clock. Input frequency of 10kHz and 1MHz are entered in DC/SFQ. Output date from OR gate go to RS flip-Flop. We show output date of OR gate using oscilloscope that connect to RS Flip-Flop. We obtain bias current margins of D Flip-Flop and Confluence Buffer through measurement. This margin is each ±38.6% and ±23.2%. This OR gate was measured to inside of liquid helium.

keywords : SFQ, OR-gate, superconductor