

The Fabrication of Micro-Heaters with Low-Power Consumption Using SOI and Trench Structures

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Abstract

This paper presents optimized design, fabrication and thermal characteristics of micro-heaters for thermal MEMS (micro electro mechanical system) applications using SOI and trench structures. The micro-heaters are based on a thermal measurement principle and contains thermal isolation regions of 10 μm -thick Si membranes consisting of oxide-filled trenches in the SOI membrane rim. The micro-heaters were fabricated with Pt-RTD on the same substrate via MgO buff layer between Pt thin-film and SiO₂ layer. The thermal characteristics of micro-heater with trench-free SOI membrane structure was 280° C at input power 0.9 W; in the presence of 10 trenches, it was 580° C due to reduction of the external thermal loss. Therefore, a micro-heater with trenches in SOI membrane rim structure provides a powerful and versatile alternative technology for enhancing the performance of micro-thermal sensors and actuators.

Key Words : Micro-heater, SOI, trench, membrane, Pt-RTD, power consumption, MEMS, sensor, actuator

1. INTRODUCTION

A great interest is recently put into the development of a small size, lightweight, high-speed response and a new functional MEMS (micro electro mechanical system) using Si micromaching technology [1]. In particular, fabricating thermal micro-sensors (velocity of fluid/flux, gas, vacuum, etc.) and micro-actuators (valve, pump, etc), it is required to use micro-heaters with a low-power consumption, an exact temperature control and a low thermal capacity. Such fulfillment may provide a thermal activation and a thermal control in the ultra-microscopic area, facilitate a sensor array and integration, and have a high-TCR (temperature coefficient of resistance) and do the excellent variation of resistance and linearity with temperature [2-3].

Si membranes are widely used for MEMS applications because of their excellent electrical and mechanical properties. However, in the case of building up micro-heaters on Si substrate, to reduce big thermal conduction of Si embedded structure is one key factor in fabricating effective micro-heaters. Accordingly, in such a structure, a part of thermal insulation between outside and micro-heater necessarily required for reducing the heat loss, using MEMS techniques. In order to do this, and to enhance the heating characteristics of the low-power consumption in the fabrication of the micro-heaters, many researches have been actively made on the micro-heaters using the thin-films such as poly-Si, NiFe Alloy, NiCr, Pt/Ti, Pt/Cr, Pt/Al₂O₃, Pt/MgO deposited on the air-floating structures, the cantilevers and the bridges consisting of dielectric materials of NON (Si₃N₄/SiO₂/Si₃N₄), respectively [4-13].

However, although the micro-heaters implemented on the NON show high-thermal characteristics, the weakness to a mechanical shock causes problems in their applications of integration with other the MEMS devices. Consequently, the fabrication of the micro-heater of a low-power consumption on Si membranes should be made prior to the development of integrated thermal MEMS.

This paper, therefore, describes on a design of an optimized micro-heater by analyzing the numerical thermal distribution with the number and width of the trenches on the Si membrane. In the fabrication, the Pt thin-film micro-heater and the RTD (resistance thermometer device) facilitating the control and measurement of the temperature of an ultra-micro region were integrated into the same substrate where SOI (Si-on insulator) membrane and the trench structure are already made with the MgO buffer layer intermediating of Pt thin-films. Finally, the TCR and the variation rate of resistance of the Pt thin-film were analyzed as a function of temperature, and thermal characteristics of the micro-heater were evaluated with variation of applied power.

2. EXPERIMENTAL PROCEDURE

2.1 Design

The micro-heater was designed by using the two-dimensional FED (finite difference method) simulation for the thermal insulation of the SOI and trench structures. The two-dimensional FDM simulation is programmed with ANSYS so that the micro-heater on the SOI membrane analyzes the thermal distribution of the thermal conduction outwards [3]. In this work, the value of heat loss caused by the radiation and convection was excluded in the heat analysis of the Si membrane, since the value was negligibly smaller than that caused by a thermal

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conduction. The thermal conduction is a phenomenon that heat is transferred between certain materials where q , a heat capacity is simulated with k , a thermal conductivity as a proportional constant and a variation rate of temperature by the Fourier law, as shown in equation 1.

$$q = -k \cdot \nabla T \quad (1)$$

Besides, applied power in the simulation is to be constantly consumed in the micro-heater at the temperature of 25° C. From the simulation, it was turned out to have the better heating property in heater structures with the larger values in number, width and gap of the trenches. The number of the trench is set preferably in consideration of the size of devices.

2.2 Fabrication

SDB (Si-wafer direct bonding) SOI substrate with 10 μm -thick was used for fabricating Si membranes. Fig. 1 shows schematic procedures of the fabrication process.

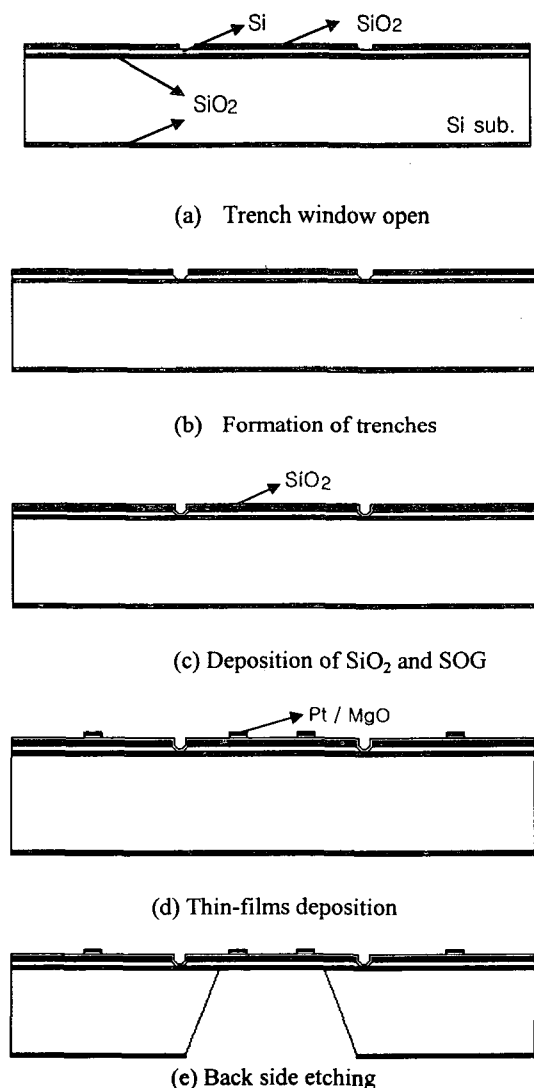


Fig. 1. Fabrication process sequence of a Pt thin-film micro-heater with trenches on the SOI membrane.

First, the substrate with 0.2 μm -thick thermally grown SiO_2 was patterned, using photolithography process in order to form a trench of 10 μm in depth, 15 μm in width and 15 μm of gap, respectively. Oxidation layer was removed with the buffer solution ($\text{HF}:\text{NH}_4\text{F}:\text{H}_2\text{O} = 15:10:100$) and then the trenches were formed by an isotropic etching (TMAH 20 wt.%, 80° C) [14]. In order to enhance the thermal insulation and mechanical characteristics of the trench, an oxidation layer of 1.0 μm was grown and SOG (spin-on-glass) was filled there. MgO thin-films were used as a mediation layer of Pt thin-films. In this case, MgO thin-films can prevent debonding and reaction between SOI and Pt thin-films during the high-temperature annealing process. Thus, a superior insulation in annealing, enhancement in the adhesiveness of the Pt thin-film and facilitation in the formation of the micro-pattern for the micro-machining technique as well as having a high-heat proof can be achieved [15]. Moreover, the RTD and the micro-heater having an active region of $400 \times 400 \mu\text{m}^2$ were integrated into the same substrate by using the Pt thin-film heater with a good linear response, and chemically and thermally good stability [16-17]. The Pt thin-film was deposited with 2 in. Pt target of 99.99 % by DC magnetron sputtering. Finally, the SOI membrane with $500 \times 500 \mu\text{m}^2$ size were formed by the anisotropic etching technique.

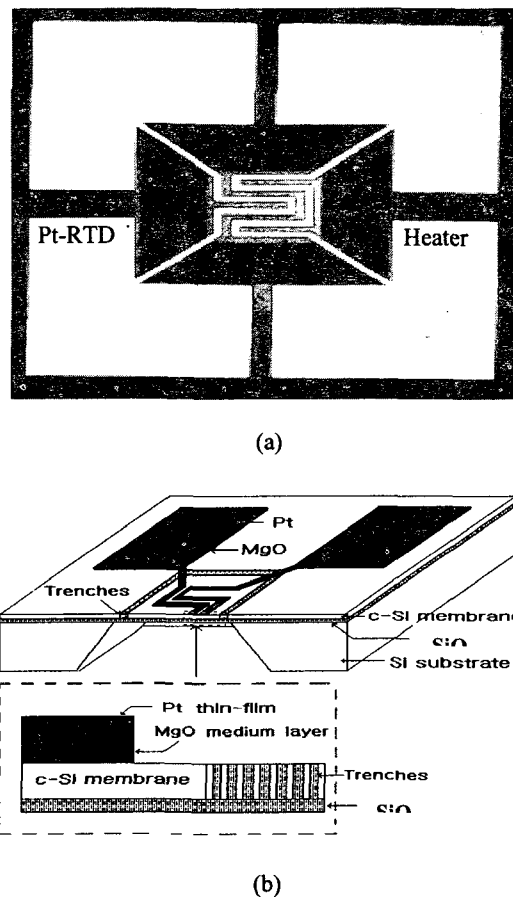


Fig. 2. (a) Surface photograph of a Pt thin-film type micro-heater and Pt-RTD fabricated on the SOI membrane and trench structure, and (b) its cross-sectional view.

Fig. 2(a) and (b) show the surface photograph and the cross-sectional view of Pt thin-film type micro-heater integrated with Pt-RTD, also, built up MgO a medium layer on the SOI membrane and the trench structure. The as-fabricated micro-heater and Pt-RTD were annealed in quartz tube furnace under N₂ atmosphere at 1000° C for 120 min and then evaluated analytically for its characteristics [17].

3. RESULTS AND DISCUSSION

Fig. 3 shows results of temperature distribution simulation of the micro-heater as a function of the numbers of trench on the SOI membrane, in which direction is shown from the center of the membrane to 580 μm. In this work, the trench has a fixed 15 μm width and simulation results for 0, 4 and 10 trenches under the applied power of 0.6 W were carried out. It is known that quantity of heat of the micro-heater was uniformly distributed on the SOI membrane, since the trenches cut off the thermal conduction by the SOI membrane. In this case, the thermal loss was reduced. Also, it is shown that the temperature distribution is much more improved by forming the trench than that in the case of trench-free structure. Therefore, the thermal blocking of the trench was so effective for the reason of a rapid thermal distribution reduction in the region of their presence. Moreover, the more number of trenches has the better low-power consumption by blocking the thermal conduction from the SOI membrane to the bulk Si.

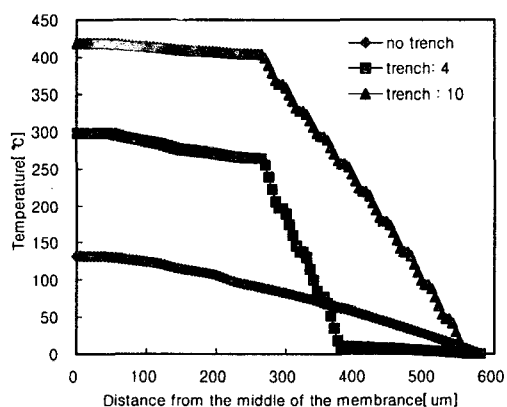


Fig. 3. FDM simulated temperature distribution of a micro-heater in one direction as a function of the distance from the middle position of the membrane according with number of trenches on the SOI membrane.

Fig. 4 shows FDM simulated temperature distribution of the micro-heater as a function of the width of the trenches on the SOI membrane. When the numbers of the trench are 4 and the gap among the trenches is fixed into 15 μm, it was also simulated for the width of 5, 10, 20, 30 and 40 μm, respectively. We may know that the wider the trench is, the smaller the thermal loss in the part of membrane is in Fig. 4.

Fig. 5 shows SEM images of Pt thin-films deposited on MgO films at different annealing temperatures. They have

a uniform surface before annealing. This surface is favorable to form a micro-patterning. On the other hand, large crystal grains were formed after the annealing at 1000° C for 120 min.

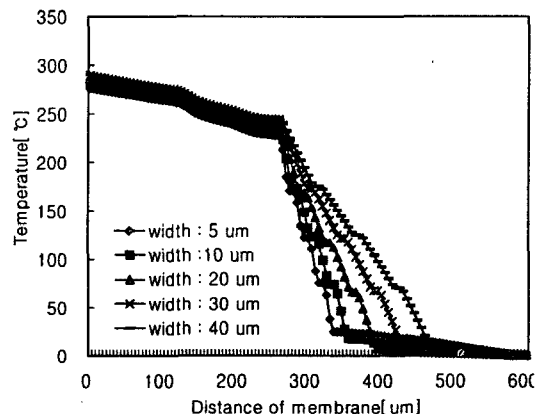
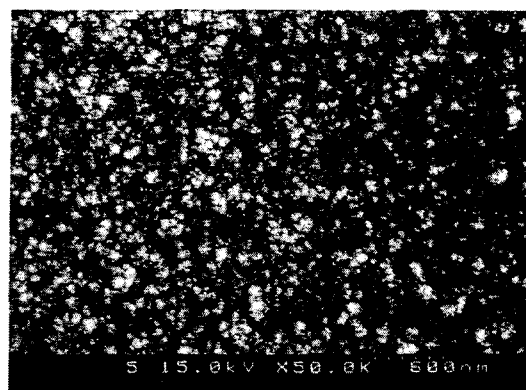


Fig. 4. FDM simulated temperature distribution of a micro-heater in one direction as a function of the distance from the middle position of the membrane as a function of width of trench on the SOI membrane.



(a)



(b)

Fig. 5. SEM images of Pt thin-films deposited on MgO films (a) without annealing and (b) with annealing temperature at 1000° C for 120 min.

Moreover, the variations in electrical resistivity and sheet resistivity of Pt thin-films deposited on MgO films were evaluated. The electrical resistivity of Pt thin-films is the product of the thickness measured by ellipsometer multiplied by the electrical sheet resistivity measured by a four-point probe method. The electrical sheet resistivity and the electrical resistivity before annealing and after annealing, respectively, were measured to be $0.246 \Omega/\square$, $24.6 \mu\Omega \cdot \text{cm}$ and $0.1288 \Omega/\square$, $12.88 \mu\Omega \cdot \text{cm}$. These results indicate that it is close to the value of the electrical resistivity of the Pt bulk, namely, $10.8 \mu\Omega \cdot \text{cm}$ [17]. Consequently, it is found that the physical and electric characteristics of Pt thin-films deposited on MgO films are drastically improved through the annealing process.

Fig. 6 shows XRD patterns of Pt thin-films deposited on MgO films for showing the enhancement of Pt crystallinity via annealing effects. It can be seen that before and after annealing, only the peak Pt thin-films (2θ) appears conspicuous in the vicinity of 39.6° and that the intensity of the main peak in XRD pattern increased, but the residual peak were greatly reduced via annealing process. Therefore, after annealing process, the Pt thin-film has no significant chemical reaction with the MgO film, which retains its own characteristics [15].

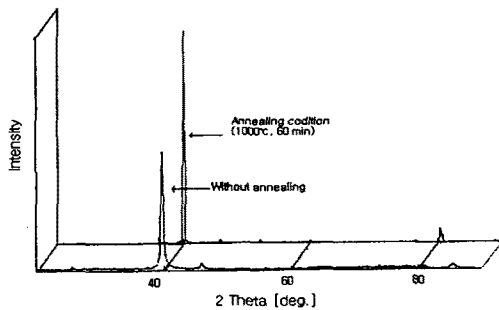
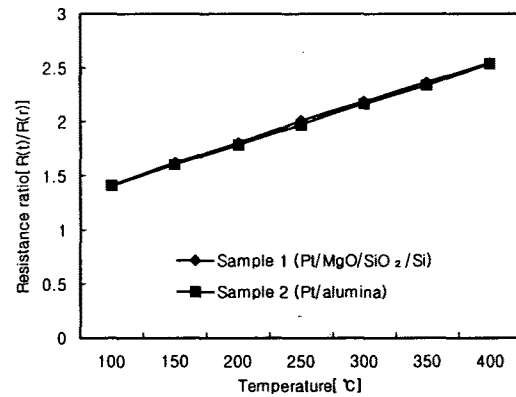


Fig. 6. XRD patterns of Pt thin-films deposited on MgO films without annealing and with annealing at 1000°C for 120 min.

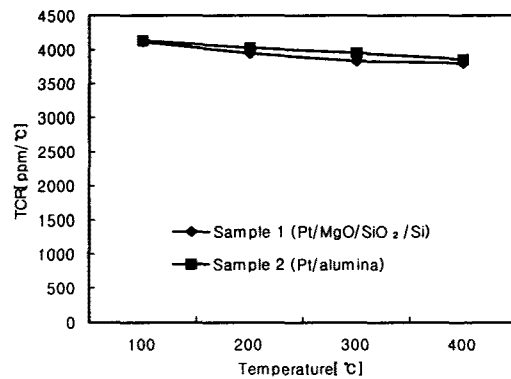
Figs. 7(a) and (b) show the variations of the resistance ratio and the TCR value of Pt-RTD fabricated on Si (Samples 1) and Al_2O_3 (Samples 2) substrates, respectively. The variation rate of the resistance was measured in the temperature range from a 25 to 400°C under N_2 atmosphere. The resistance ratio of samples 1 and 2 were found to be similar, and were almost a straight line with respect to the variation of measuring temperature. This indicates that both samples have a good linearity. Moreover, the TCR value of sample 1 was $3927 \text{ ppm}/^\circ\text{C}$. This value was much similar to that of bulk of Pt [14]. Owing to the standard deviation of $0.7 \text{ ppm}/^\circ\text{C}$, it is assured that it has a superior linearity.

Fig. 8 shows thermal characteristics of Pt micro-heaters implemented at different substrate structures as a function of applied power; type I is Pt micro-heaters formed on Si substrate; type II is Pt micro-heaters built on Si membrane [13]; type III is Pt micro-heaters fabricated on SOI membrane; and type IV is Pt micro-heaters implemented on the membrane of SOI with trench structures.

The number of the trenches: 10, the width: $15 \mu\text{m}$ and the gap: $15 \mu\text{m}$ were used. Also, in all types, MgO layer was



(a)



(b)

Fig. 7. Variations of (a) the resistance ratio and (b) the TCR value of Pt-RTD fabricated on Si and Al_2O_3 substrates, respectively.

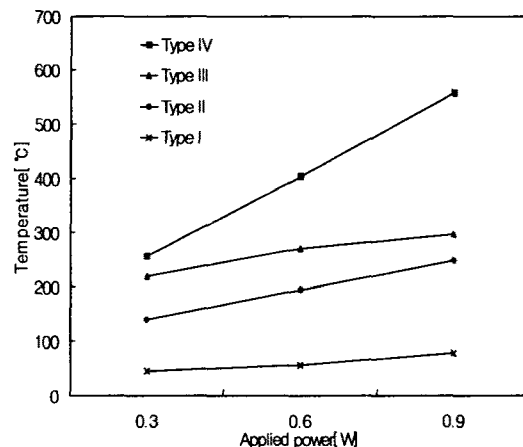


Fig. 8. Thermal characteristics of micro-heaters fabricated on a Si substrate, Si membrane, SOI membrane and SOI membrane with trenches, respectively.

as a medium layer. It is known that the type I has a low heating characteristic due to high thermal conductivity of Si. In comparison with the type I, the heating characteristic of the type II was improved by the presence of the membrane formed to reduce the thermal loss. The type III thermal characteristic was also improved via SOI membrane, resulting blocking the thermal conduction towards Si bulk. Moreover, the type IV, the thermal loss of the thermal conduction towards Si side was significantly reduced and thus the effective heat insulation from outside was shown via a structure of trench. As a result, a high heat characteristic above 580° C was observed in the Pt micro-heater structure having SOI membrane and trenches at an applied power of 0.9 W.

4. CONCLUSION

This paper describes on design, fabrication, measurement and analysis of a micro-heater with MgO thin-films used as a medium layer on an SOI membrane, and a trench at a rim of the membrane was used. Thin-film type Pt-RTD was also integrated on SOI membrane structure. By forming a trench at a rim of the SOI membrane, the thermal loss due to the conduction was reduced by insulating heat from outside. In such structure, heating characteristic was greatly improved. The more numbers of trenches are formed and the larger width and gap of the trench has, the more efficiently the micro-heater distributed the heat throughout the membrane. This improved the thermal isolation as well as reduced the thermal loss. Therefore, when fabricating the micro-heater, an exact control of operational temperature was enabled with the low-power consumption as minimized the thermal influence on external circuit, by configuring trenches at the rim of the SOI membrane.

On the other hand, the MgO thin-film as a medium layer improved the adhesion of Pt on SOI. It provided a perfect insulation without any chemical reaction during very high temperature annealing. The TCR value of the integrated thin-film type Pt-RTD was an average of 3927 ppm/° C. Its linearity was so good that the deviation was 0.7 ppm/° C, meeting the DIN and JIS standards. Furthermore, the Pt thin-film micro-heater fabricated effectively isolated heat flow from outside. Superior thermal characteristic over 580° C was observed at the applied power of 0.9 W.

Consequently, the thin-film type Pt-RTD and micro-heater employed MgO films as a medium layer, on the structure of SOI membrane along the trenches formed on its rim are expected to be applied for developing an integrated micro-thermal sensors and an actuators

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References

1. P. M. Sarro, *Sensors & Actuators A*, 31, 138, 1992.
2. M. A. Gajda and H. Ahmed, *Sensors & Actuators A*, 49, 51, 1995.
3. L. Qui, E. Obermeier and A. Schubert, *Tech. Dig. IEEE Int. Conf. on Solid-State Sensors & Actuators*, p. 520, IEEE, Sweden, 1995.
4. M. Parameswaran, *IEEE Electron Device Letters*, 13, 57, 1991.
5. E. Yoon and K. D. Wise, *IEEE Trans. Electron Devices*, 39, 1376, 1992.
6. J. W. Gardner, A. Pike, N. F. de Rooij, M. K. Hep, P. A. Clerc, A. Hierlemann and W. Gopel, *Sensors & Actuators B*, 26, 135, 1995.
7. U. Dibern, *Sensors & Actuators B*, 2, 63, 1999.
8. V. V. Luchinin, *Tech. Dig. Of the 7th Sensor Symp.*, p. 30, IEE, Japan, 1996.
9. U. Dibern,, *Sensors & Actuators B*, 2, 63, 1990.
10. D. Mutschall, C. Scheibe and E. Obermeier, *Tech. Dig. IEEE Int. Conf. on Solid-State Sensors & Actuators*, p. 256, IEEE, Sweden, 1995.
11. S. H. Lee, I. C. Sub and Y. K. Sung, *J. Korean Sensors Society*, 5, 69, 1996.
12. G. S. Chung, S. S. Noh, *Sensors & Materials*, 10, 251, 1998.
13. G. S. Chung, S. W. Hong, *J. KIEEME*, 13, 509, 2000.
14. G. S. Chung, *Sensors & Materials*, 12, 133, 2000.
15. G. S. Chung and S. W. Hong, *J. Korean Sensors Society*, 9, 171, 2000.
16. G. S. Chung and S. S. Noh, *J. KIEEME*, 9, 911, 1996.
17. G. S. Chung and S. S. Noh, *J. Korean Sensors Society*, 6, 81, 1997.