The Fabrication of SDB SOI Structures with Buried Cavity for Bulk Micro Machining Applications

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Abstract

This paper described on the fabrication of microstructures by DRIE(deep reactive ion etching). SOI(Si-on-insulator) electric devices with buried cavities are fabricated by SDB technology and electrochemical etch-stop. The cavity was fabricated the upper handling wafer by Si anisotropic etch technique. SDB process was performed to seal the fabricated cavity under vacuum condition at −760 mmHg. In the SDB process, captured air and moisture inside of the cavities were removed by making channels towards outside. After annealing(1000℃, 60 min.), The SDB SOI structure was thinned by electrochemical etch-stop. Finally, it was fabricated microstructures by DRIE as well as an accurate thickness control and a good flatness.

Key Words : DRIE(Deep Reactive Ion Etching), SOI(Si-on-insulator), SDB(Si-Direct-Bonding)

1. Introduction

As being easy to make microstructures by Si micromachining, recently, the study is being actively progressed to fabricate MEMS(Micro Electro Mechanical System). Si micromachining technology divides the bulk micromachining technology which fabricates three-dimensional microstructures by anisotropic etching and the surface micromachining technology which makes the microstructures by the sacrificial layer etching and the thin film deposits on the surface of Si wafer. Mechanical devices which are fabricated by the bulk micromachining are large and relatively high cost. Being fabricated by the anisotropic wet etching technique in KOH or TMAH solutions, the structural shapes are restricted by the limitation of Si crystal silicon. Also, because the surface micromachining technology uses the growing multi-layers or the deposition on Si wafer, the vertical size of the structures is limited that thickness of the deposition or growing thin film is 10 ~ 20㎛. The residual stresses and the stress gradients in the thin film place limitations on the lateral dimensions. So, to fabricate the high-quality or micro MEMS using Si micromachining technology, the good mechanical characteristics can be used of the former IC manufactural technology, Si foundry and single crystal Si. It is developing the method of using the Si sacrificial layer which makes the active devices or the surface microstructures: the SOI which has the single-crystal Si on the insulator achieves an electric insulator and a chemical sacrificial layer[1-2].

The SDB can fabricate the Si thin film which has the perfect single-crystal and the SOI substrate which has the large area and the buried cavity oxidation with good insulator. Especially, it can simply make the thick film for

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Si bulk micromachining with the buried cavity or the three-dimensional microstructures. Also, the thin film diaphragm, the cantilever, and the bridge are accurately fabricated[3]. Now, it is being developed actively because of using the good electric-mechanical characteristics of the single-crystal Si in the MEMS area [4-5]. It is the most important to the method for thinning and the accurate thickness control of SOI active layer to use the SDB SOI technology in the MEMS area. The electrochemical etch-stop is the safest of the thickness control technologies. And it can control some dozens of Å of the final surface roughness and the thickness within 0.2 ㎛.

Consequently, we has fabricated the SOI substrate with buried cavity and has investigated the flatness of the etched surface and the thin film thickness, applying electro-chemical etch-stop to the method for thinning of SDB SOI substrate. Also, we has made the three-dimensional microstructures for Si bulk micromachining, using DRIE.

2. Fabrication of SDB SOI structures with buried cavity

The Si wafer has (100) crystal directions. The p-type handling wafer of the growth of 5000 Å thermal oxide and the active layer of the growth of the n-epi. of 15 ㎛ on the p-sub. which has the (100) crystal directions have been used. The size is 3.0 cm x 3.0 cm.

Figure 1 shows the fabrication process of SOI structure with buried cavity. The p-type handling wafer among the wafers of the growth of thermal oxide has had, before processing SDB, the anisotropic etch toward the n-epi. since having electrochemical etch-stop. The wafer has had the anisotropic is the p-sub./n-epi.. We have processed the early junction after pre-treating for one minute in the solution of HF 2.0%[6]. After the pn junction has treated with heat for 60 minutes at 1000 ℃, we has fabricated the SOI structure with buried cavity as controling the thickness of n-epi. layer by electrochemical etch-stop. We has used the pn junction to fabricate the SOI structure with buried cavity. The anisotropic etch solution has kept a 20 wt.% TMAH one at 80 ℃.

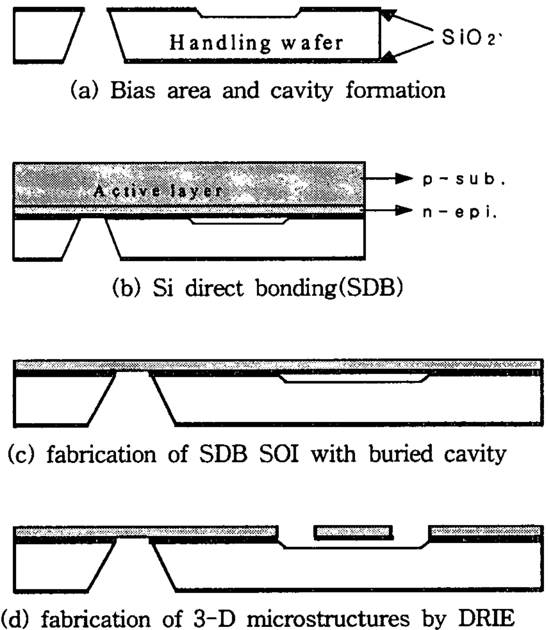


Fig. 1. Fabrication process of SOI structures with buried cavity.

3. Result and Discussion

Figure 2 shows the leakage current-voltage characteristic curve of p-type in a 20 wt.% TMAH solution at 80℃. The scan rate is 5㎷/sec and the voltage is -2 V ~ 2 V. As OCP point is -1.4 V, the leakage current has been increased continually until arriving at PP point. At PP point of 1.2 V, the leakage current which has been increased spirally is suddenly decreased on the Si wafer by the passivation. The highest current density has measured about 0.5㎃/㎠, and the leakage current density has kept 0.035 ~ 0.046㎃/㎠ after having been etch-stopped.

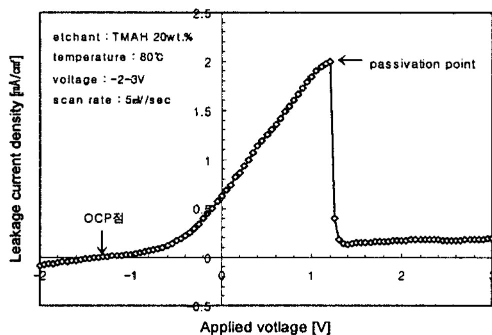
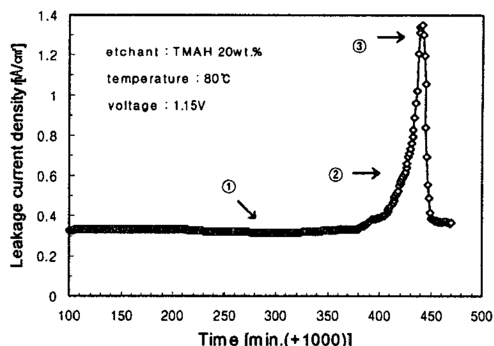
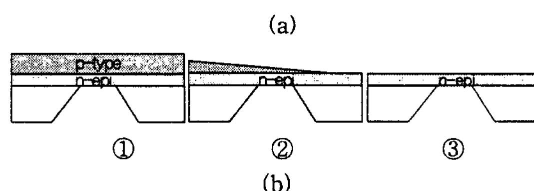


Fig. 2. Leakage current-voltage characteristic curve of p-type Si wafer.

Figure 3(a) shows the leakage current-time characteristic curve at electrochemical etch-stop. Using the RE electrode in three-electrode system, the leakage current has been kept regularly in the Si etching course. After the p-type Si has been etched, the leakage current has been increased abruptly when n-epi. Si has been appeared in etched solutions. When the n-epi. Si has been appeared wholly, the etching has been stopped by the passivation of the chemical reaction with etched solutions. Figure 3(b) shows the etch-stop step. ① is the etched situation that the p-type Si has been appeared by the oxidation- reduction in etched solutions. ② shows that the surface of p-type Si has been appeared wholly in the etched solutions and then the leakage current of pn junction has been increased abruptly. ③ presents that the p-type Si has been etched perfectly and the etching has been stopped by the passivation in the n-epi. Si. Figure 4(a) and (b) are the AFM images of Si wafer and SDB SOI substrates with buried cavities etch-stopped by electrochemical etch-stop in a 20 wt.% TMAH solution. Each average roughness of Si wafer and etch-stopped SOI substrates is 5.12 nm and 5.4nm. In the case of thinning SDB SOI by electrochemical etch-stop, the flatness of etch-stopped SOI substrates is much better than the former electric method, and corresponds to that of Si wafer[7].

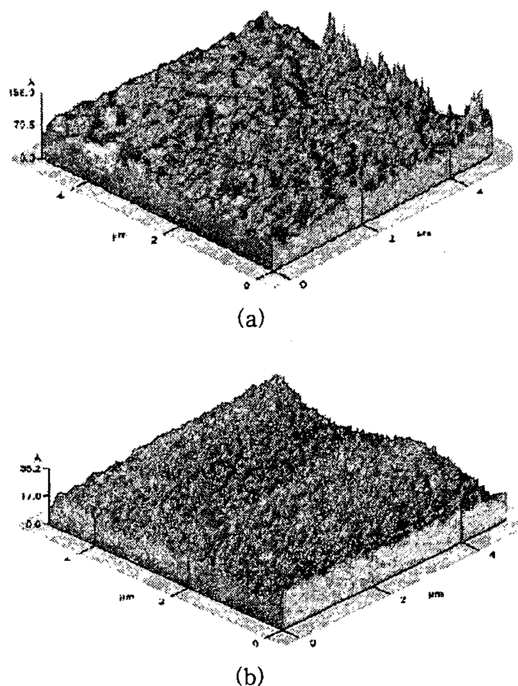


(a)



(b)

Fig. 3. (a) Leakage current-time characteristic curve at electrochemical etch-stop and (b) etch-stop step.

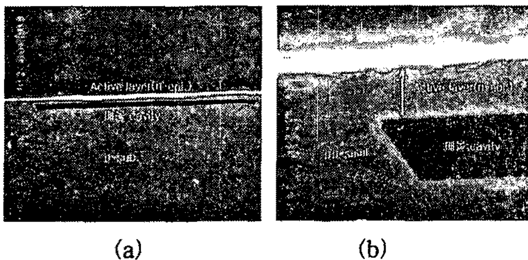


(a)

(b)

Fig. 4. AFM images of (a) Si wafer and (b) SOI substrates with buried cavities etch-stopped by electrochemical etch-stop in TMAH solution, respectively.

Figure 5 shows the sectional SEM photography of SOI structure with buried cavity by SDB and electrochemical etch-stop technique. This experiment has successively achieved SDB and electrochemical etch-stop progress using the handling wafer(p-type) and the p-sub./n-epi.(15 ㎛) wafer. The thickness of active layer over etch-stopped cavity is 15㎛, each of the depth and the width is 18, 900㎛. Figure 5(a) and (b) is the SDB SOI structure with buried cavity cross sectional view and the SEM image.



(a) (b)

Fig. 5. SDB SOI structure with buried cavity (a) cross sectional view (b) SEM image.

4. Conclusion

Applying electrochemical etch-stop to the method for thinning of SDB SOI substrate, we has fabricated the SOI substrate of structure with buried cavity and then has investigated the flatness of the etch-stopped surface and the thin film thickness. Also, the three-dimensional microstructures for Si bulk micromachining have been achieved by DRIE technology. First, after making buried cavity it has been fabricated SDB SOI structure, and then PP point and OCP point have been analyzed. SDB SOI structure with buried cavity, active layer thickness is 15*um* and each width and depth is 18, 900㎛, has been fabricated by electro-chemical etch-stop. And then the possibility of SDB SOI structure with various buried cavity has been realized.

Consequently, after making SDB SOI substrate with buried cavity, three-dimensional microstructures which are fabricated using DRIE technology can use the electric and machine quality which is very good. Because an accurate thickness control of active layer and a good flatness are obtained by electrochemical etch-stop, it can be valuably applied in MEMS area for bulk micromachining.

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