Novel Driving Technology for PDP with Multi-Level Sustainer Circuit

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Abstract – **A novel driving technology of PDP, which enables to decrease the sustain voltage of conventional technology by half without lowering the gas discharging voltage. This technology, realizable without much increased cost of the semiconductor devices, gives a significant improvement in the power efficiency, essential for the design of a drive circuit for PDP. A comparative analysis and experimental results are presented to show the validity of the proposed driving technology.**

I. INTRODUCTION

Plasma Display Panels (PDP) which has the large view angle and screen dimensions take advantages over the other competing flat panel displays and are expected to be the displays of the next generation. In an AC-PDP driver, there is a need for a high-power and high-frequency switching circuit called a 'sustain circuit', to process the required gas discharge current in the AC-PDP. The sustain circuit has a well-known full-bridge configuration[4] to convert a DC voltage to a high-frequency AC voltage. Because of a pure capacitive load characteristics of the AC-PDP, the capacitive displacement current occurred during charging and discharging the PDP, can exceed the required gas discharge current itself. Due to this displacement current, there exist considerable reactive power and power losses in the sustain circuit. To relieve these problems, many types of sustain circuits, which reduce the capacitive displacement current by adopting the LC resonant technique, have been proposed and widely used [1,2]. The displacement current and the associated power losses are significantly reduced since the reactive power is mostly recovered through the operation of an 'energy recovery circuit'. The most severe problem is that this sustain circuit is suffered not only from a gas discharge current of about *100A* during the whole gas discharging period ('sustain' period), but also from a high voltage of about *160V* for a gas discharge phenomena to be occurred. Therefore, the high-cost and low performance semiconductor devices should be used in the sustain circuit. These facts not only degrade the whole power efficiency but also result in a severe ringing in the panel voltage waveforms. Thus, it is necessary to develop an efficient sustain circuit operated under the low semiconductor device stresses for a reliable and high-efficient AC PDP driver.

In this paper, a new sustain circuit with an energy recovery operation suitable for an AC PDP driver, is introduced. The proposed circuit, based on the three-level converter techniques[3,4], features half the device voltage stresses and the significantly reduced power losses, compared to those of the conventional ones. Also, while this circuit can be realized without much increased cost of the semiconductor devices, it gives a significant improvement in the power efficiency, essential for the design of a drive circuit for the AC-PDP. A comparative analysis and experimental results are presented to show the validity of the proposed sustain circuit.

II. PROPOSED DRIVING TECHNOLOGY

Fig.1 shows the block diagram of the PDP driver based on the proposed sustain circuit and its electrical equivalent circuit during the whole gas discharging period, e.g., the sustain period are shown in Fig.2. During the sustain period, the separating circuit is always on and the other circuits such as a scan-pulse generator and a scan driver, are disabled. The proposed equivalent circuit shown in Fig.2 resembles after the three-level converter with diode clamp circuit [3,4]. By applying the proper switching sequences to the sustain switches $S_{u,i}$ and $S_{d,i}$ ($i=1,2,3,4$), the voltage across the plasma panel capacitor C_p features three voltage levels, e.g., 0, $\pm V_s/2$, and, $\pm V_s$. The dc input voltage V_s is the required voltage level to maintain the gas discharge of the plasma panel. There exist four energy recovery stages in the proposed circuit, to reduce the capacitive displacement current and the reactive power of the PDP. Each energy recovery stage is composed of an inductor L_i, pair of power *MOSFET* switches $S_{r,i}$ and $S_{f,i}$, pair of diodes $D_{r,i}$ and $D_{f,i}$, and two split input capacitors $C_{u,i}$ and $C_{d,i}$. The energy recovery operation is achieved by the resonance between the inductor L_i and the plasma panel capacitor C_p during the charging and discharging periods of the PDP.

For the analysis of the circuit operation, the following assumptions are made :

- all the power switches are ideal
- the input capacitor values are the same, e.g., $C_{u,i}=C_{d,i}=C$
- the inductor values are the same, e.g., $L_i=L$
- the input capacitance C is much larger than the panel capacitance C_p, e.g., $C>>C_p$
- the voltage across each input capacitor is considered as the constant voltage of $+V_s/4$
- the switches S_{d4} and S_{d3} are on during the half switching cycle.

The last assumption simply states that the side 2 electrodes of the PDP are held ground level during the half switching cycle. Fig.3 shows the key waveforms of the proposed sustain circuit. The detailed description of each topological state is given below.

Mode 1 ($t_0 \le t < t_1$; *pre-charging mode*): Prior to t_0, the switches S_{d1} and S_{d2} are *ON*, and the voltage across the panel capacitor C_p, v_p remains zero. The drain-to-source voltages across the switches S_{u1} and S_{u2} are the same values of $+V_s/2$. At $t=t_0$, the switch S_{d1} is tuned *OFF*, while S_{r1} is turned *ON*. In mode 1, the stored energy in input capacitor C_{d1} is transferred to the panel capacitor via the path

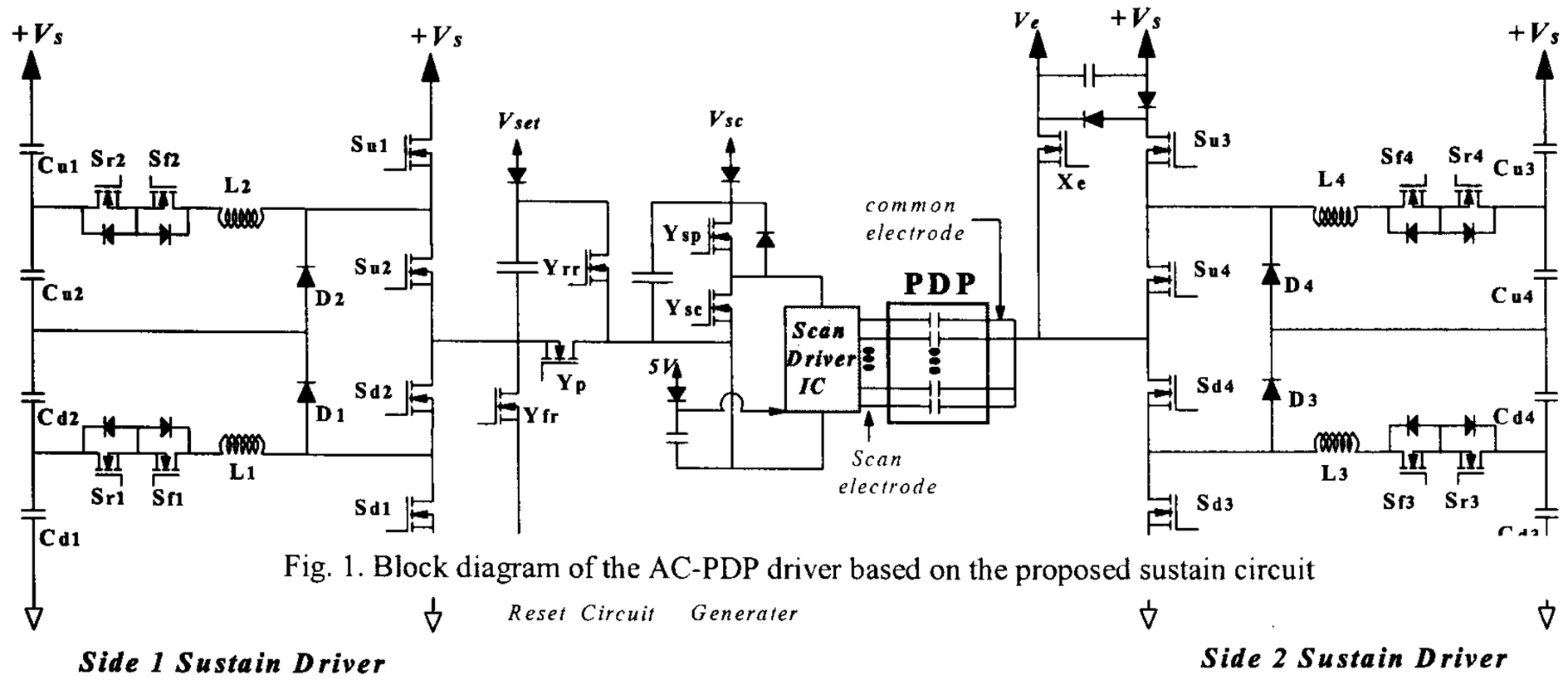

Fig. 1. Block diagram of the AC-PDP driver based on the proposed sustain circuit

$C_{d1} - S_{r1} - D_{f1} - L_1 - S_{d2} - C_p$ in a resonant manner. The current i_{L1} and the voltage v_p can be obtained as follows:

$$i_{L1}(t) = \frac{V_s}{4Z_r}\sin w_r(t-t_0)\,(1), \quad v_p(t) = \frac{V_s}{4}(1-\cos w_r(t-t_0))\,, \qquad (2)$$

where $w_r = 1/\sqrt{LC_p}$ and $Z_r = \sqrt{L/C_p}$. v_p and the voltage across S_{d1} increase from zero to $+V_s/2$, and the peak panel current $i_{p,pk}$ is clamped to $+V_S/(4Z_r)$. Mode 1 ends when i_{L1} becomes zero at $t = t_1$. Using the equation (1), the duration of mode 1, T_{r1} , can be easily obtained as follows: $T_{r1} = \pi / w_r = \pi\sqrt{LC_p}$.(3)

Mode 2 ($t_1 \le t < t_2$; *idling mode*): At $t = t_1$, the switch S_{d2} is turned *OFF*, and the switch S_{u2} is turned *ON*. The voltages across S_{u1} , S_{d1} , and S_{d2} are clamped to $+V_s/2$. In mode 2, v_p remains at $+V_s/2$ and there does not exist any gas discharge current flowing through the panel. While the duration of mode 2 can be arbitrarily determined, it is recommended to be as short as possible for the very high frequency operation in a real plasma display drive unit.

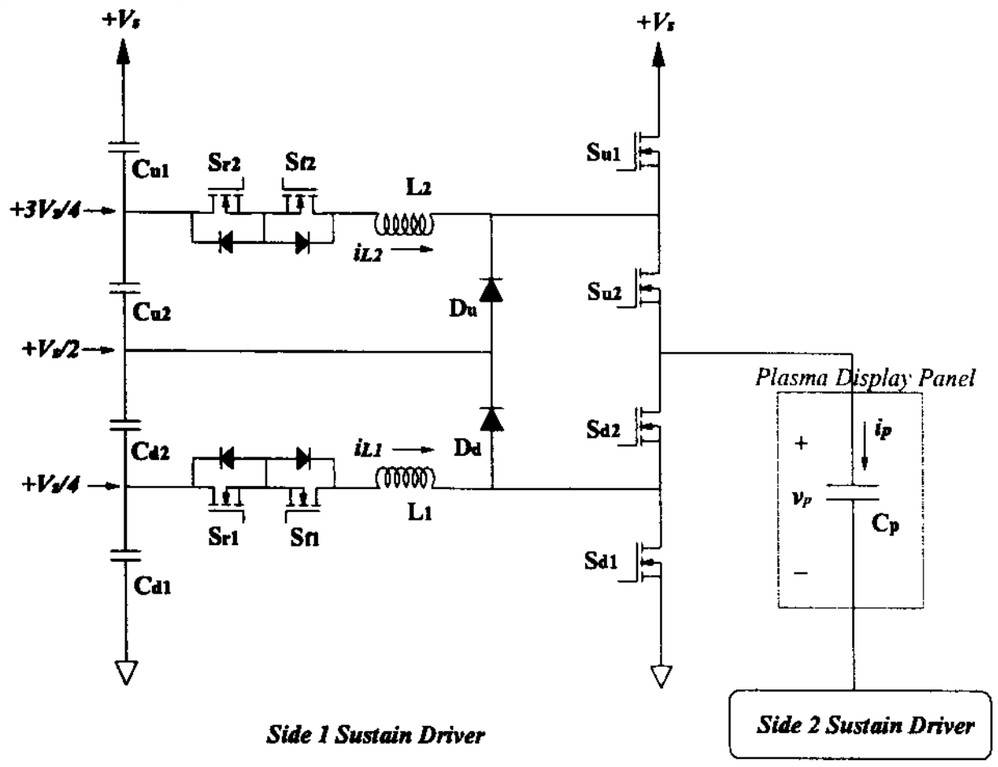

Fig.2 Electrical equivalent circuit during the whole gas discharging period

Mode 3 ($t_2 \le t < t_3$; *post-charging mode*): Mode 3 begins when S_{r2} is turned *ON* at $t = t_2$. The stored energy in the input capacitors C_{d1} , C_{d2} , and C_{u2} , is transferred to the panel capacitor via the path $C_{d1} - C_{d2} - C_{u2} - S_{r2} - D_{f2} - L_2 - S_{u2} - C_p$ in a resonant manner. In mode 3, the current i_{L2} and the voltage v_p are obtained as follows:

$$i_{L2}(t) = \frac{V_s}{4Z_r}\sin w_r(t-t_2)\,,(4) \qquad v_p(t) = \frac{V_s}{4}(3-\cos w_r(t-t_2))\,.(5)$$

The voltage v_p increases from $+V_s/2$ to $+V_s$, and the peak panel current $i_{p,pk}$ is clamped to $+V_S/(4Z_r)$. The voltage across S_{u1} decreases from $+V_s/2$ to zero during mode 3. Mode 3 ends when i_{L1} becomes zero at $t = t_3$. The duration of mode 3, T_{r2} , is the same as that of mode 1, e.g., $T_{r2} = T_{r1} = \pi\sqrt{LC_p}$.

Mode 4 ($t_3 \le t < t_4$; *gas discharging mode*): At $t = t_3$, S_{u1} is turned *ON* under the zero-voltage-switching condition and the switching turn-on loss of S_{u1} is zero. In mode 4, v_p remains at $+V_s$ and supports the gas discharge current in the plasma panel. Mode 4 ends when S_{u1} is turned *OFF*, and S_{f2} is turned *ON* at $t = t_4$. It is noted that the duration of mode 4, T_{sus} , can be arbitrarily chosen as long as it is longer than the time for the gas discharge current to be reduced to zero, typically in the range of 1.7*us* to 2.5*us* [see Ref [1-2]].

Mode 5 ($t_4 \le t < t_5$; *pre-discharging mode*) : During mode 5, half the stored energy in C_p is recovered by the input capacitors C_{d1} , C_{d2} , and C_{u2} , via the path $C_p - S_{u2} - L_2 - S_{f2} - D_{r2} - C_{u2} - C_{d2} - C_{d1}$ in a resonant manner. The current i_{L2} and the voltage v_p , are written as follows:

$$i_{L2}(t) = -\frac{V_s}{4Z_r}\sin w_r(t-t_4)\,,(6) \qquad v_p(t) = \frac{V_s}{4}(3+\cos w_r(t-t_4))\,.(7)$$

During mode 5, v_p decreases from $+V_s$ to $+V_s/2$, and the voltage across S_{u1} increases from zero to $+V_s/2$. The peak panel current $i_{p,pk}$ is clamped to $-V_S/(4Z_r)$. Mode 5 ends when i_{L2} becomes zero at $t = t_5$. Using the equation (6), the duration of mode 5, T_{f1} , can be easily obtained as follows: $T_{f1} = \pi / w_r = \pi\sqrt{LC_p}$. (8)

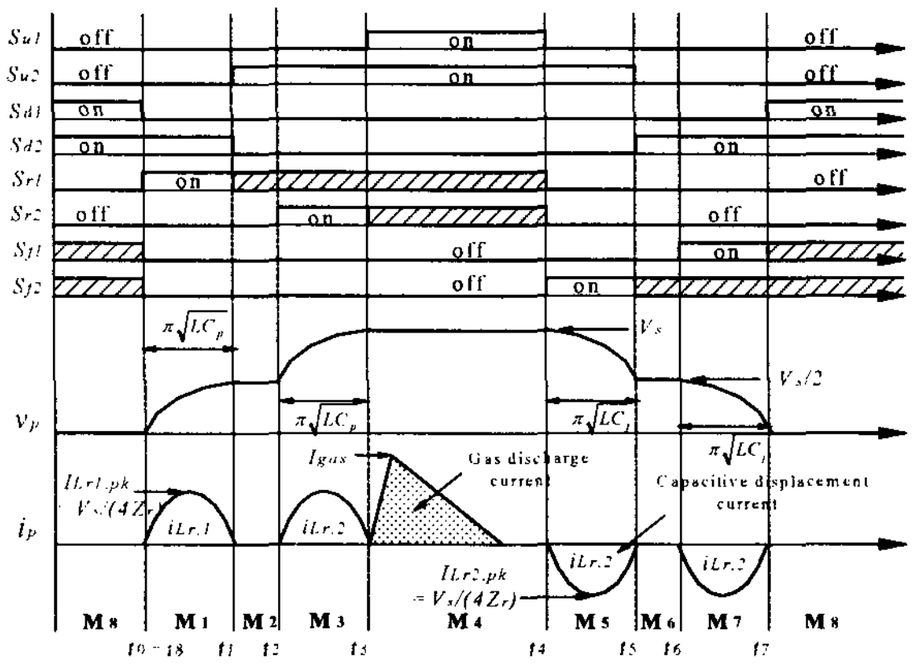

Fig.3. Key voltage and current waveforms

Mode 6 ($t_5 \le t < t_6$; *idling mode*): At $t = t_5$, S_{u2} is turned *OFF*, while S_{d2} is turned *ON*. The voltages across S_{u1} , S_{u2} and S_{d1} are clamped to $+V_s/2$. The voltage v_p remains at $+V_s/2$ during mode 6. As in the case of mode 2, the duration of mode 6 is recommended to be as short as possible.

Mode 7 ($t_6 \le t < t_7$; *post-discharging mode*): Mode 7 begins when S_{f1} is turned *ON*, while S_{u2} remains *ON* at $t = t_6$. The remaining energy in C_p is now fully recovered by the input capacitor C_{d1} via the path $C_p - S_{d2} - L_1 - S_{f1} - D_{r1} - C_{d1}$ in a resonant manner. The current i_{L1} and the voltage v_p , are obtained as follows:

$$i_{L1}(t) = -\frac{V_s}{4Z_r}\sin w_r(t-t_6) \ ,(9) \qquad v_p(t) = \frac{V_s}{4}(1+\cos w_r(t-t_6)) \ .(10)$$

v_p decreases from $+V_s/2$ to zero, and the peak panel current $i_{p,pk}$ is clamped to $-V_S/(4Z_r)$. The voltage across S_{d1} decreases from $+V_s/2$ to zero. Mode 7 ends when i_{L1} becomes zero at $t = t_7$, and the duration of mode 7, T_{f2} , is the same value as T_{f1} . It is noted that the required times of the charging or discharging are all the same in the proposed circuit, e.g., $T_{r1} = T_{r2} = T_{f1} = T_{f2}$.

Mode 8 ($t_7 \le t < t_8$; *ground mode*): At $t = t_7$, S_{d1} is turned *ON* under the zero-voltage-switching condition, and v_p remains at zero during mode 8. When S_{d3} is tuned *OFF*, while S_{r3} is turned *ON* at $t = t_8$, which are shown in side 2 sustain driver, the other half of the switching cycle continues. While the duration of mode 4, T_{gnd} , can be arbitrarily determined, it is recommended to be as short as possible for the very high frequency operation in a real plasma display unit.

III. COMPARATIVE ANALYSIS AND DESIGN

3.1. Device Stresses and power losses

The proposed circuit features the half the device voltage stresses and half the reactive power compared to those of the conventional circuit. Table I. summarizes the comparison of the proposed circuit and the conventional circuit, which can be deduced from the key waveforms of Fig.3. Here, I_{gas} is defined as the peak gas-discharge current in the PDP, typically in the order of one hundred ampere range. N_{vp} is the number of pulse voltage v_p per a TV frame, and T_{frame} is the period of a TV frame. f is defined as $f = N_{vp}/T_{frame}$. As can be seen in this table, though the peak values of the device current are the same as those in the conventional circuit, all the peak values of the device voltage and the *rms* value of the device current are significantly reduced in the order of about half time.

Table I. Device stresses comparison

Device stresses		Proposed.	Conventional.
Sustain MOSFET Switches	V_{ds,pk_sus}	$\frac{V_s}{2}$	V_s
	I_{ds,pk_sus}	I_{gas}	I_{gas}
	I_{ds,rms_sus}	$\frac{V_s}{4Z_r}\sqrt{\frac{T_r f}{2}}$	•
Energy Recovery MOSFET Switches	V_{ds,pk_ER}	$\frac{V_s}{4}$	$\frac{V_s}{2}$
	I_{ds,pk_ER}	$\frac{V_s}{4Z_r}$	$\frac{V_s}{2Z_r^*}$
	I_{ds,rms_ER}	$\frac{V_s}{8Z_r}\sqrt{T_r f}$	$\frac{V_s}{2Z_r^*}\sqrt{T_r f}$
Energy Recovery Diode	V_{D,pk_ER}	$\frac{V_s}{4}$	$\frac{V_s}{2}$
	I_{D,pk_ER}	$\frac{V_s}{4Z_r}$	$\frac{V_s}{2Z_r^*}$
	I_{D,rms_ER}	$\frac{V_s}{8Z_r}\sqrt{T_r f}$	$\frac{V_s}{2Z_r^*}\sqrt{T_r f}$
	I_{D,ave_ER}	$\frac{CV_s f}{2}$	$CV_s f$
inductors	$I_{L,rms}$	$\frac{V_s}{4Z_r}\sqrt{\frac{T_r f}{2}}$	$\frac{V_s}{Z_r^*}\sqrt{T_r f}$
capacitors	$V_{C,pk}$	$\frac{V_s}{4}$	$\frac{V_s}{2}$
	$I_{C,rms}$	$\frac{V_s}{4Z_r}\sqrt{\frac{T_r f}{2}}$	$\frac{V_s}{Z_r^*}\sqrt{T_r f}$
Clamp diode	$V_{D,pk}$	$\frac{V_s}{2}$	•

All the power losses except the sustain switch loss, are significantly reduced in the order below quarter time, since a devices with low parasitic resistance can be selected in the proposed circuit. Although there exist the conduction losses of the sustain switches due to the *rms* displacement current, it is noted that, however, the conduction losses due to the gas discharge current are so high enough to neglect the effect of that due to this displacement current. Consequently, it is expected that the proposed circuit gives an significantly improved efficiency in designing high density sustain circuit for the PDP drive.

3.2. Design Example

The sample designs are carried out based on both circuits to drive a 42-inch PDP. The practical power losses are also calculated to compare both circuits. The main specifications are listed as follows:

V_s	$180V_{dc}$	T_r	$300ns$

T_{sus}	2.4*us*	C_p	66*nF*
I_{gas}	100*A*	$I_{gas.rms}$	8.16*A*
N_{vp}	1,024	T_{frame}	16.67*ms*

By using the equation (13) and the equation (14), the required values of each inductor are obtained as $L = 35nH$, and $L^* = 140nH$, respectively. The characteristic impedances are also obtained as $Z_r = 0.73$, and $Z_r^* = 1.46$. The sustain switches should support the peak gas discharge current $I_{gas}(=100A)$. While the *MOSFETs* with *250V* voltage rating should be selected in the conventional circuit, those with *150V* voltage rating are sufficient in the proposed circuit. From Table I, the required peak current flowing through each energy recovery *MOSFET* switch is obtained as $I_{S\_ER,pk} = 61.6A$ for both the circuit. The required voltage and current ratings of the energy recovery diodes are the same as those of the energy recovery switches. It is noted that the current flowing through a clamp diode is zero in the theoretical condition. Their role is to help balancing the voltages across the series connected devices such as the sustain switches and the input capacitors. A *220uF* electrolytic capacitor with *100V* voltage rating and four parallel *2.2uF* ceramic type capacitors with *150V* voltage rating are chosen for the proposed circuit and the conventional circuit, respectively.

Based on the above considerations, the calculated power losses in designing a circuit to drive 42-inche PDP are shown in Fig. 4. As can be seen in this figure, all the power losses are significantly reduced, and the total power losses are estimated as *8.61W* for the proposed circuit and *19.58W* for the conventional circuit, respectively. The reasons are as follows: (1) All the device *rms* currents are reduced in the order about half time, and (2) All the parasitic resistances are significantly reduced in the order about quarter time. In general, the semiconductor devices suffered from a low voltage rating feature not only the more reduced parasitic effects such as the parasitic resistance and the parasitic capacitance, but also the lower cost, compared to those suffered from a high voltage rating. Table III. shows the estimated costs in designing a 42-inche PDP drive circuit. As can be seen, the total costs of the semiconductor devices in the proposed circuit are comparable to those in the conventional ones.

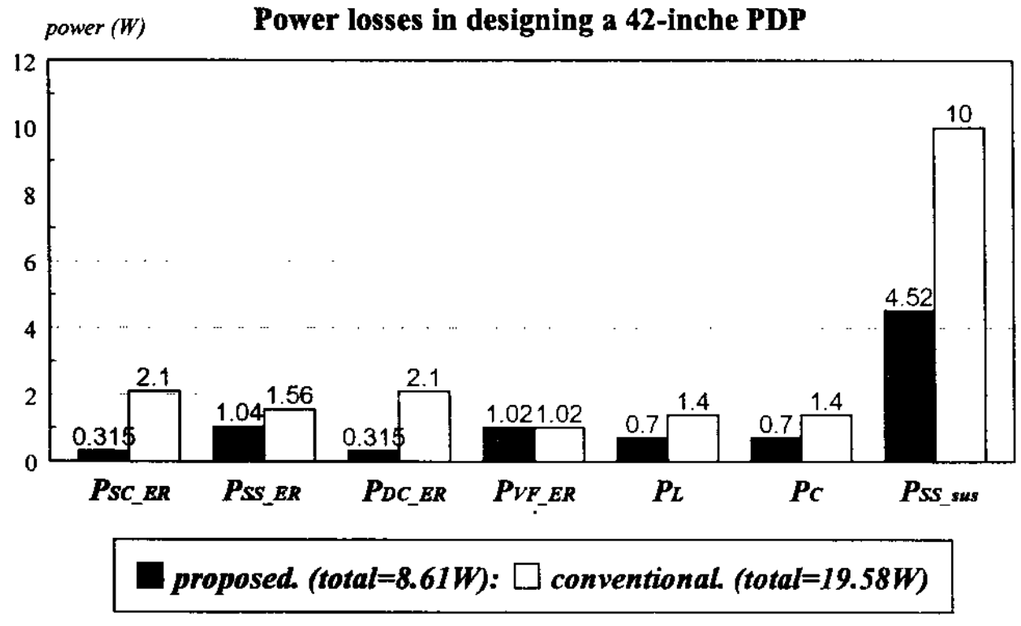

Fig.4. Calculated power losses in designing a circuit to drive 42-inche PDP

IV. EXPERIMENTAL RESULTS AND CONCLUSION

To experimentally characterize the proposed driving technology, a prototype of Fig.1 has been constructed to drive a 42-inch PDP. The gate signal generator is based on the logic chip EPM7032LC44-15 from ALTERA. Fig. 5 shows the experimental results of the voltage and current waveforms under the peak panel capacitance condition. The peak inductor current is measured as 2.2*A*, The voltage and current waveforms for the sustain witches are shown in Fig. 6. All the figures show that the waveforms agree well with the theoretical analysis. In a conclusion, a new sustain circuit for an AC PDP drive is presented. The proposed circuit, which can be implemented with a set of half the voltage-rating devices, guarantees high-efficiency and reduced power losses compared to the conventional circuit. The proposed circuit is best suited for designing a low cost, high power density, AC PDP driver.

V. REFERENCES

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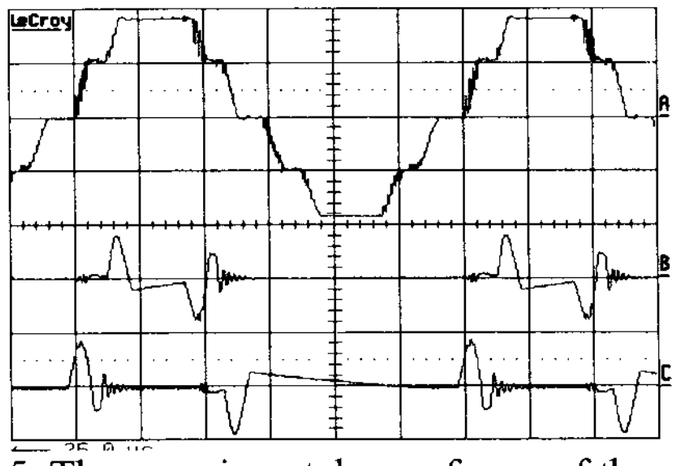

Fig. 5. The experimental waveforms of the panel (top trace:Vp@100V/div; middle trace:iL2@2A/div; bottom trace:iL1@2A/div; time:5us)

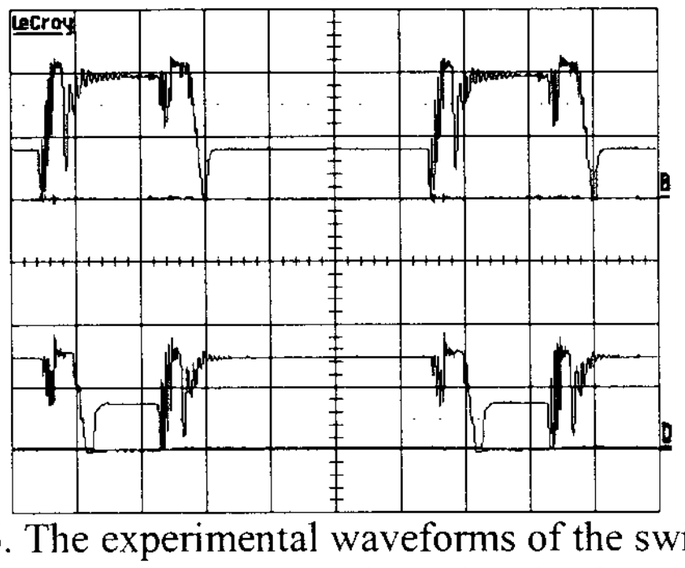

Fig. 6. The experimental waveforms of the switches (top trace:Vgs(Sd1)@20V/div;Vds(Sd1)@100V/div; bottom trace:Vgs(Su1)@20V/div;Vds(Su1)@100V/div)