

Study on Characteristics of Organic Thin Film Transistors with Rubbed Organic Gate Insulators

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Abstract

In this work, the electrical characteristics of organic thin film transistors with the surface-treated organic gate insulators have been studied. For the surface treatment, the simple rubbing technique was used. The field effect mobilities of the devices with PVP gate insulator was improved about four times as high as those of TFTs without the insulator surface treatment.

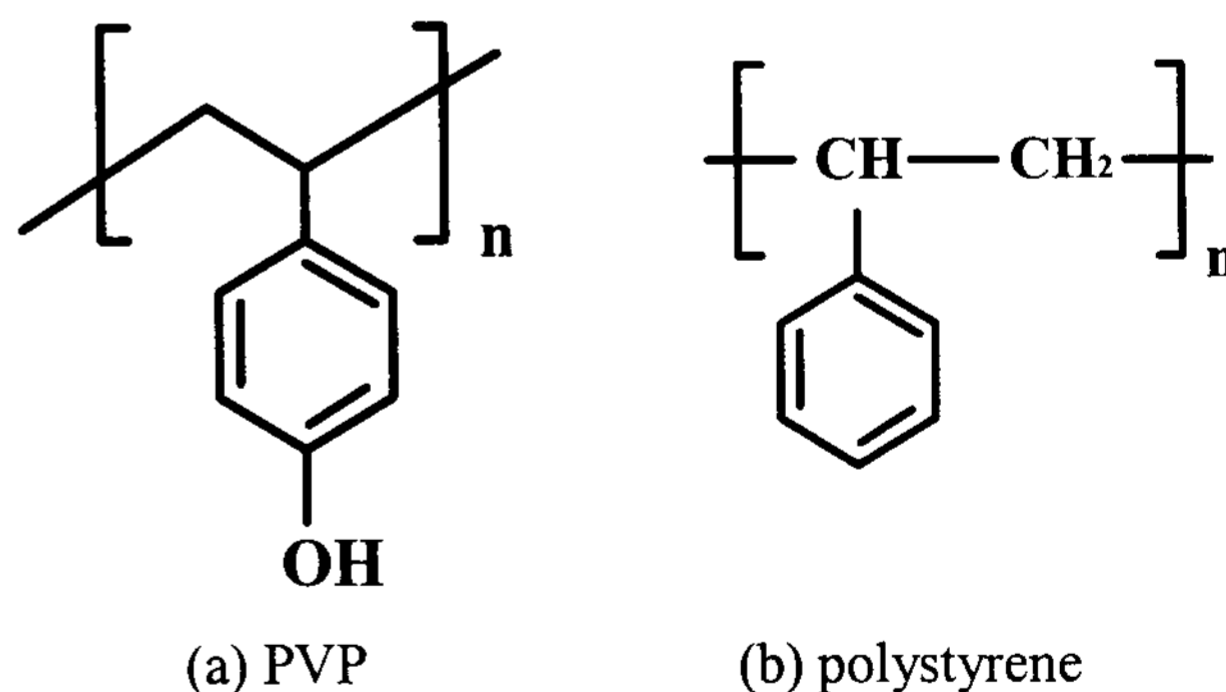
1. Introduction

Some organic materials have received considerable attention as semiconductors for the device applications such as thin film transistors (TFT) and light emitting diodes [1-6]. They can offer substantial advantages in terms of the processing simplicity and competitive cost. Recently, much attention to all-organic devices has been drawn [7, 8]. In this work, the electrical characteristics of two kinds of organic TFTs with the surface treated organic gate insulators have been investigated. Pentacene was used as a semiconductor layer, and PVP (Polyvinylphenol) and polystyrene as a gate insulator. For the surface treatment, the simple rubbing technique was used. The rubbing technique is a simple method to form the induced orientation layer for liquid crystal displays. The electrical characteristics of thin film transistors with and without surface-treated insulators are discussed.

2. Experimental Details

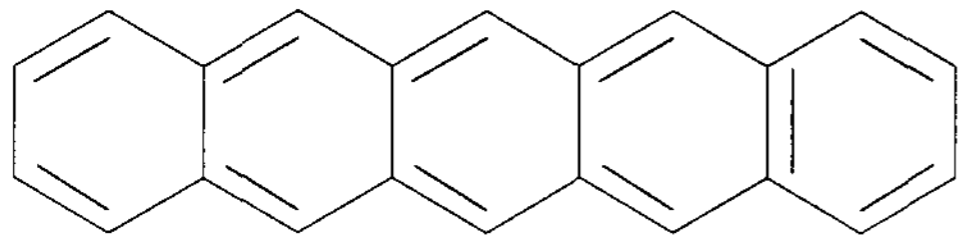
Pentacene was thermally evaporated in vacuum at a pressure of about 10^{-6} Torr and at a deposition rate of

0.5 Å/sec. Aluminum and gold were used for the gate and source/drain electrodes, respectively [9, 10]. The gate, source and drain electrodes were evaporated through shadow masks. During the evaporations, the substrates were held at room temperature. As gate insulators, PVP and Polystyrene films were coated by spinning. For spin-coating, MEK (Methyl Ethyl Ketone) and toluene were used as solvents, respectively. The thicknesses of the pentacene, PVP and polystyrene layers are 60nm, 300nm and 250nm, respectively, which were confirmed by ellipsometry (Plasmos, SD-2100) and α -step profiler (Tenkor, 200). The channel length and width of the TFT were 50 μ m and 5mm, respectively. Insulator surfaces were rubbed before the depositions of pentacene layers onto the insulators [11]. Figure 1 shows the molecular structures of the PVP, polystyrene and pentacene, and the structures of the devices are shown in figure 2. The electrical characteristics were measured by Keithley 238 and 617 source-measurement unit and under the shielded condition.



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(c) pentacene

Figure 1. Molecular structures of (a) PVP and (b) polystyrene and (c) pentacene.

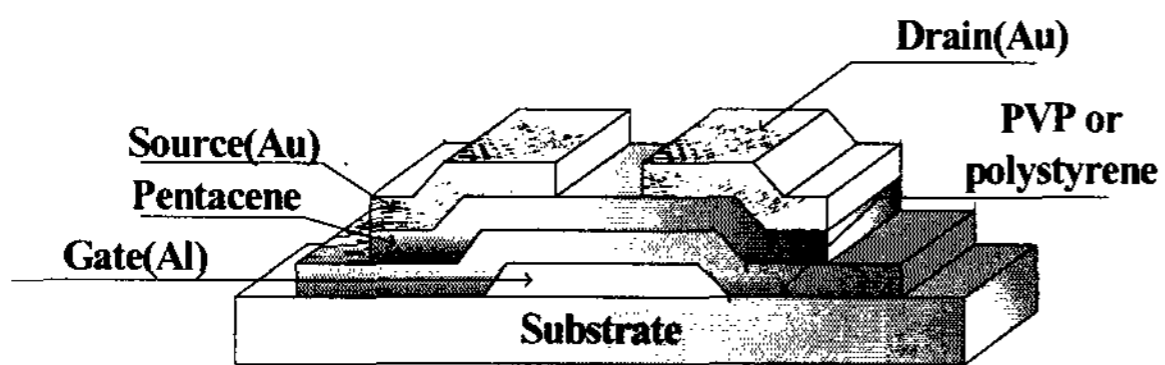


Figure 2. Structure of the devices

3. Results and Discussions

The insulating properties of the PVP and polystyrene thin layers are shown in figure 3. The 300nm thick PVP and polystyrene films sustained the bias stress up to 80 V across them without a dielectric breakdown. In addition, polystyrene shows better insulating property than that of PVP. This result describes earlier saturation of polystyrene-based TFT at the output characteristics.

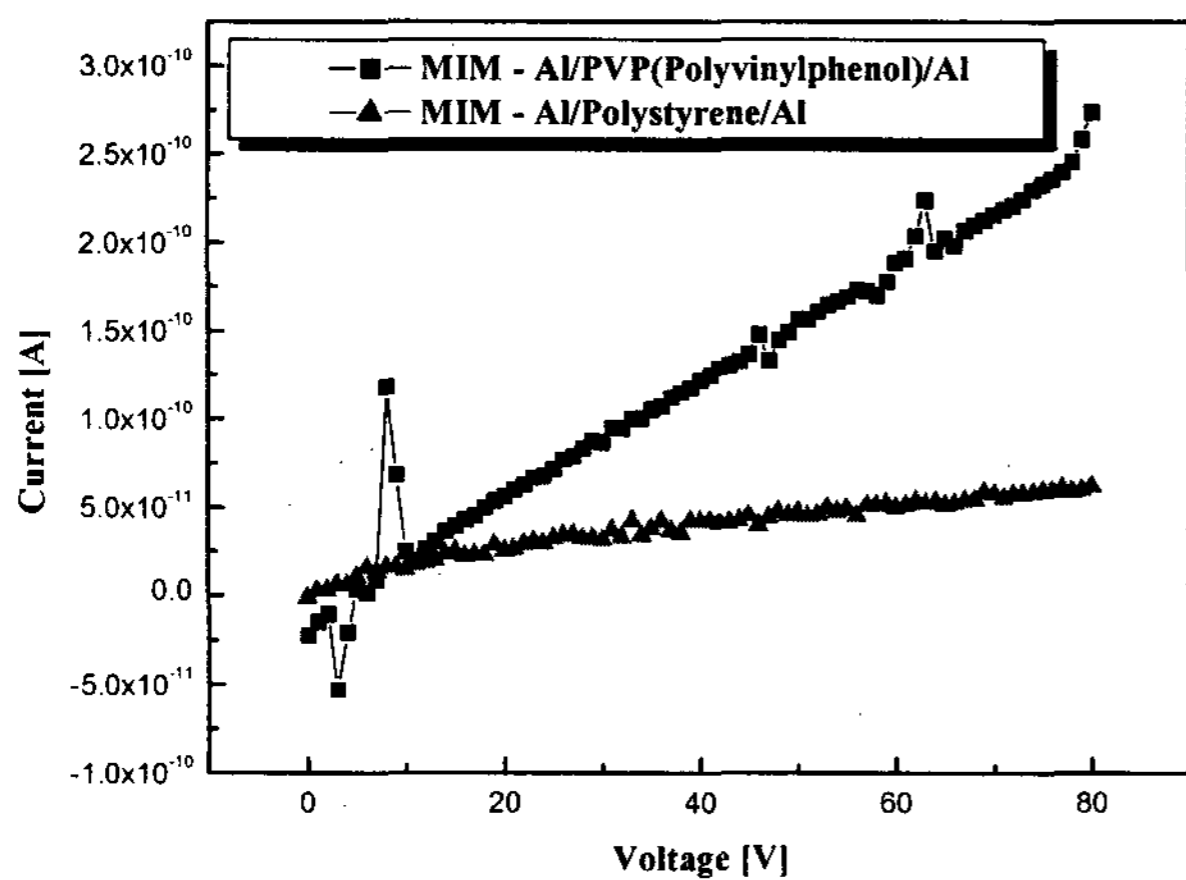
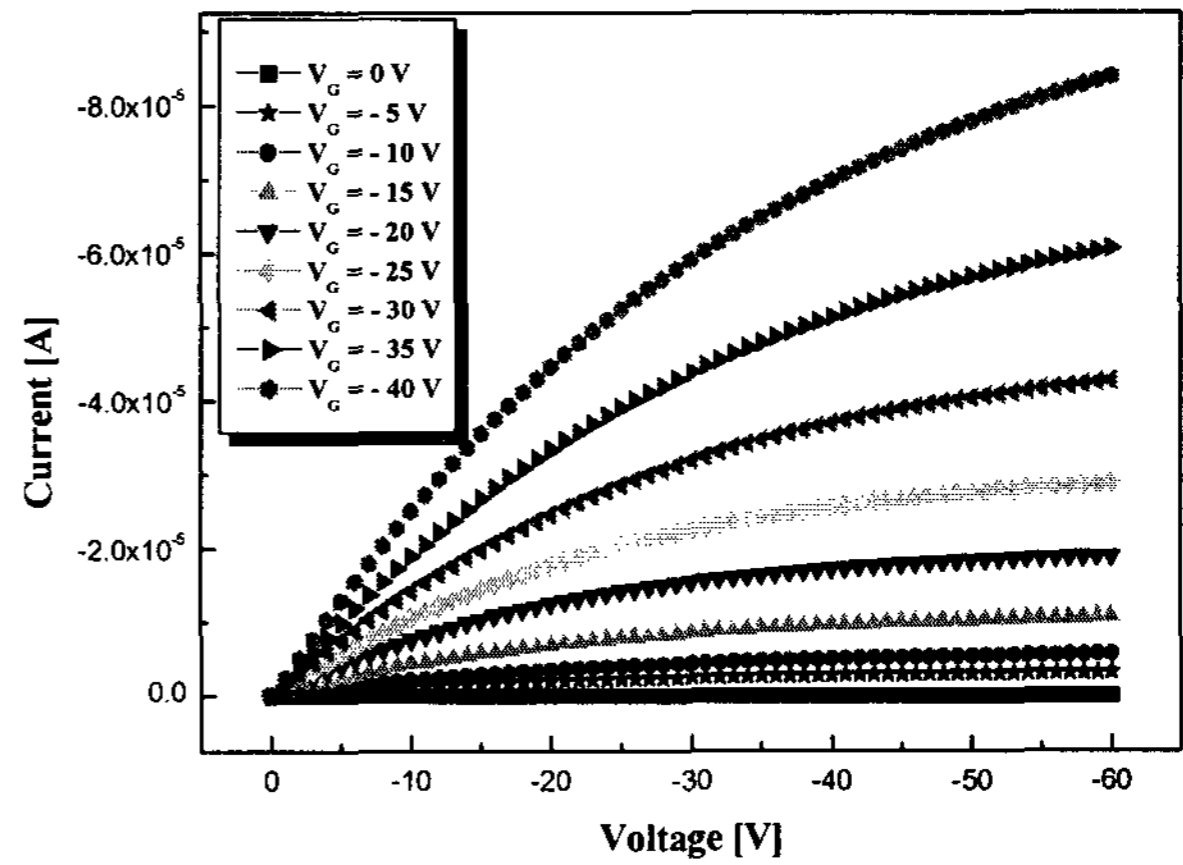
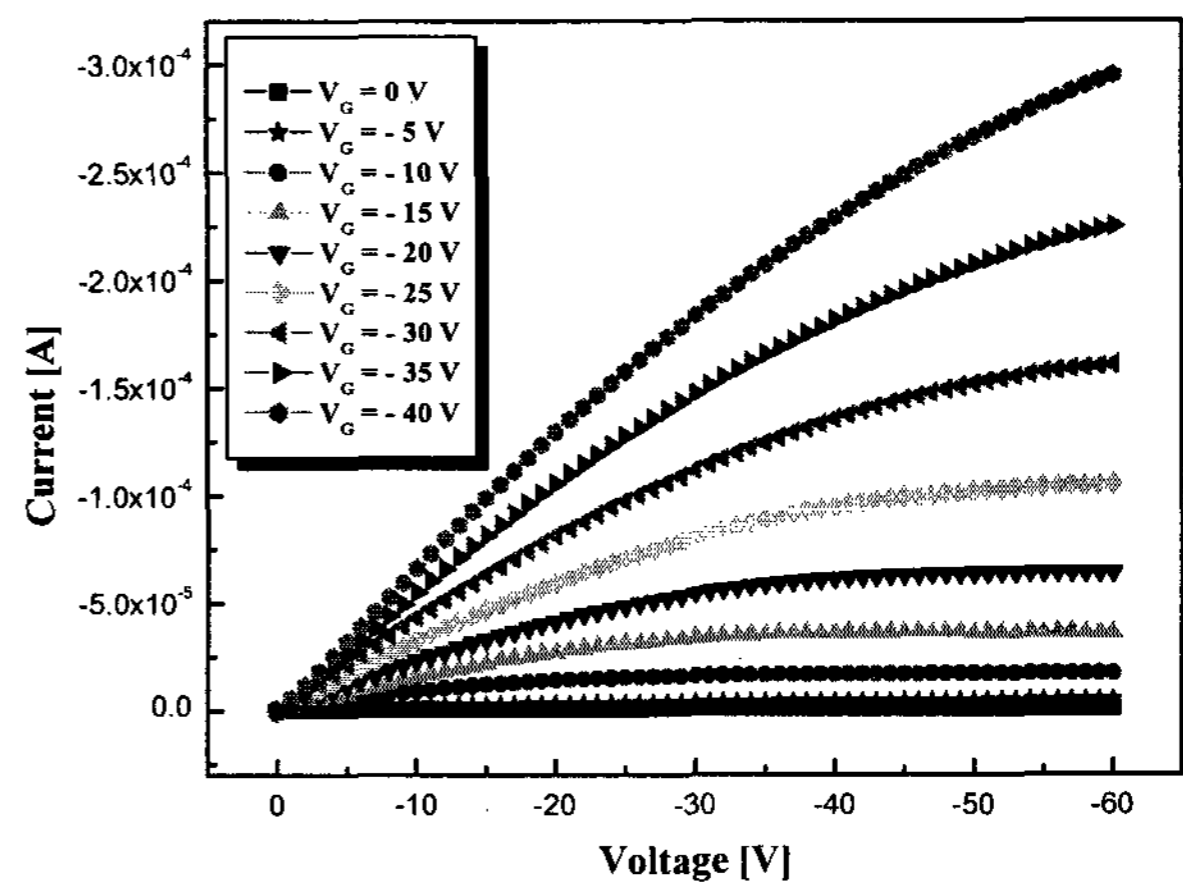


Figure 3. Insulating properties of PVP and polystyrene.

The output characteristics of the pentacene TFTs with PVP gate insulator are shown in figure 4. The output characteristic of the unrubbed PVP-based TFT is shown in figure 4(a), and with rubbed gate insulators shown in figure 4(b). The TFT with the surface-treated PVP provides the improved output characteristics. It is considered that the molecular orientation of pentacene molecules, induced by the rubbing treatment, leads to the improved interface properties between pentacene and PVP layer



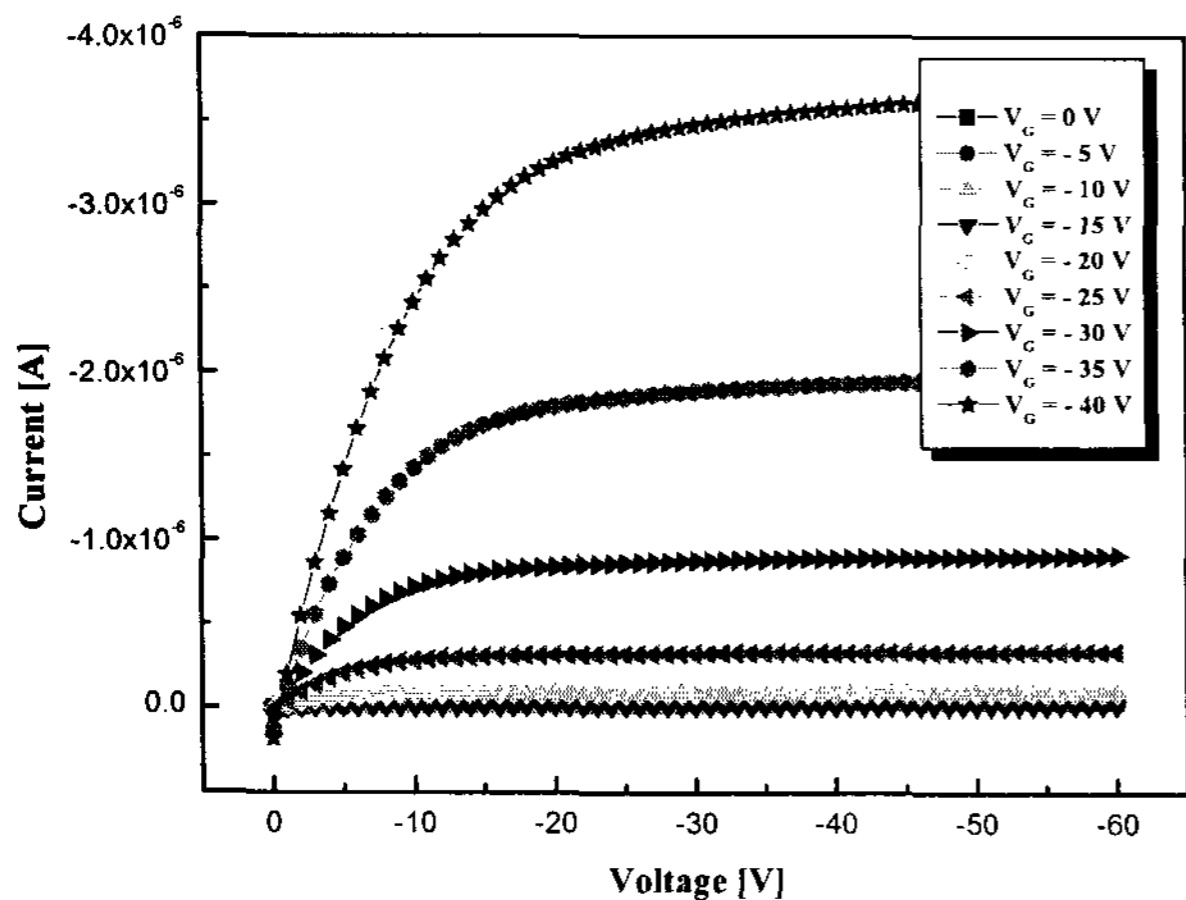
(a)



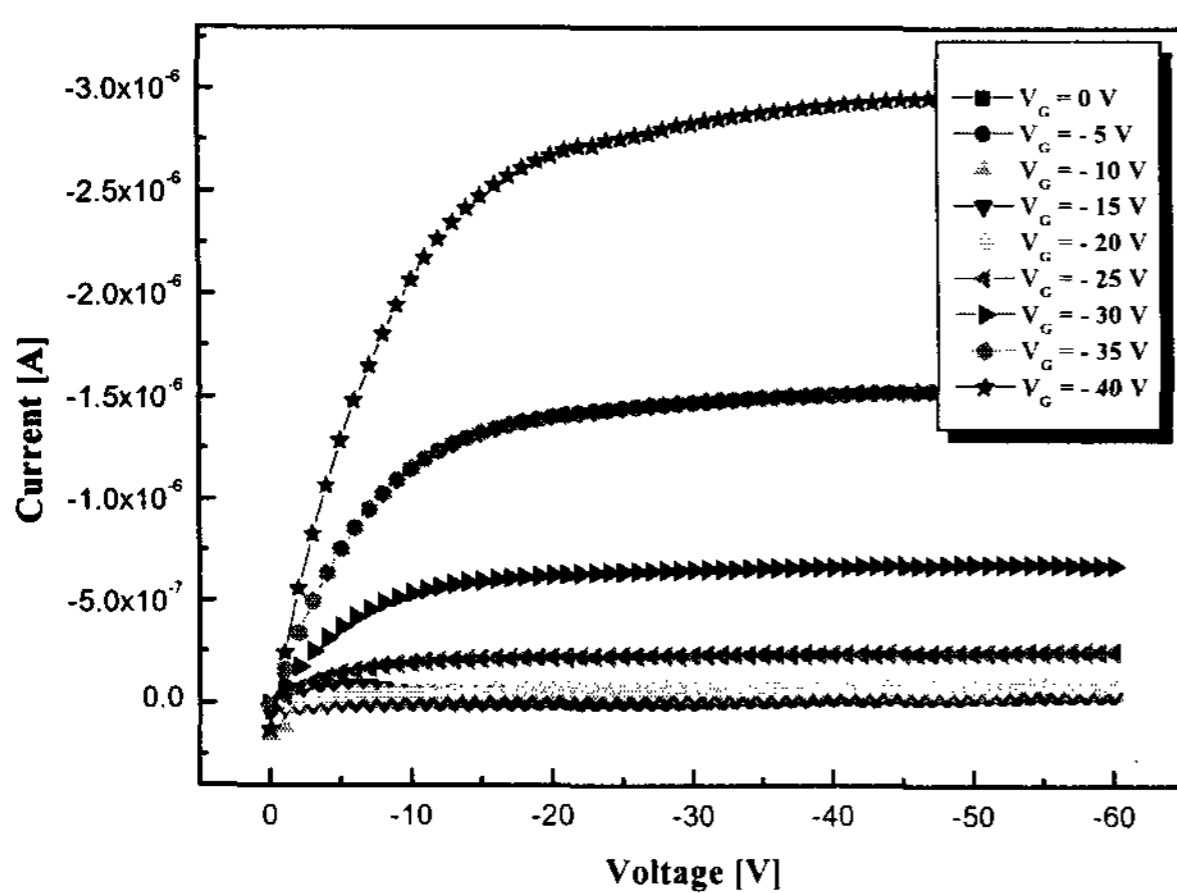
(b)

Figure 4. Output characteristics of pentacene TFT; (a) on as-deposited PVP, (b) on rubbed PVP.

But for polystyrene-based TFTs, the characteristics were not improved as much as the PVP-based TFT. This result indicates that polystyrene layer is less affected by the rubbing treatment, due to its hardness. The output characteristics of the pentacene TFTs with polystyrene gate insulator are shown in figure 5. The output characteristic of the untreated polystyrene-based TFT is shown in figure 4(a), and treated gate insulators shown in figure 4(b).



(a)



(b)

Figure 5. Output characteristics of pentacene TFTs; (a) on the as-deposited polystyrene, (b) on the rubbed polystyrene.

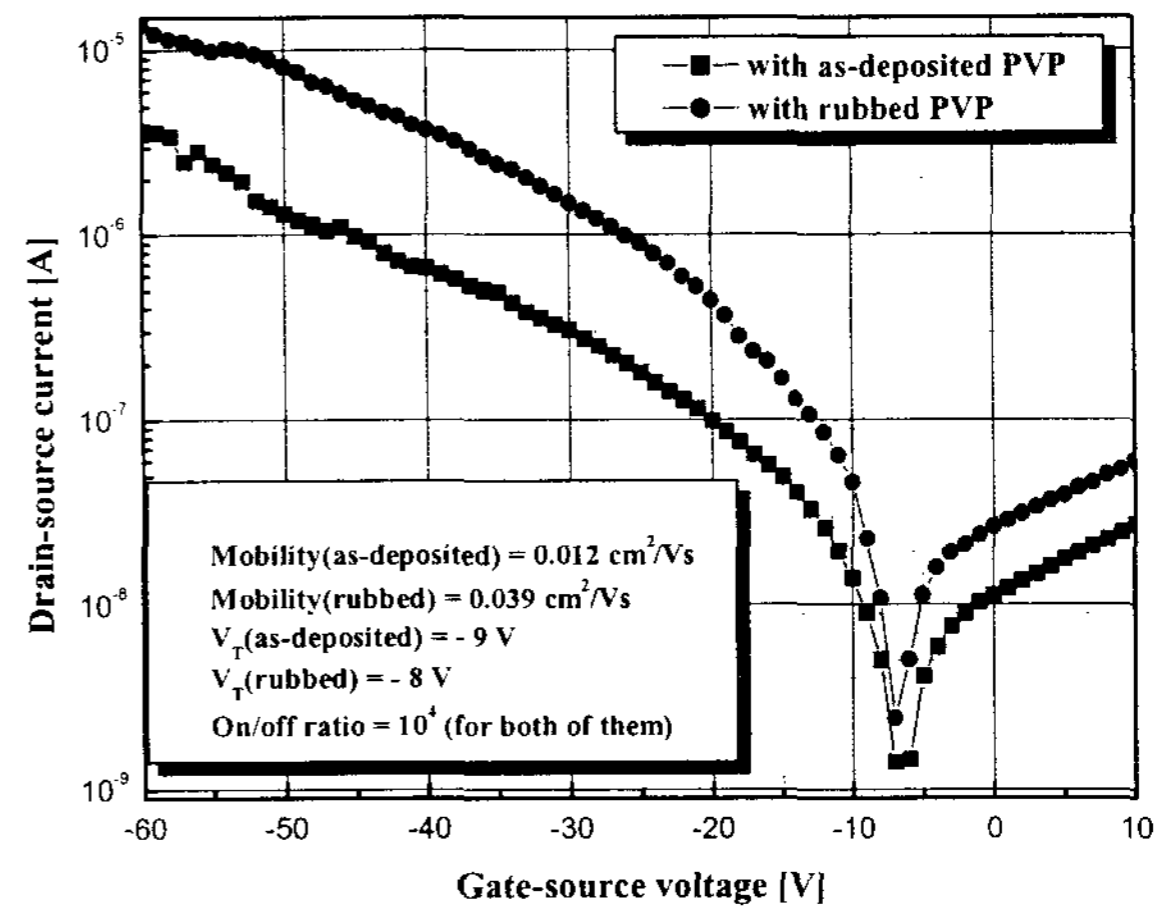


Figure 6. Transfer characteristics of pentacene TFT with rubbed and as-deposited gate insulators.

Figure 6 shows the transfer characteristics of the organic TFTs with as-deposited and rubbed PVP. The higher on/off ratio of the TFT with treated PVP was obtained as about 10^5 , while without surface treatment of PVP was 10^4 . The threshold voltage of the TFT with rubbed dielectric layer is about -8 V, which is lower than that of the TFT with unrubbed dielectric layer (-9V). The extracted mobilities are $0.012 \text{ cm}^2/\text{Vs}$ for the TFT with as-deposited insulator and $0.039 \text{ cm}^2/\text{Vs}$ for the TFT with rubbed PVP, respectively. All the parameter values were extracted from the drain current equation in the saturation region as follows [12];

$$I_D = \frac{W}{2L} C_i \mu (V_G - V_T)^2$$

where W is the channel width, L is the channel length, C_i is the capacitance of the insulator per unit area, μ is the field effect mobility, V_T is the threshold voltage, and V_G is the gate voltage. These improved operational device parameters might indicate that the rubbed insulator can provide better insulator/pentacene interface properties due to the improved molecular orientation and adhesion of pentacene molecules to the gate insulator surface.

4. Conclusions

The pentacene TFTs with different organic insulators were fabricated. Upon the investigation, it is observed that the rubbed organic gate insulator surface can

improve the characteristics of pentacene TFTs. As a result, we suggest that the rubbing treatment results in the improved interface characteristics at pentacene/insulator and the enhanced electrical characteristics of the pentacene TFT. If the fabrication can be optimally processed under lower vacuum pressure and the substrate temperature for organic layer depositions is raised higher, the purer and better-ordered organic layer can be obtained. It will provide the more improved characteristics that can be comparable to those of conventional amorphous silicon TFT.

5. Acknowledgements

This work was supported by the Korea Research Foundation Grant (KRF-99-E00169).

6. References

- [1] Horowitz, G., Hajlaoui, R., Bourguiga, R., and Hajlaoui, M., *Synthetic Metals*, 101, p. 401 (1999).
- [2] Kalinowski, J., *J. Phys. D; Appl. Phys.*, 32, p. R179, (1999).
- [3] Horowitz, G., Hajiaoui, R., Fichou, D., and Kassmi, A. E., *J. Appl. Phys.*, 85(6), p. 3202, (1999).
- [4] Jackson, T., Lin, Y.Y., Gundlach, D., and Klauk, H., *IEEE J. Selected Topics in Quantum Electronics*, 4(1), p. 100, (1998).
- [5] Tecklenburg, R., Paasch, G., and Scheinert, S., *Adv. Mater. Opt. Electron.*, 8 p.285, (1998).
- [6] Jones, G.W., *SID 01 DIGEST*, p. 384, (2001).
- [7] M. Matters, D.M.de Leeuw, M.J.C.M. Vissenberg, *Optical Materials* 12, p.189, (1999)
- [8] T. Kawase, H. Sirringhaus, R.H. Friend, T. Shimoda, *SID 01 DIGEST*, p.40, (2001)
- [9] Choi, J.S., Kim, D.Y., Lee, J.H., Kang, D.Y., Kim, Y.K., and Shin, D.M., *Mol. Cryst. And Liq. Cryst.*, 349, p. 339, (2000).
- [10] Lee, J.H., Kim, D.Y., Choi, J.S., Kim, J.S., Kang, D.Y., and Shin, D.M., *JKPS*, 38(3), p. 282, (2001)
- [11] Lee, Y.S., Lee, J.H., Park, J.H., Lee, J.H. and Choi, J.S., *IMID '01 DIGEST*, p. 769, (2001)
- [12] Sze, S.M., *Physics of Semiconductor Devices*, John Wiley and Sons, p. 442, (1981).