Measurement of wall charge characteristics for three-electrode AC PDP

Sang-Jin Yoon
Digital PDP Division, LG Electronics Inc., Gumi-city, Gyung Buk, Korea
Hee-Chan Yang, Seong-Ho Kang, Jae-Hwa Ryu, and Bongkoo Kang[1]
[1] Division of Electrical and Computer Engineering, Pohang University of Science and Technology, Pohang, Gyung Buk, Korea

Abstract
This paper proposes a real-time wall charge measurement circuit for three-electrode AC PDP. It includes a charge-compensation network, current-integrating capacitors, initializing switches, and an op-amp. With this equipment, we measure the wall charge variations for the effects of sustain voltage, sustain pulse width, sustain frequency, and neighboring cells.

1. Introduction

AC Plasma Display Panel (PDP) [1] is a flat panel display, which can create a large, thin, and high-resolution display screen. The AC PDP emits visible light by exciting fluorescent layers with the vacuum ultraviolet (VUV) light created by a gas discharge. At present, the most widely used AC PDP is the three-electrode surface-discharge type [2]. In this type, two row electrodes S and C, which are formed on the front glass plate, are covered with a dielectric/MgO layer. One column electrode D is formed between the rear glass plate and a dielectric/phosphor layer.

In the AC PDP, a discharge is induced when the externally applied voltage between two electrodes exceeds the gas firing voltage. Ions and electrons are created by the discharge and move toward the inner walls due to the external electric field. The electric charges accumulated on the inner walls (wall charges) [1] cancel the external electric field, and the discharge is quenched. The wall charges give the AC PDP the memory function, by which the previous cell state is kept. For driving the AC PDP, the characteristics of wall charges should be understood.

Up to now, the wall charge measurement and analysis have been made mostly for understanding of two-electrode AC PDP [3,4]. In this paper, we propose a real-time wall charge measurement circuit for three-electrode AC PDP and measure wall charge transfer characteristics.

2. Wall Charge Measurement Circuit

A real-time wall charge measurement circuit for three-electrode AC PDP, as shown in figure 1, consists of the following: a charge-compensation network, current-integrating capacitors, initializing switches, and an op-amp. The wall charge measurement circuit measures wall voltage variation induced by drive pulses applied to the C electrode. The charge-compensation network consists of two variable capacitors C_{SC}` and $C_{CD}$`, which are set to be equal to the S-C capacitance C_{SC} and the C-D capacitance C_{cd} of the AC PDP cell, respectively. The current-integrating capacitors C_{SP} and C_{SP}` are in series with the AC PDP cell and the charge-compensation network, respectively. $C_{SP}$ integrates both the discharge current and the displacement current, but $C_{SP}$` integrates only the displacement current. The initializing switches SW1 and SW2

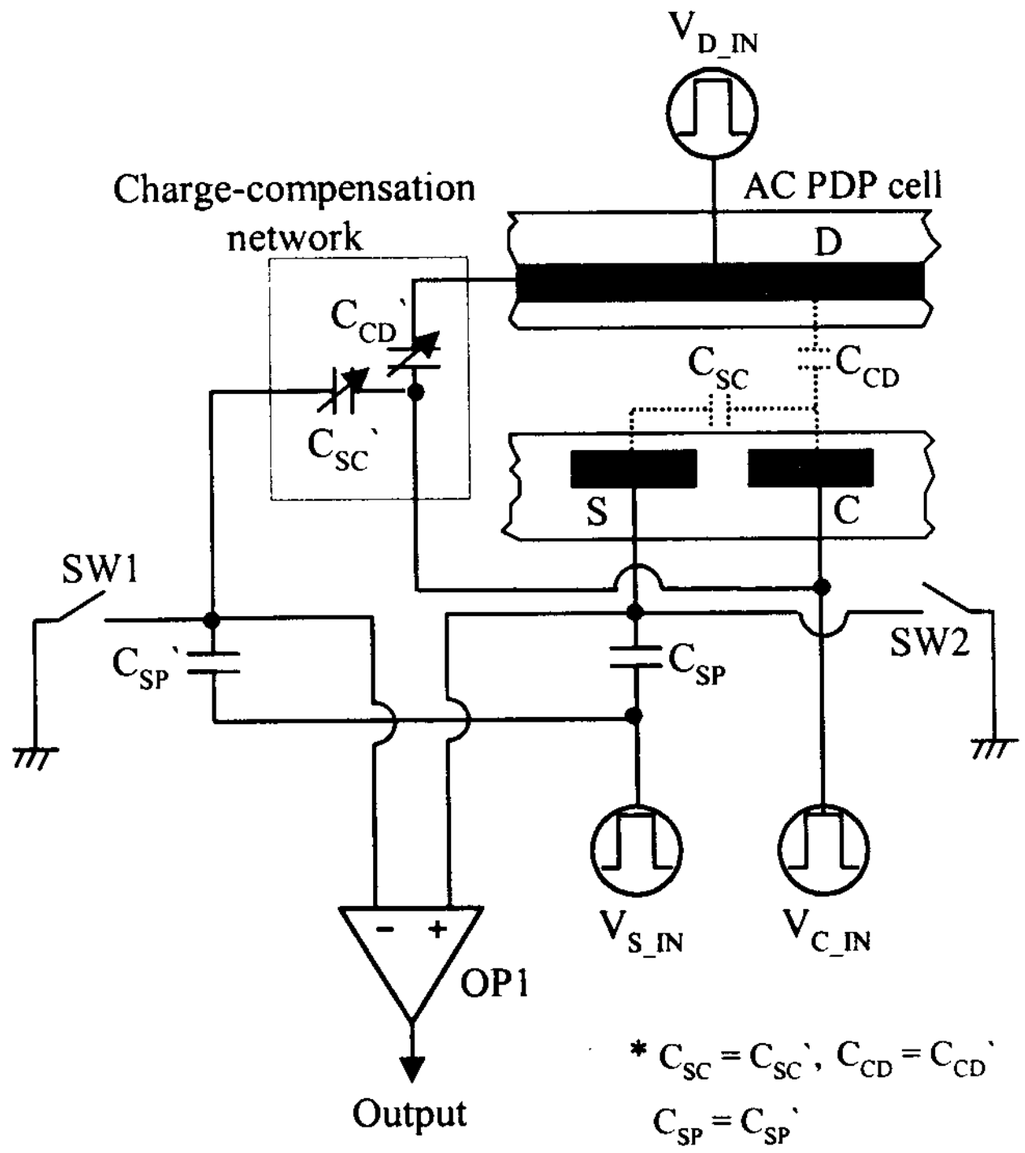

Figure 1. The wall charge measurement circuit

initializes C_{SP} and C_{SP}`, respectively, before measuring. The op-amp OP1 subtracts the displacement component from the measured signal, and output the discharge component that is proportional to the wall voltage.

Experimental drive waveforms for measuring wall voltage variations are shown in figure 2. After the total-write pulse of voltage V_{tw}, which has a step at voltage V_s, is applied to the C electrode, the sustain pulses of voltage V_s are applied alternately to the S and C electrodes. Finally, the erase pulse of voltage V_e is applied to the C electrode. The initializing switches SW1 and SW2 are turned-on during 1μs before applying pulses to the C electrode.

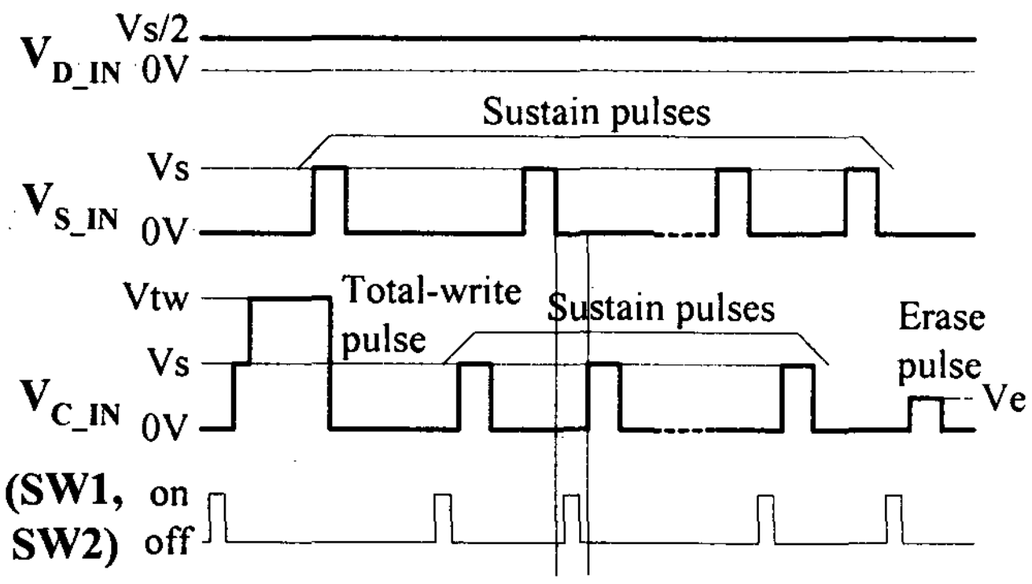

Figure 2. Drive waveforms for measuring wall voltage variations.

The measured waveforms are shown in figures 3 and 4. The trace 1 is the op-amp output voltage, which represents the wall voltage, and the trace 2 is the drive waveform applied to the C electrode. On the trace 1, the signal of positive polarity, which is induced by the C drive waveform, is used for analyzing wall voltage characteristics. In figure 3, the gas discharge initiated by the total-write pulse is not sustained by sustain pulses of voltage 140V. The wall voltage induced by the sustain pulses decreases to nearly 0V. However, in figure 4, the sustain pulses of voltage 145V maintain the discharge stably. The sustain discharge reaches the equilibrium condition at the fourth sustain pulse. For analyzing the wall voltage characteristics, the wall voltage induced by the sustain discharge under the equilibrium condition is used.

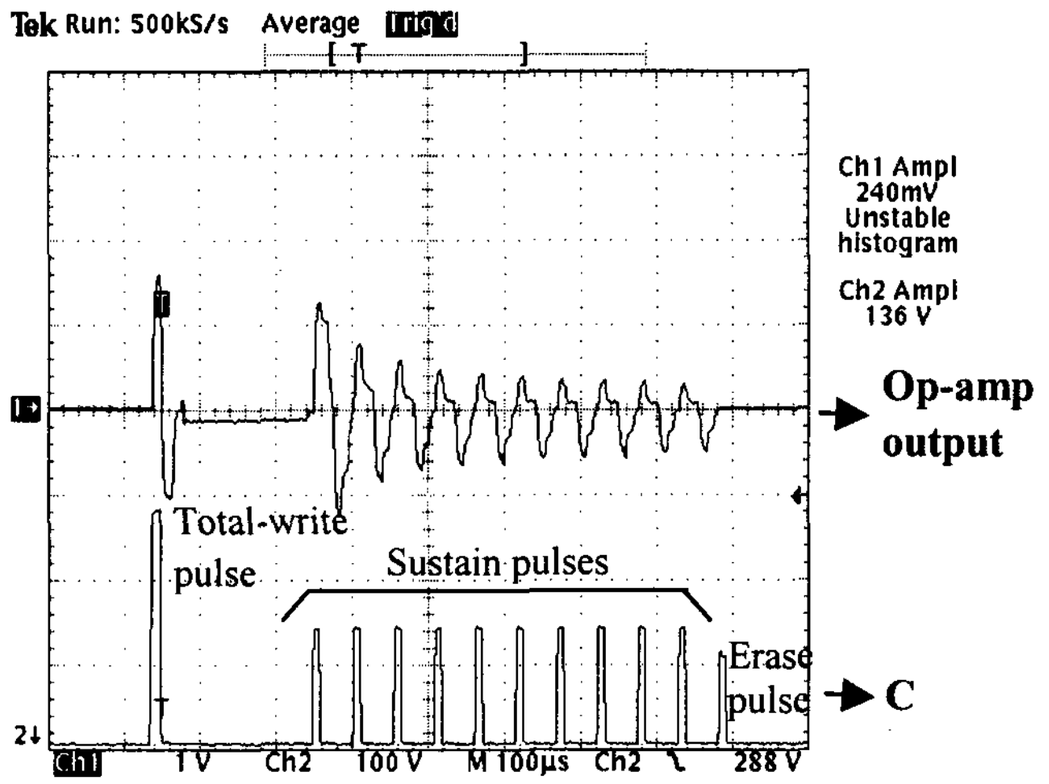

Figure 3. The measured waveforms for V_s = 140V

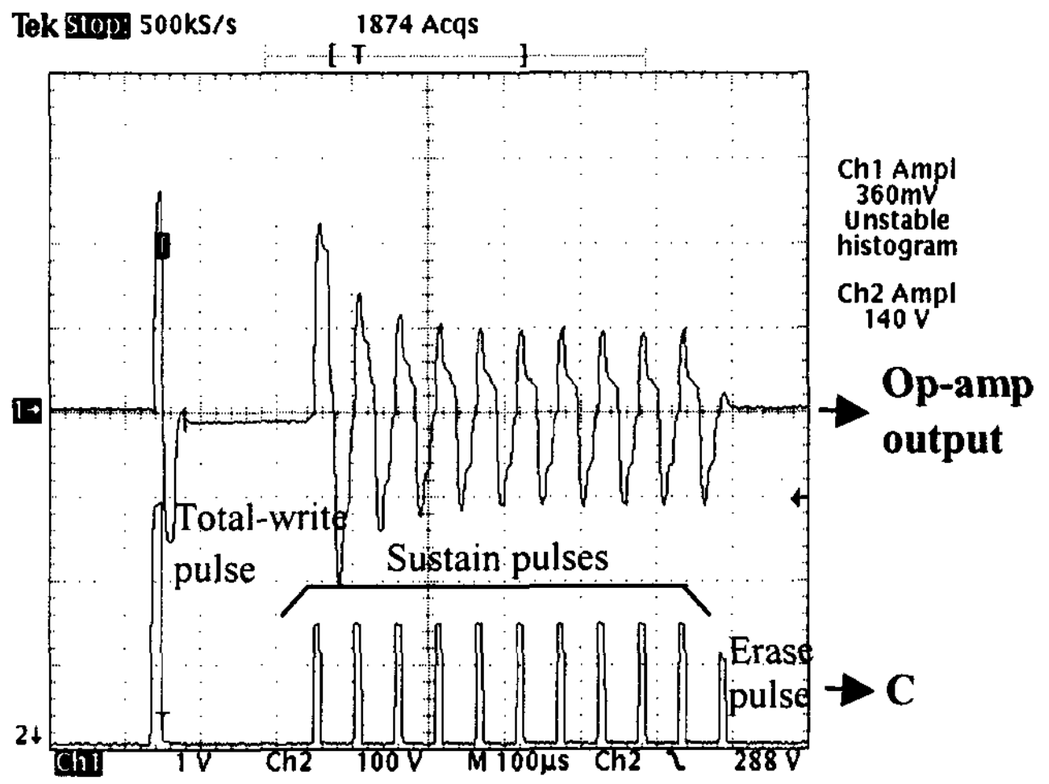

Figure 4. The measured waveform for Vs = 145V

3. Experimental Results

Using the proposed real-time wall charge measurement circuit, we measured the wall charge variations for the effects of sustain voltage, sustain pulse width, sustain frequency, and neighboring cells.

The effects of sustain voltage V_s on wall voltage are shown in figure 5. The wall voltage is proportional to the op-amp output voltage. The period and pulse width of the sustain pulse are 54μs and 9μs, respectively. For V_s below 140V, the sustain voltage is too low to support a stable sustain discharge. For $140 < V_s < 160$V, the wall voltage increases sharply

with V_s. For V_s above 160V, the wall voltage increases gently with V_s. V_s above 160V is suitable for the sustain operation, because stable sustain sequence can be accomplished.

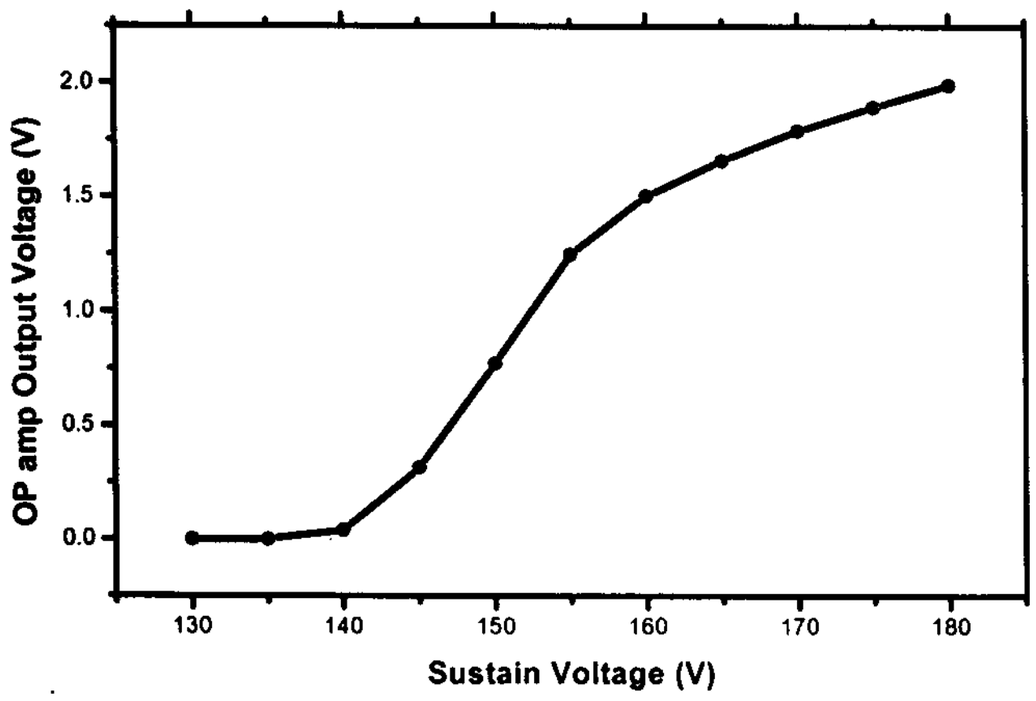

Figure 5. The effects of sustain voltage on wall voltage.

The effects of sustain pulse width T_s on the wall voltage are shown in figure 6. Sustain pulse width is varied by 3μs from 3μs to 15μs. The minimum sustain voltage is 150V for 3μs sustain pulse, and 140V for $T_s \geq 6\mu s$. The induced wall voltage increases with sustain pulse width for $T_s < 9\mu s$, and almost constant for $T_s \geq 9\mu s$. As the sustain pulse width increases, the more stable sustain discharge is induced. Accordingly, the minimum sustain voltage decreases and the induced wall voltage increases with increasing sustain pulse width. If both stability and time are considered, the sustain pulse width of 9μs is the most suitable for the sustain operation.

The effects of sustain frequency on wall voltage are shown in figure 7. Sustain frequencies to be tested are 27.8KHz, 18.5Kz, and 5.56KHz for the sustain pulse width of 9μs. The minimum sustain voltage is 145V for the sustain frequency of 5.56KHz, and 140V all for the sustain frequencies of 18.5KHz and 27.8KHz. Due to the priming effect, the minimum sustain voltage decreases with increasing sustain frequency.

The effects of neighboring cells on wall voltage are shown in figure 8. The driving conditions are the same as those for figure 5. Wall voltage characteristics are represented by the line [— • —] when only one line to be tested is turned on, and by the line [— ♦ —] when seven lines including six neighboring lines (three upper lines and three lower

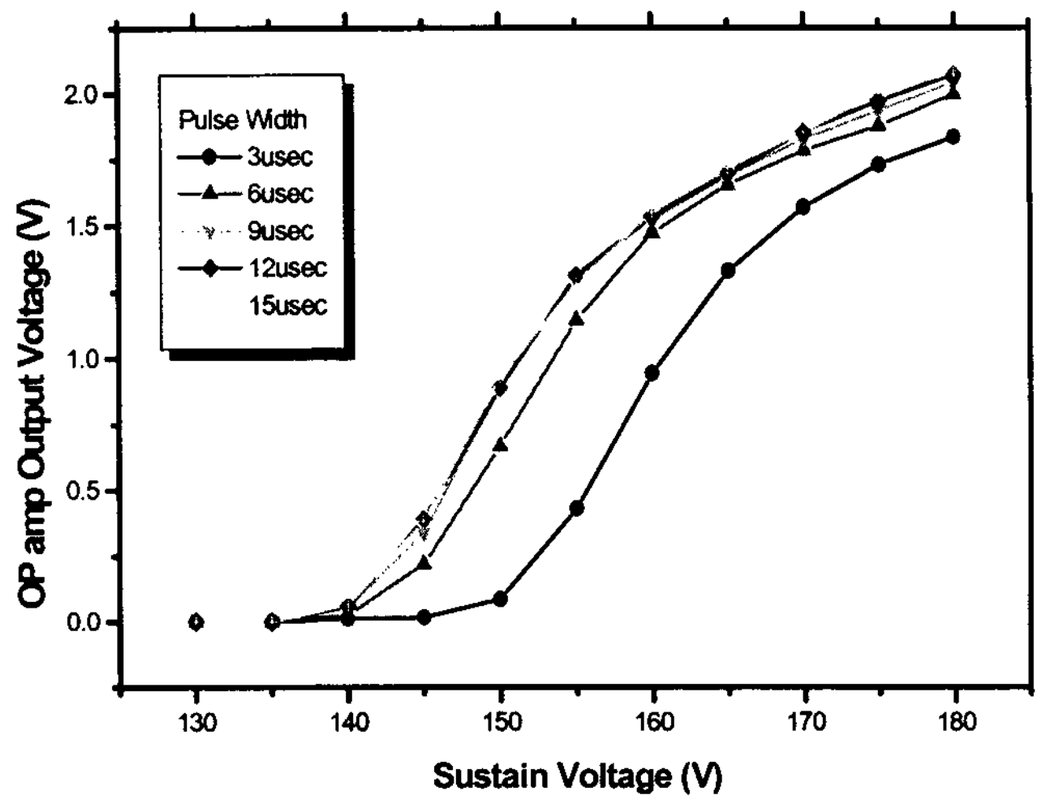

Figure 6. The effects of sustain pulse width on wall voltage.

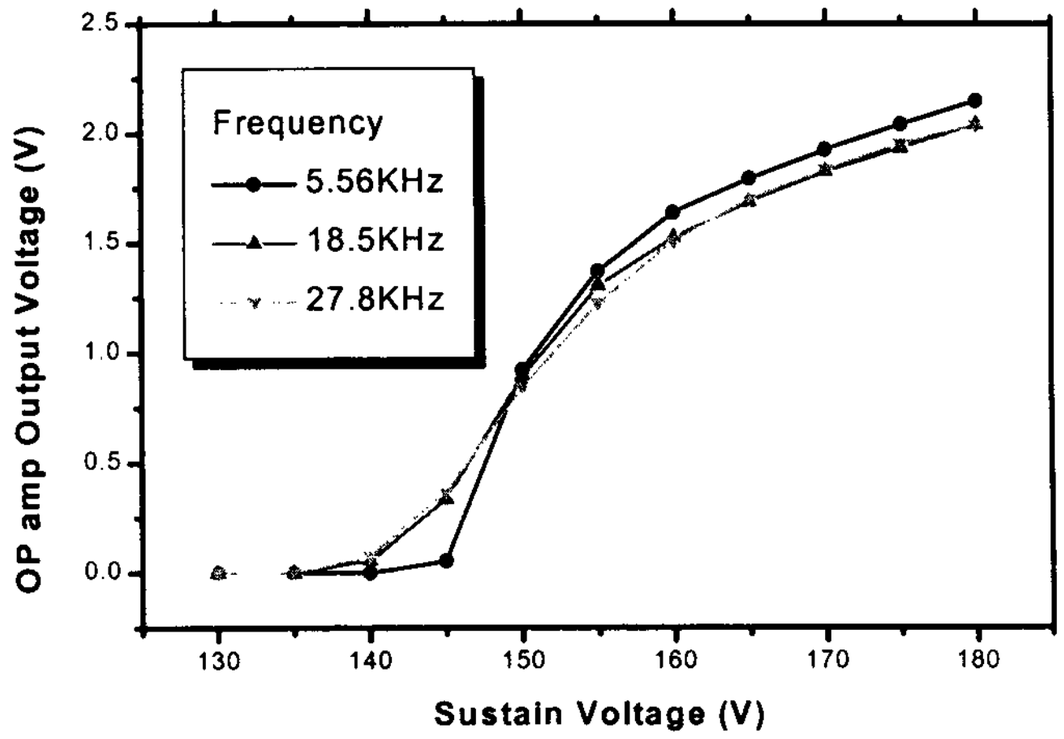

Figure 7. The effects of sustain frequency on wall voltage.

lines) are turned on. The more neighboring cells are turned on, the more wall charges are created and the induced wall voltage increases due to the priming effect.

The effects of sustain voltage on erase voltage are shown in figure 9. The driving conditions are the same as those for figure 5. As the sustain voltage

increases, the erase voltage decreases because the wall voltage induced by the sustain discharge increases.

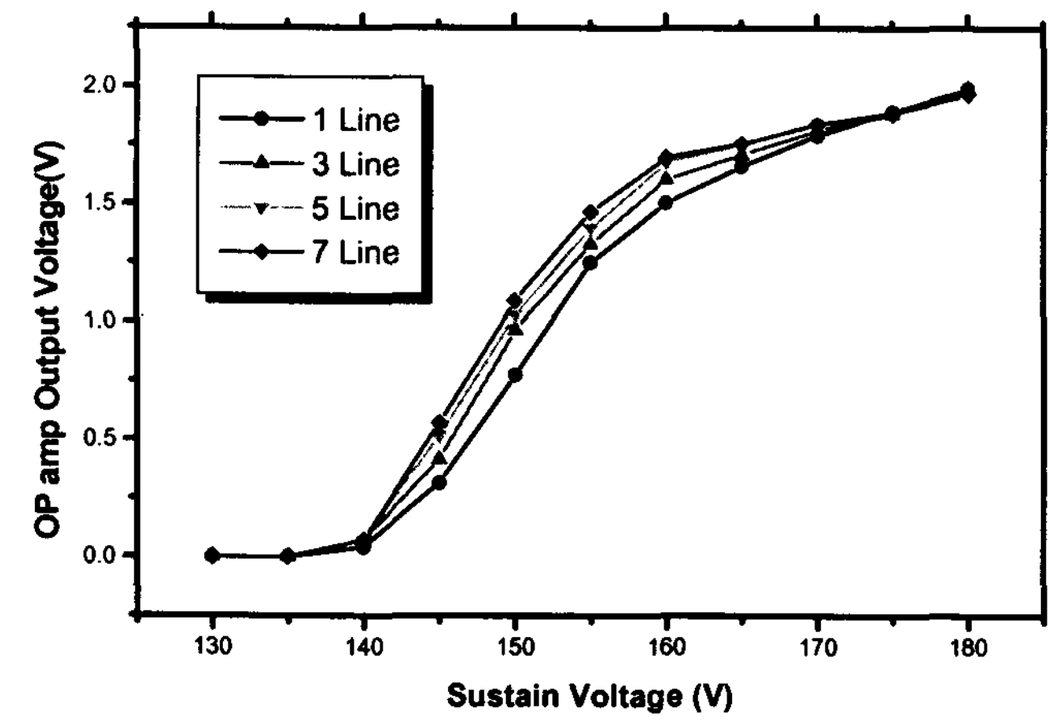

Figure 8. The effects of neighboring cells on wall voltage.

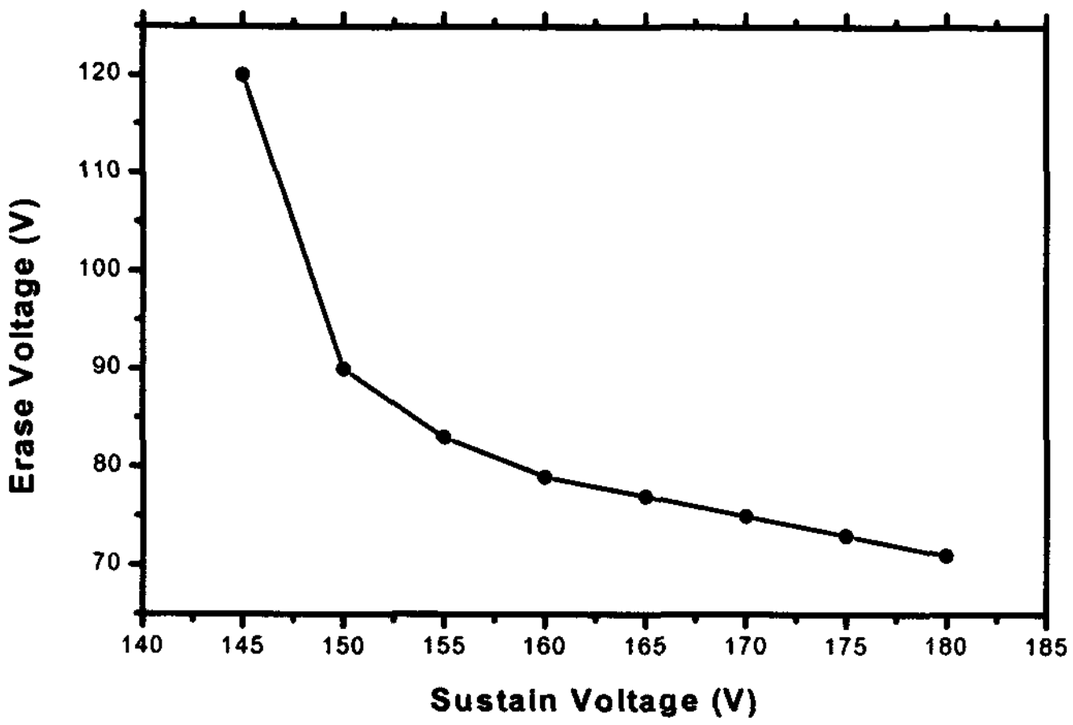

Figure 9. The effects of sustain frequency on wall voltage.

4. Conclusions

The proposed wall charge measurement equipment is relatively simple. By using this equipment, we can directly observe the wall charge variation for the drive waveform in a commercially large plasma panel. Therefore, the proposed equipment is expected to make great contributions to the development of new AC PDP driving methods.

5. References

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