Pentacene TFTs with Photoaligned Gate Insulator Surface

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Abstract

In this work, the electrical characteristics of organic thin film transistors with the surface-treated organic gate insulator have been studied. For the surface treatment, the photoalignment technique was used. The field effect mobilities of the devices with PVP gate insulator was improved about ten times as high as those of TFTs without the insulator surface treatment.

1. Introduction

Some organic materials have received considerable attention as semiconductors for the device applications such as thin film transistors (TFT) and light emitting diodes[1-6]. They can offer substantial advantages in terms of the processing simplicity and competitive cost. Recently, much attention to all-organic devices has been drawn[7, 8]. In this work, the electrical characteristics of organic TFTs with surface-treated organic insulator have been investigated. Pentacene was used as a semiconductor layer, and PVP(Polyvinylphenol) as a gate insulator. For a surface treatment, the photoalignment technique was used. The photoalignment technique is one of the promising methods to form induced orientation layers for liquid crystal displays. Applied to gate dielectric layers of inverted type organic TFTs, it might provide a preferential orientation of pentacene molecules, which would be deposited on the gate insulator(PVP) surface previously exposed to the linearly polarized UV light (LPUVL)[9].

2. Experimental Details

Pentacene(Sigma Aldrich) was thermally evaporated in vacuum at a pressure of about 10^{-6} Torr and at a deposition rate of 0.5 Å/sec. Aluminum and gold were used for the gate and source/drain electrodes, respectively. The metal electrodes were formed by thermal evaporations through shadow masks[10, 11]. During the evaporations, glass substrates were held at room temperature. PVP(Sigma Aldrich) film was coated by spinning, and patterned with acetone as a gate insulator. For PVP spin-coating, MEK(Methyl Ethyl Ketone) was used as a solvent. The thickness of the pentacene layer was about 60nm, which was confirmed by ellipsometry (Plasmos, SD-2100) and α-step profilemeter (Tenkor, 200). The channel length and width of TFTs were 50μm and 5mm, respectively. The insulator surface was UV-exposed before the pentacene layer is deposited on it. Figure 1 shows the molecular structure of the pentacene and PVP. The schematic structure of the device is shown in figure 2. To confirm the surface morphological changes, the atomic force microscopy (AFM; Park Scientific Instrument) was utilized. The electrical characteristics were measured by Keithley 238 and 617 source-measurement unit.

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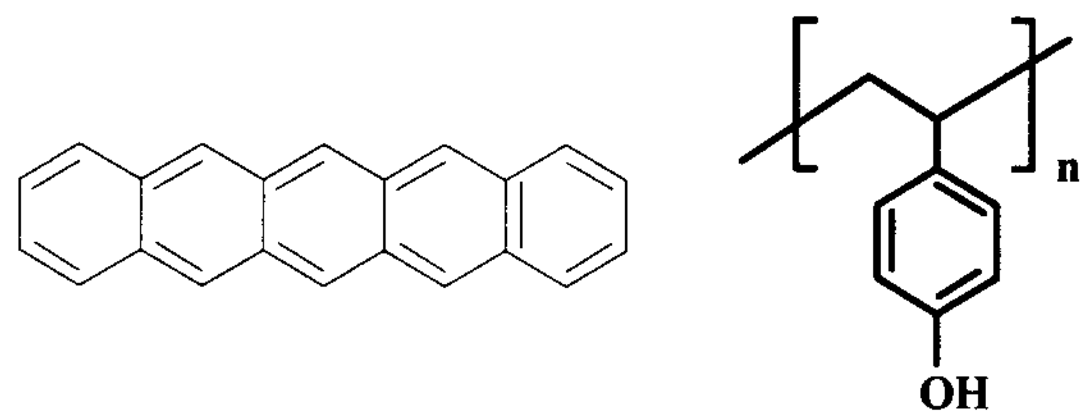


(a) (b)

Figure 1. Molecular structures of (a) pentacene and (b) PVP.

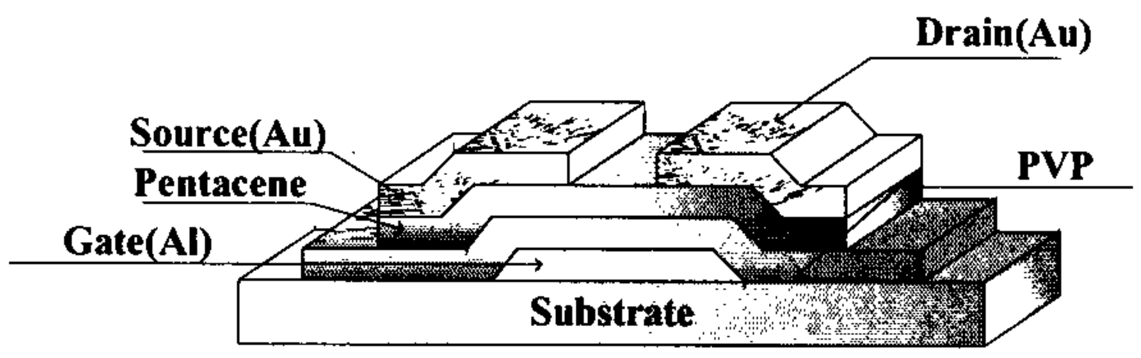


Figure 2. Structure of pentacene TFTs.

3. Results and Discussions

3.1 Photoreactivity of PVP(polyvinylphenol)

The photoreactive behavior of PVP film were studied as shown in figure 3. Varying the UV exposure time, the UV absorptions of the PVP film were measured. The anisotropic absorption characteristics of the PVP film represents the anisotropic photoreaction of surface PVP molecules, which is required for the photoalignment process. The photoalignment process is schematically presented in figure 4.

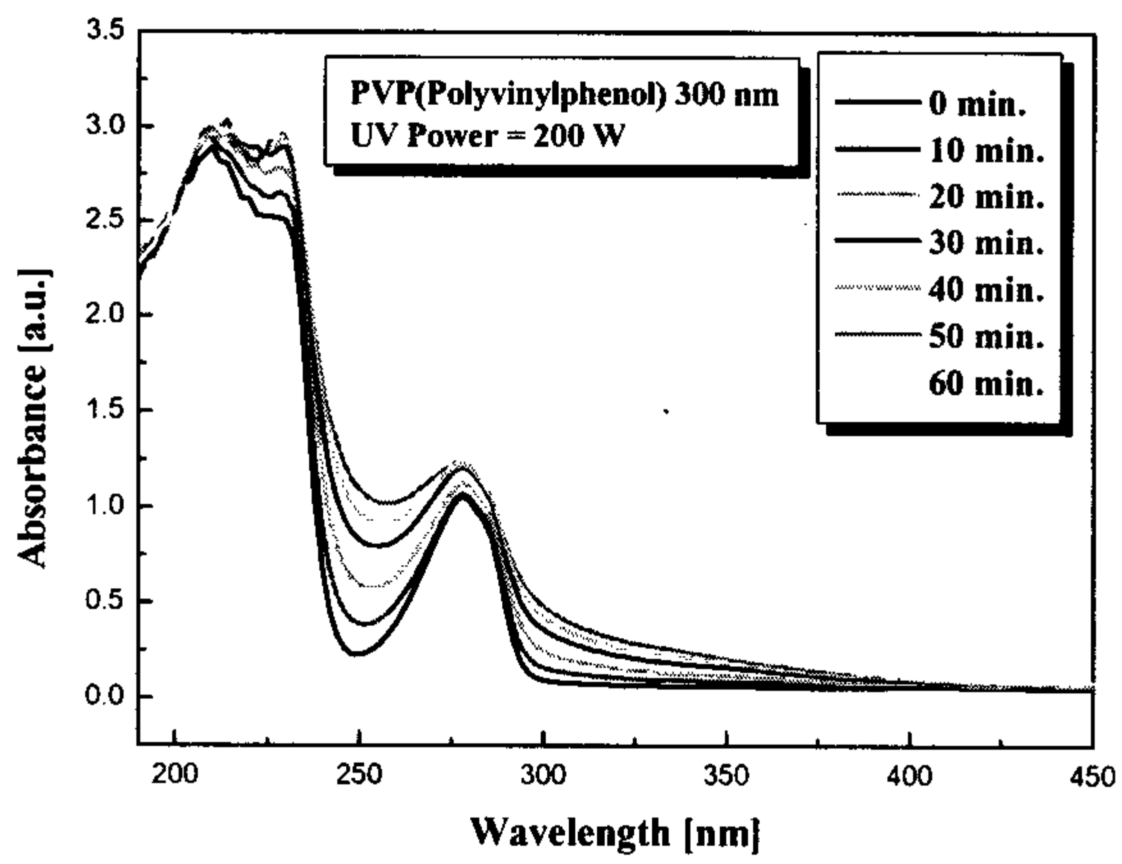


Figure 3. Anisotropic photoreactive characteristics of PVP.

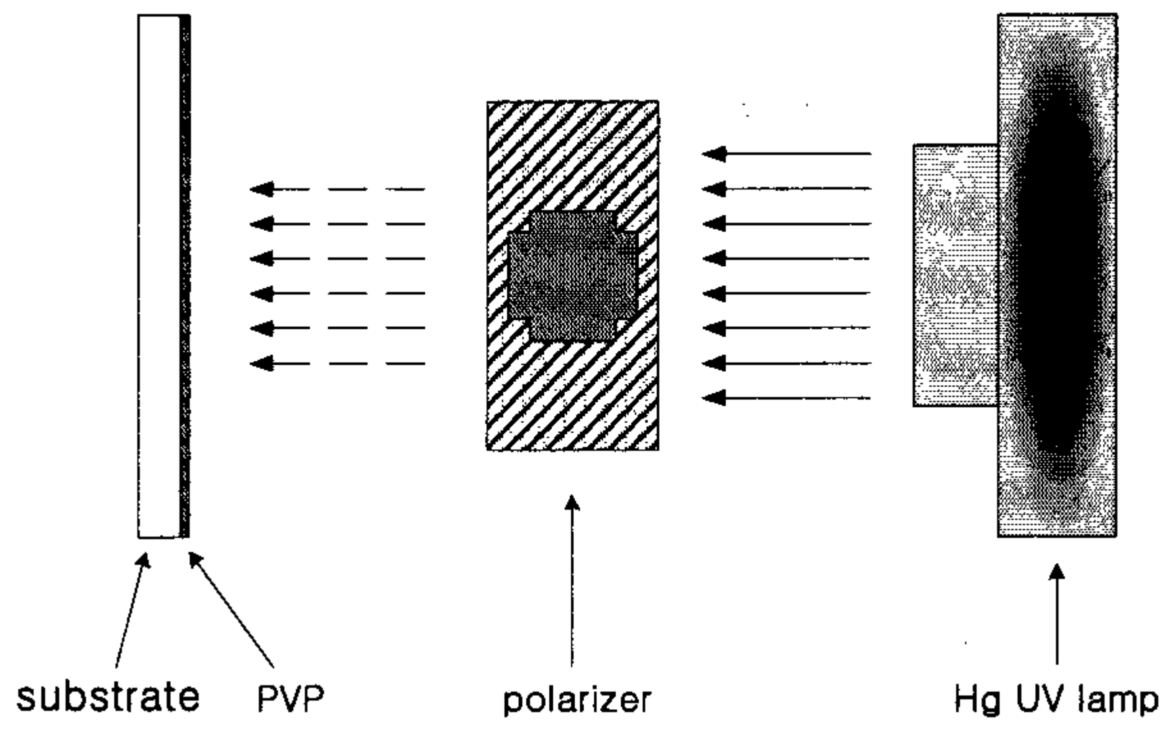
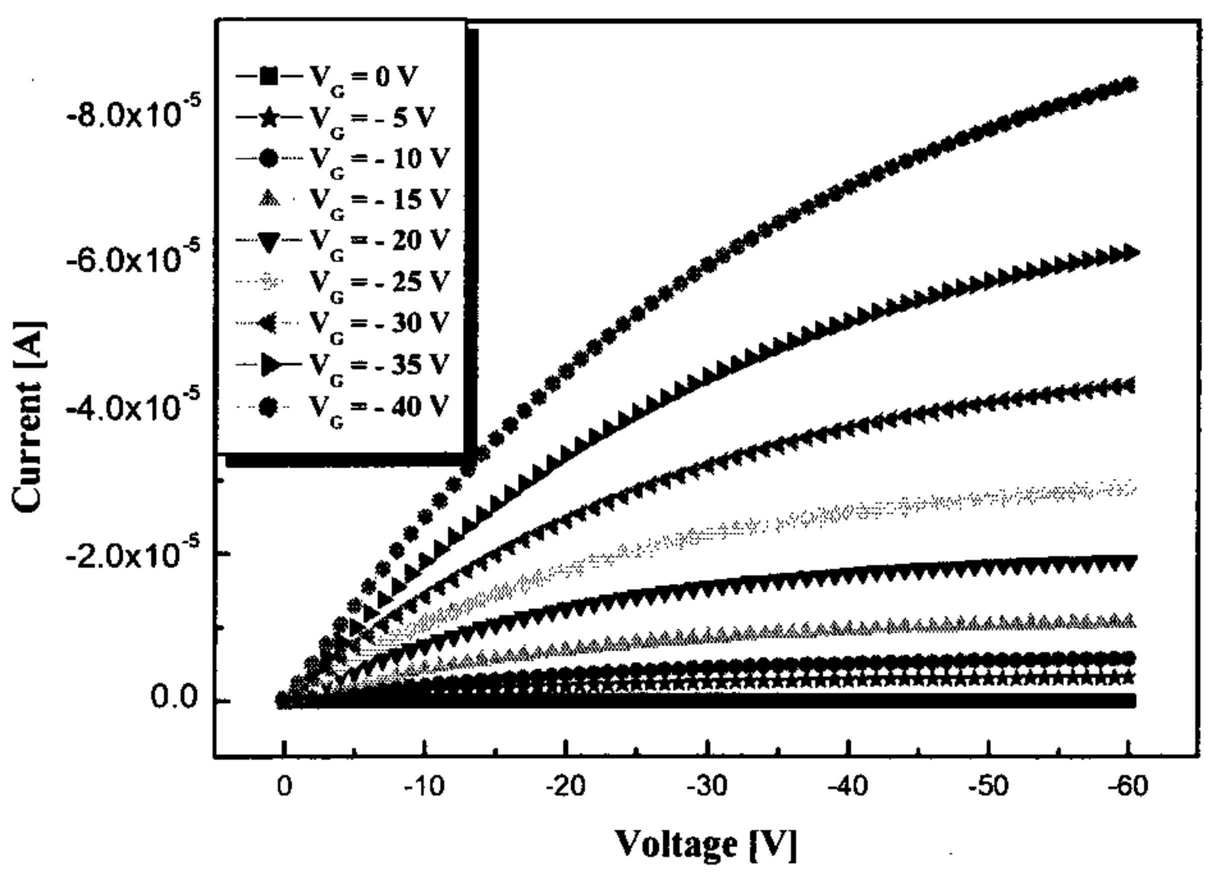


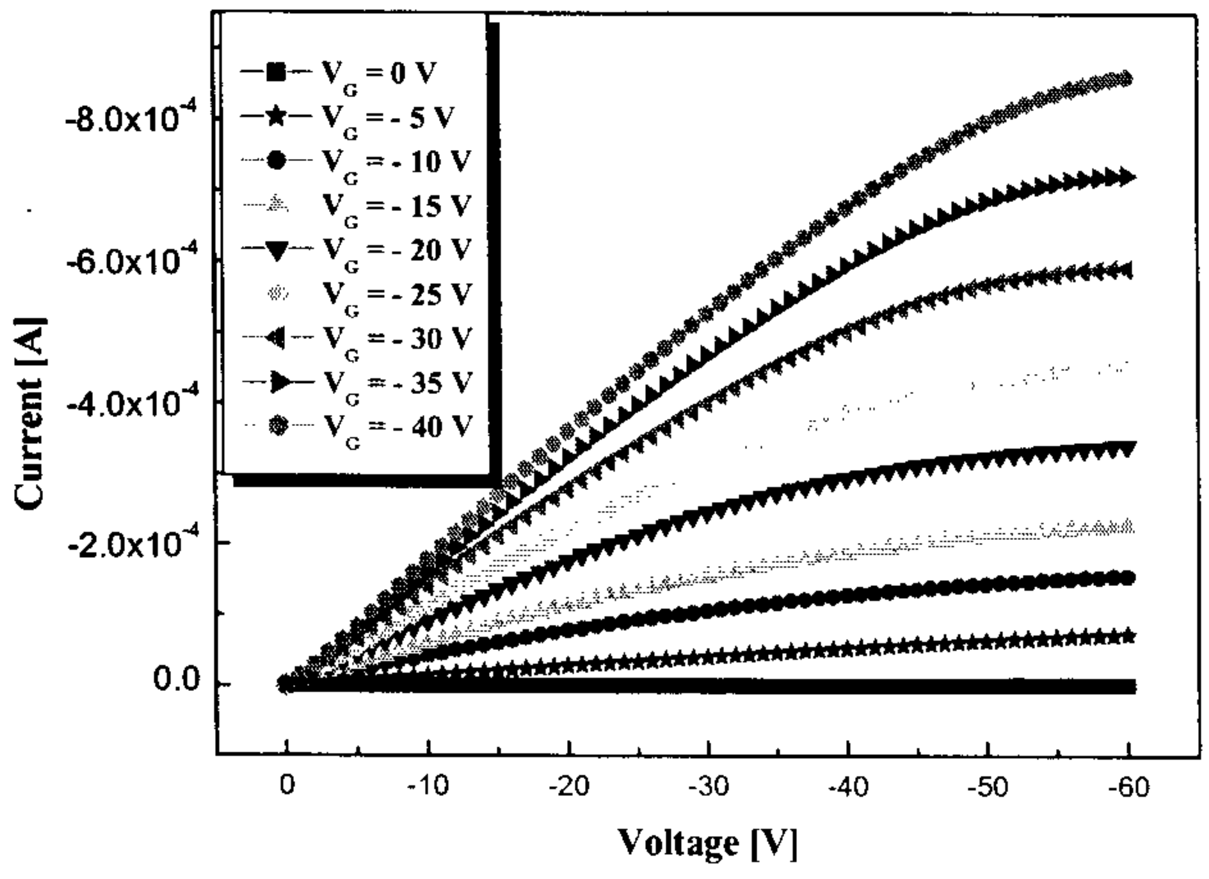
Figure 4. Photoalignment process of PVP surface molecules.

3.2 Electrical characteristics of devices

The output characteristics of the TFT without the surface treatment are shown in figure 5(a), and those with the photoaligned gate insulators are shown in figure 5(b). The TFT with the surface-treated PVP provides much improved output current levels. It is considered that the molecular orientation of pentacene molecules, induced by the photoalignment treatment, leads to the improved interface properties between pentacene and PVP layer. Figure 6 shows the transfer characteristics of the organic TFTs with as-deposited and photoaligned PVPs. The on/off ratios of the TFTs with treated and untreated PVPs are about 10^5 and 10^4, respectively.



(a)



(b)

Figure 5. Output characteristics of TFTs (a)with as-deposited PVP and (b) with photoaligned PVP.

The threshold voltage of the TFT with photoaligned gate insulator is about -3 V, while the TFT with as-deposited gate insulator has -9V threshold. The mobilities are extracted as 0.009 cm^2/Vs and 0.102 cm^2/Vs for the TFTs with as-deposited and photoaligned PVPs, respectively, using the equation below[12] ;

$$I_{DS} = \frac{W}{2L} \mu_{FET} C_i (V_G - V_T)^2$$

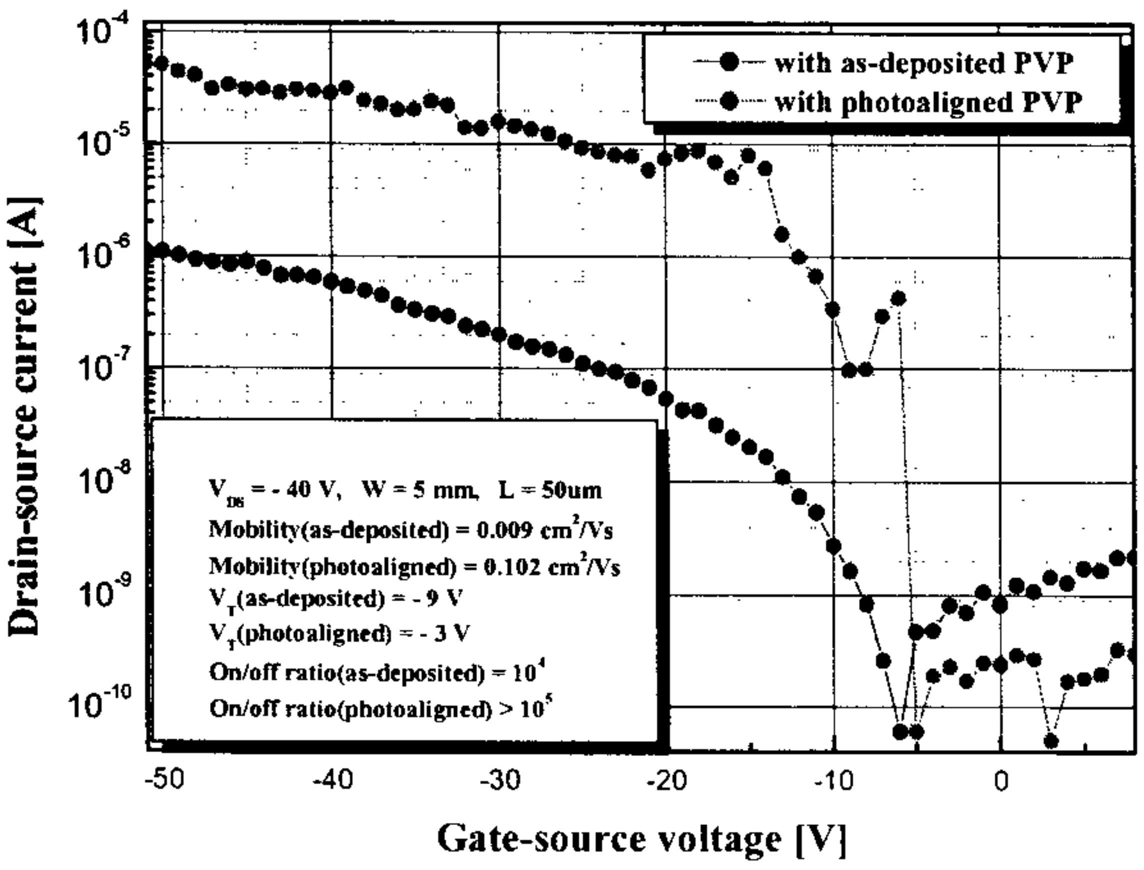
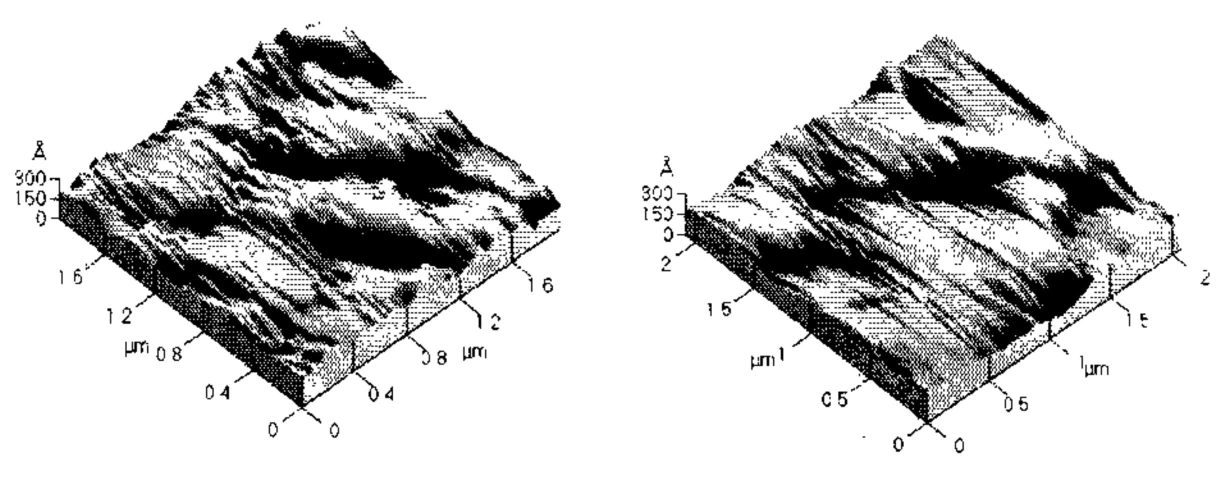


Figure 6. Transfer characteristics of TFTs.

The AFM images of as-deposited and UV-exposed PVPs are shown in figure 7. The surface of the photoaligned PVP shows smoother morphology than that of as-deposited one. Thus, the photoaligned insulator can provide better insulator/pentacene interface, which is attributed to the improved molecular orientation and adhesion of pentacene molecules to the gate insulator surface.



(a) (b)

Figure 7. AFM images of (a) as-deposited PVP and (b) photoaligned PVP.

4. Conclusions

The pentacene TFTs with surface-treated organic insulators were fabricated. The polarized UV-exposed PVP dielectric layer presents much improved surface roughness and thereby enhances the characteristics of the pentacene TFTs. As a result, it can be suggested that the UV-exposure of the photoreactive PVP surface may induce the orientational alignment of pentacene molecules deposited on it and subsequently enhances the electrical characteristics of the pentacene TFT. Most characteristic device parameters such as on/off current ratio, threshold voltage and carrier mobility are significantly improved by using the UV-exposed PVP layer as a gate insulator of TFTs.

6. References

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