New Material Architecture and Its Process Integration for a-Si TFT Array Manufacturing

Jean-Ho Song, Hong-Sick Park, Sang-Gab Kim, Hong-Je Cho, Chang-Oh Jeong,
Sung-Chul Kang, Chi-Woo Kim, Kyu-Ha Chung
AMLCD Division, Device Solution Network, Samsung Electronics Co. Ltd., KOREA
e-mail: jh.song@samsung.com

Abstract

In order to achieve higher performance and low cost a-Si TFT-LCD panel, new material architecture and its process integration for a-Si TFT array manufacturing method were developed. Material combination of low resistant dry-etchable metal and new pixel electrode under currently adopted 4 mask process made it possible to get more-simplified manufacturing method and better device performance for the a-Si TFT-LCD application. Proposed 4 mask process architecture with optimized wet etchants and dry etching process was applicable to various devices such as notebook, monitor and TV.

1. Introduction

TFT-LCD has prevailed in recently emerged digital display market and many technologies have been proposed to improve its device performance and manufacturing method. [1] Considering nearly saturated displaying qualities and LC technologies for wide viewing & fast response, many TFT-LCD panel makers have tried to reduce their production cost in terms of simplified manufacturing method for the cost effective device against other competitors such as FED, PDP and CRT. [2][3][4]

Nowadays, 4 mask process architecture and conventional combination of materials were introduced to breakthrough the theoretical limitation of photolithography count for a-Si TFT array. Although current 4 mask process took advantages of realizing less-mask concept and reducing essential photolithographic process, it has not been considered as true 4 mask process as its count due to cumulative manufacturing inefficiency and yield loss by improper material combination and confused process flows with redundant unit process.

Considering that mass production by increased productivity and reduced process step is the only way to achieve low production cost, new material architecture combined with more simplified 4 mask

process is the most-wanted prerequisite for a-Si TFT array manufacturing method.

2. New Material Architecture and Process

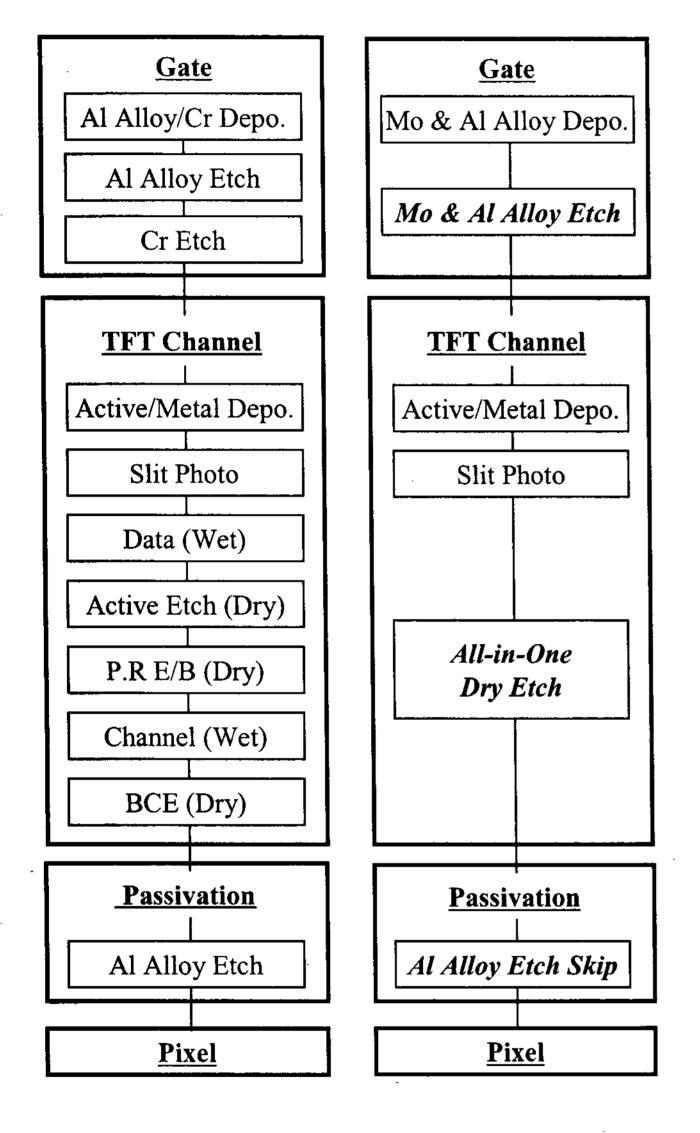
In order to improve many problems in current 4 mask process and realize more simplified manufacturing method, we innovated current 4 mask process architecture by replacing conventional material combination of Al alloy, Cr and ITO to optimized new material architecture of Al alloy, Mo alloy and IZO, as shown in Table. 1

Layer	Material (Etchant)		
	Current MA	Improved MA	
Gate	Al alloy (Al Etchant)	Mo alloy/Al alloy Mo Alloy	
S/D	Cr (Cr Etchant)	(Multi-purpose Etchant)	
Pixel	ITO & IZO (ITO Etchant) (Cr Etchant)	IZO (IZO Etchant)	

Table.1 Optimized New Material Architecture

Introduction of Mo alloy in new material architecture not only improved bus-line resistance and contact resistance with pixel IZO layer for IC pad formation, but also reduced redundant wet etchings for gate and passivation formation. But, we had to introduce Indium Zinc Oxide with its mild etchant as a pixel electrode to prevent chemical attack of data Mo alloy from vicious hydrochloric-based ITO etchant. Another benefit of dry-etchable Mo alloy as a data bus-line was more simplified process flow for TFT channel formation during slit photolithography.

Data formation of Cr-based 4 mask process requires 2 wet etchings for data bus-line and TFT channel during series of etching process respectively, which caused process inefficiency, yield loss by particle, confused equipment layout in the manufacturing line.



a. Current PAb. Improved PAFigure.1 Improved 4 Mask Process Flow

Application of Mo dry etching in the data and TFT channel formation gave very unique solution for the bunch of confused processes and simplified subsequent 5 etchings as consolidated all-in-one dry etching. Figure. 1 shows simplified process flow of improved 4 mask process with optimized material architecture.

3. Process Integration

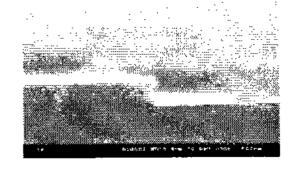
3.1 Wet Etching and Its Etchant

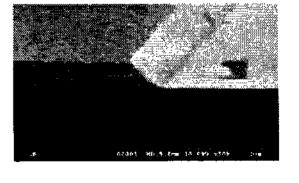
As Mo and Mo alloy are well-known bus-line materials in TFT-LCD industry, some panel makers adopted Mo and Mo alloy as their main electrode and well-developed dry & wet etching processes for single Mo layer were already established. But, In case of double-layered gate structure, Mo alloy/Al alloy gave serious limitation for both dry etch and wet etch during gate formation. It was unpopular to have Al dry etching for large substrate due to corrosion and equipment maintenance, moreover, the singular behavior of double layer at gate wet etching process resulted in non-uniformity, undesired taper and uncontrollable etch rate.

	Mo & Al Alloy	IZO
Com- ponent	HNO3, H3PO4 CH3COOH Stabilizer	HCl CH3COOH Inhibitor
Etch Rate	~ 50 Å / sec	~ 40 Å / sec
Taper	~ 50 degree	~ 60 degree
Skew	≤ 1.0 um	≤ 0.6 um
Uniformity	≤ 2.0 %	

Table. 2 Etchants for Electrode

Uniquely blended etchant for double-layered gate was developed from conventional Al and Mo etchants after considering singular etching behavior and electrochemical behavior of combined Mo and Al alloy, which satisfied process requirements such as uniformity, stable etch rate, and desired taper. Gate profiles of different etchants are shown in Figure. 2





a. Current Al Etchantb. Developed EtchantFigure 2. Gate Patterning and Taper

Because there was no optimized IZO etchant, Cr etchant or oxalic acid have been used for the most of IZO patterning, which resulted in high cost and increased processing time as well as storage and utility-maintaining problem. For the new pixel electrode of IZO, hydrochloric acid-based ITO etchant was modified to alleviate its aggressive etching behavior to other metal layers. Composition and process parameter for developed etchants are shown in Table. 2

3.2 All-in-One Dry Etching

Changing data material from Cr to dry-etchable Mo alloy made it possible to have series of dry etching flows during slit photolithography and TFT channel formation. Five sequential dry etching process composed of data etch, active etch, P.R. etch back, TFT channel etch and back channel etch are consolidated into all-in-one dry etching process. Because dry etching behaviors of Mo alloy and hydrogenated Si families were nearly same, whole etching process was optimized to have reasonable processing time and residue-free condition. Vertical structure of TFT channel after all-in-one dry etching is shown in Figure. 3.

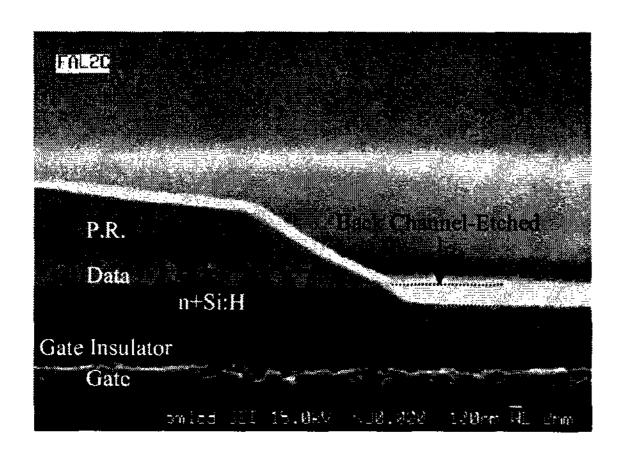


Figure. 3 Vertical Structure of TFT Channel

Although it was necessary to renovate dry etching equipment for metal dry etching, such as more powerful pumping-out system and heating jacket for chamber, consolidated all-in-one dry etching at single equipment with multi-chambers greatly improved manufacturing productivity and gave right solution to chronic problems of currently adopted 4 mask process.

4. Discussion

Since several attempts have been made to get more simplified TFT array manufacturing process in terms of reduced photolithography process, simultaneous patterning of 2 layers by using slit-mask or halftone-mask was successfully tested or applied to current manufacturing line. [5][6][7] Considering essential layers for fully integrated TFT arrays on substrate, at least 4 mask process are needed to have fully integrated back channel etch typed-process architecture with top pixel electrode.

Another approach for more simplified manufacturing process is optimized material architecture combined with process architecture and process flow as we presented in this paper. Considering many combinations from possible material candidates in the TFT-LCD manufacturing, Al alloy, Mo alloy and IZO are the best materials for the simplified manufacturing method from small-sized mobile devices to large-sized monitor & TV applications.

5. Conclusion

For more simplified a-Si TFT arrays manufacturing process, new material combination with improved 4 mask process architecture and drastically reduced unit process were developed.

Process	Current PA	Improved PA	
Photo	4		
Sputter	4		
CVD	2		
Wet	6	2	
Dry	4	2	
PR Strip	4		
Total	24	18	
Productivity	100 %	~ 125 %	

Table. 3 Productivity Comparison

Table. 3 clearly shows reduced process steps of proposed 4 mask process comparing to currently adopted one, resulting in at least 25 % increase of process productivity. Proposed manufacturing

method, featuring with low resistant materials, uniquely blended etchants, all-in-one dry etching process and noble slit photolithography made it possible to overcome many problems of conventional 4 mask process.

Finally, Proposed novel manufacturing method, optimized material combination with 4 mask process architecture, is not only totally compatible to current manufacturing line and equipment but also suitable for organic insulator process and other LC mode.

6. Acknowledgements

The authors would like to thank Dr. S. S. Kim and his R&D team. Also, we would like to appreciate Dr. J. H. Choi, Dr. S. H. Yang and Dr. C. C. Chai for their encouragement.

7. References

[1] P. Semenza, "FPD Market Analysis and Forecaster", IMID 01 special session, p41 (2001)

- [2] A. Van Calster et al., "A Simplified 3-Step Fabrication Scheme for High Mobility AMLCD Panels", SID 94, p289 (1994)
- [3] J. Glueck et al., "A 14-in.-Diagonal a-Si TFT AMLCD for PAL-TV", SID 94, p263 (1994)
- [4] A. Ban et al., "A Simplified Process for SVGA TFT-LCDs with Single-Layered ITO Source Bus-Line", SID 96, p93 (1996)
- [5] K. Ono, "A Simplified 4 Photo-mask Process for 24-cm diagonal TFT-LCDs", Asia Display 95, p693 (1995)
- [6] C.W. Han et al., "A TFT Manufactured by 4 Masks Process with New Photolithography", Asia Display 98, p1109 (1998)
- [7] C.W. Kim et al., "A Novel Four-Mask-Count Process Architecture for TFT-LCDs", SID 2000, p1006 (2000)