Low-Power, High Slew-Rate OP-AMP for Large Size, High Resolution TFT-LCDs

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Abstract

We have developed a low-power, high slew-rate OP-AMP for large size and high resolution TFT-LCDs which have 8μA quiescent current with settling time less than 6μsec. The proposed OP-AMP contains newly developed the driving circuit of class-AB output stage which can achieve a low quiescent current less than 8μA and a slew-rate higher than 3.14V/μsec.

1. Introduction

As the size and resolution of TFT-LCDs are becoming larger and higher, capacitive and resistive loads of data lines increase according to the longer length of the data lines and one row line time decrease according to the more gate lines. In AMLCDs, a various voltage levels of signals are transmitted to a pixel precisely through the data lines whenever the pixel is located at the front-end or at the rear-end of the line. At the rear-end of RC-transmission line, the signal is delayed by the RC-delays and, if the one row line time is not sufficient, pixel cannot express a precise gray level due to the voltage level error. In order to reduce the error, OP-AMPs of the data driver must have high slew-rate so that can charge or discharge the data line to the desired voltage within the row line time. Because the slew-rate of a OP-AMP is proportional to the quiescent current of the OP-AMP, it is required more power dissipation for the high slew-rate. One method to achieve low-power and high slew-rate OP-AMP compared to the conventional one is reducing the OP-AMP's stages by merging there functions in one stage. In this paper, we proposed the driving circuit of class-AB output stage and its OP-AMP. Designed OP-AMP has an open-loop gain of 130dB, quiescent current of 8uA and settling time less than 6μsec.
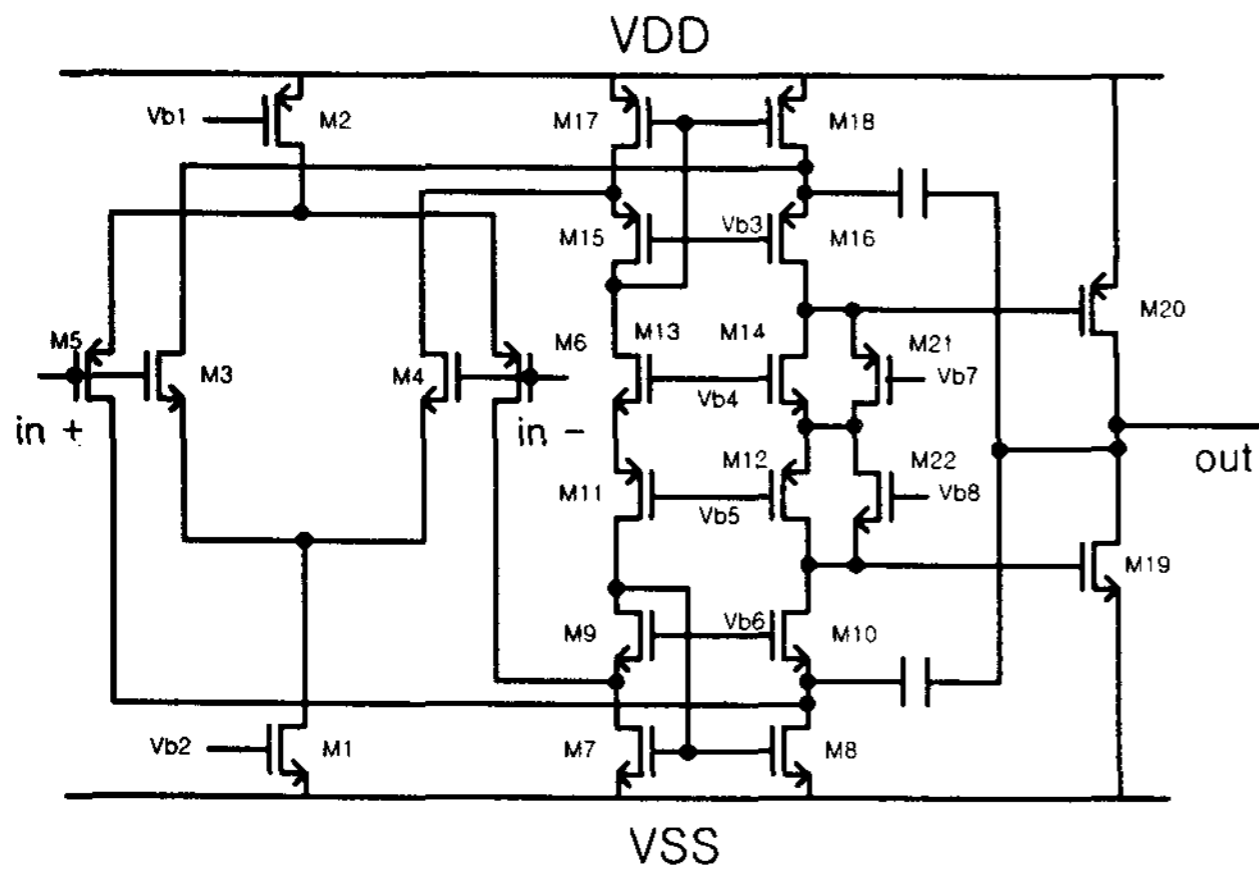
2. OP-AMP with Proposed Driving Circuit of Class-AB Output Stage

Generally, OP-AMPs for TFT-LCDs are composed of input stage, intermediate stage and output stage. Among these, intermediate stage controls the output stage and also dissipates the power. Proposed OP-AMP has no intermediate stage because the proposed driving circuit of class-AB output stage in the input stage can control the output stage.

Figure 1 shows the schematic diagram of the proposed OP-AMP with the driving circuit of class-AB output stage. It is composed of a rail-to-rail folded-cascode input stage which contains the driving circuit of class-AB output stage, and class-AB output stage.

In rail-to-rail folded cascode input stage, M11 and M13 act as a floating current source and define the current of left side cascode branch. The current is mirrored to right side cascode branch by M7 ~ M10 and M15 ~ M18. As shown in equation (1), because W/L of M11 and M14 are smaller than that of M12 and M14 with the same bias voltage, the current through M12 and M14 is smaller than the current through M11 and M13. Because the current of left side cascode branch and that of right side cascode branch must be equal, the current difference between the current through M12 and M14 and the current through M11 and M13 flows through M21 and M22.

$$\left(\frac{W}{L}\right)_{M14} < \left(\frac{W}{L}\right)_{M13}$$
$$\left(\frac{W}{L}\right)_{M11} < \left(\frac{W}{L}\right)_{M12} \tag{1}$$

Figure 1. Schematic diagram of proposed OP-AMP with a class-AB output stage driving circuit.

Therefore, with the proper bias voltage on the nodes Vb7 and Vb8, the quiescent current of the class-AB output stage can be adjusted to the desired value as shown in equation (2).

$$V_{G\_M20} = V_{b7} - V_{GS\_M20}$$
$$V_{G\_M19} = V_{b8} - V_{GS\_M22}$$

(2)

In an operation with unity gain configuration, if input voltage is higher than output voltage, the voltage of node X falls toward the voltage of VSS as shown in figure 2-(a). Accordingly, both M12 and M21 are turned off and both M14 and M22 are turned on so that the gate voltages of the output stage fall toward the voltage of VSS through M14 and M22. Therefore, the output voltage is rising toward the same voltage level of the input voltage. Likewise, figure 2-(b) shows down-slewing operation. Because the driving voltage range of gate voltage of the output MOSs(M19 and M20) is almost from VDD to VSS, the width of the output stage transistor can be minimized compared to the conventional OP-AMPs.

3. Simulation results

Simulation conditions are VDD=10V, VSS=0V and temp=25°C. Figure 3 shows the simulation model for the step response of the OP-AMP. The load is the electrical model of one data line; the transmission gate is used as a switch of the charge-sharing, the 300 Ω resistor is the resistance of the bonding pad

between the data driver chip and TCP(Tape Carrier Package), and the 2pF capacitor is the model of the probe tip capacitance in real measurement. Figure 4 shows the result wave forms of the step response when input voltage is a pulse which swings from 0.2V to 9.8V assuming the black pattern. Settling time to the target voltage within 20mV error is less than 6μsec and slew-rate is 3.14V/μsec at the mid point of the transition. Figure 5 shows the simulation model for AC characteristics. The 2pF capacitor is the model of the probe tip capacitance in real measurement and

(a)

(b)
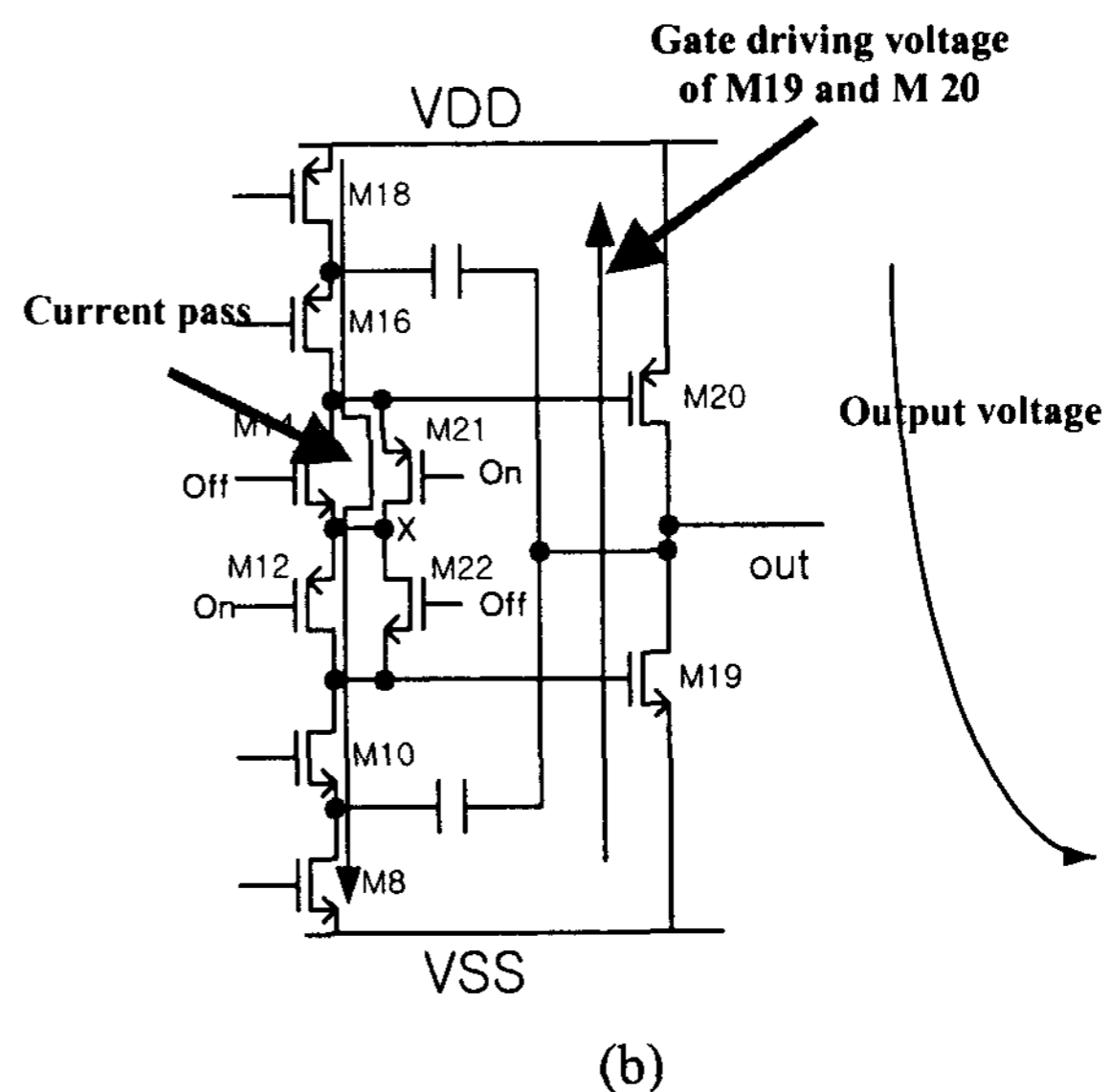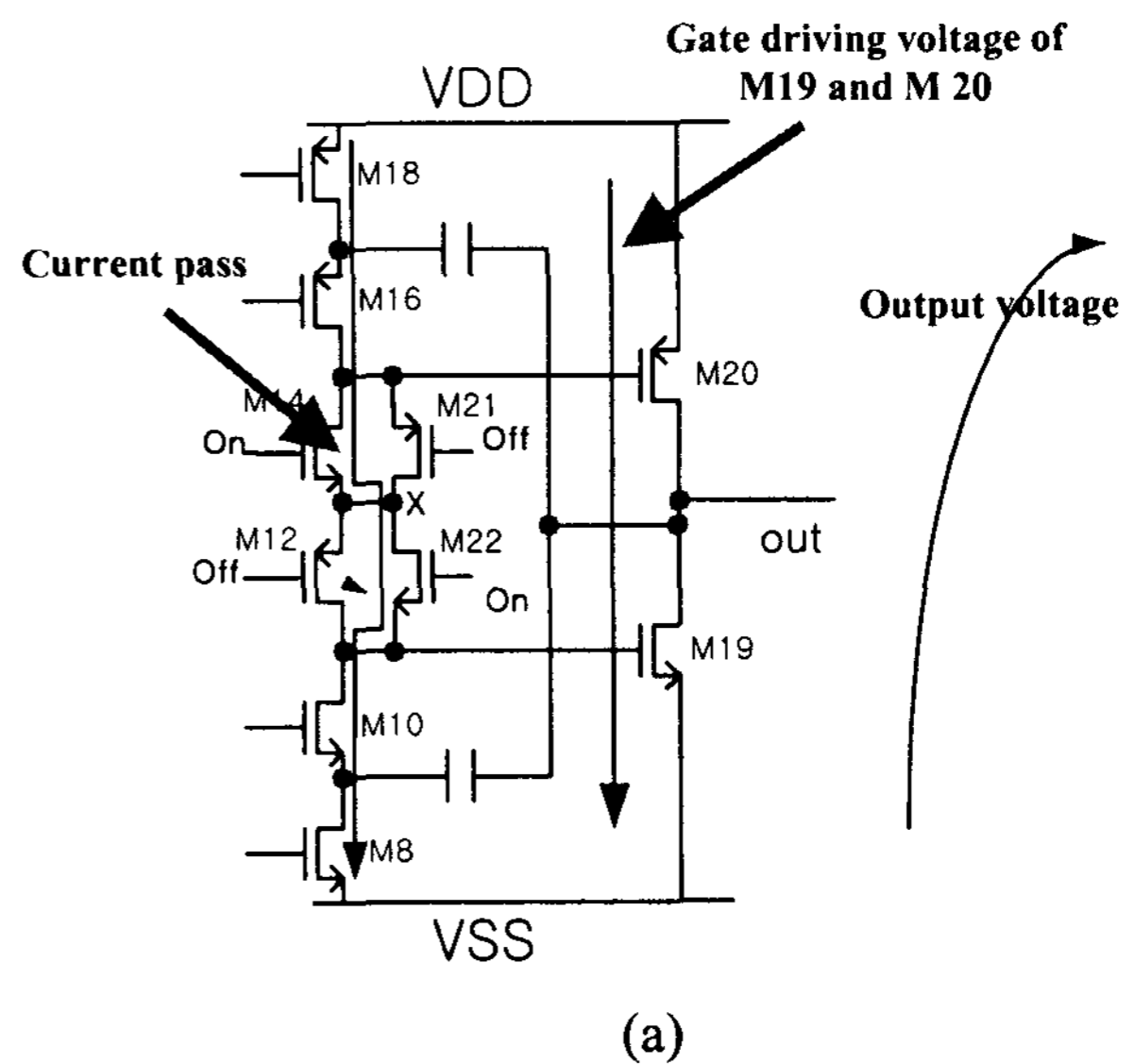
Figure 2. Operation of driving circuit of class-AB output stage ; (a) up-slewing operation and (b) down-slewing operation.
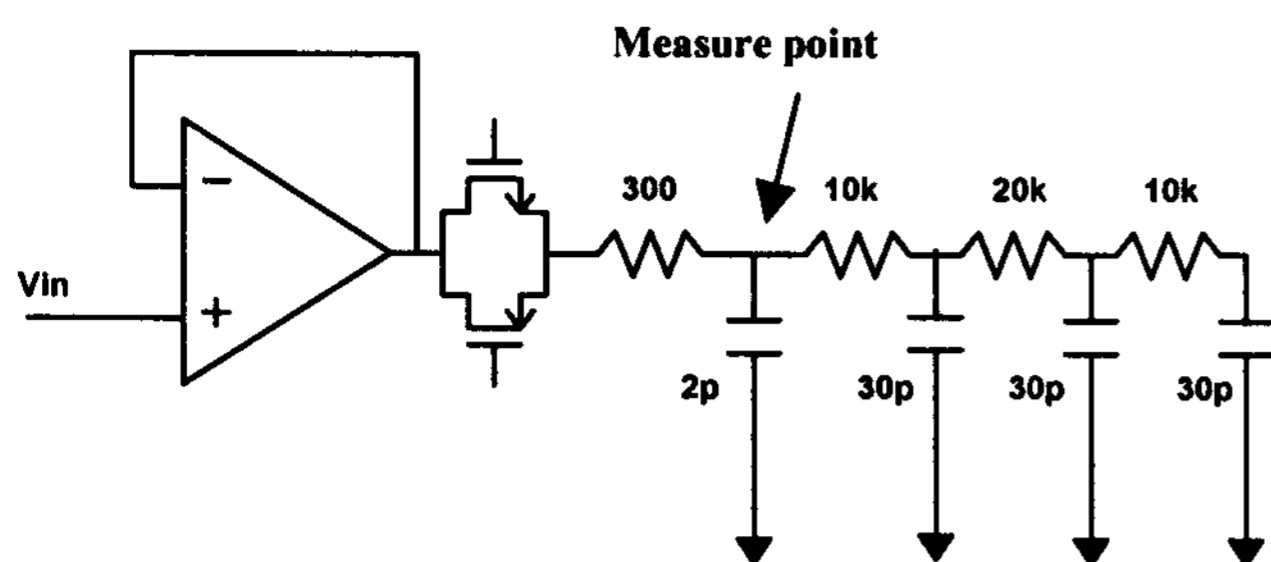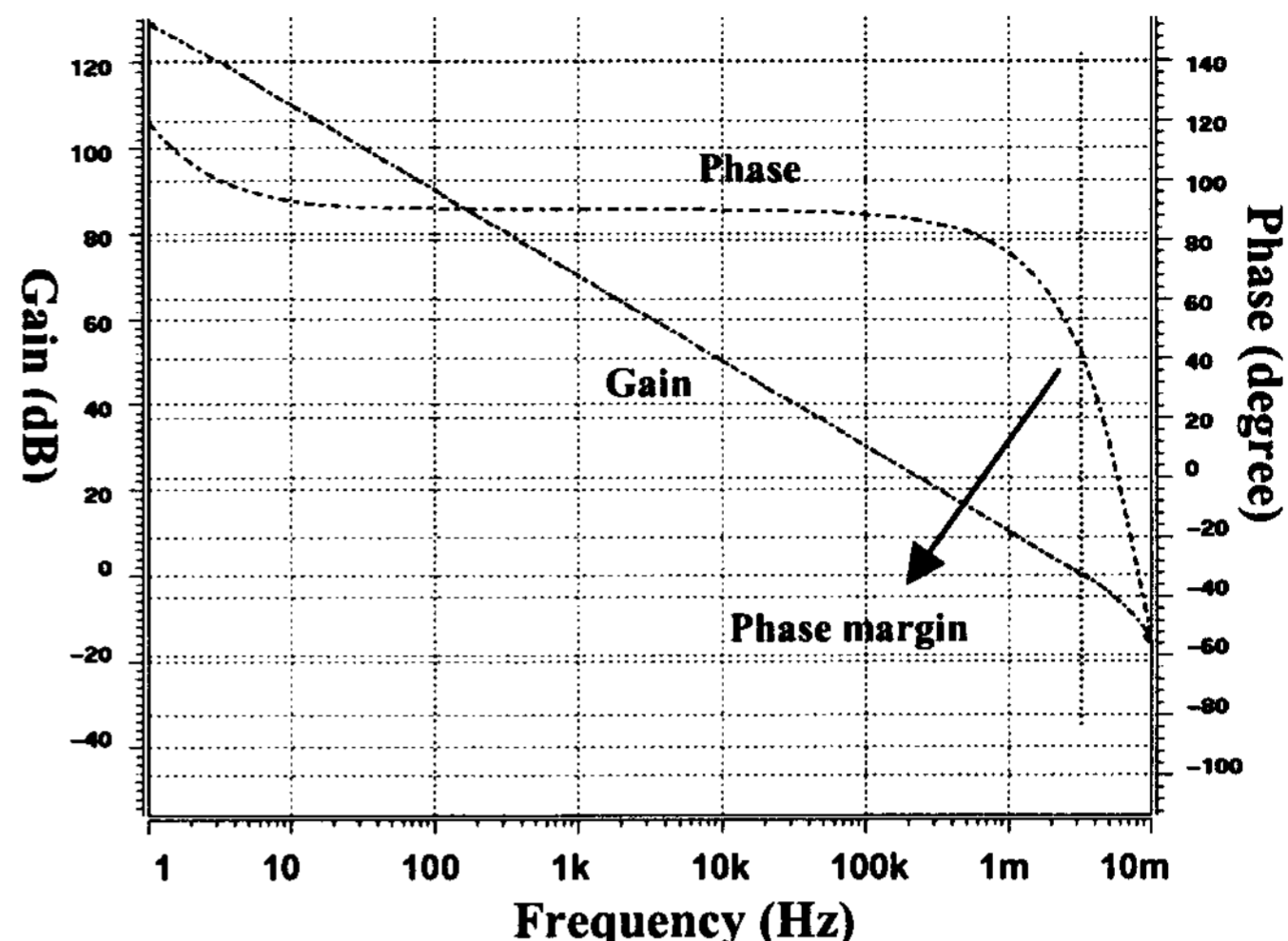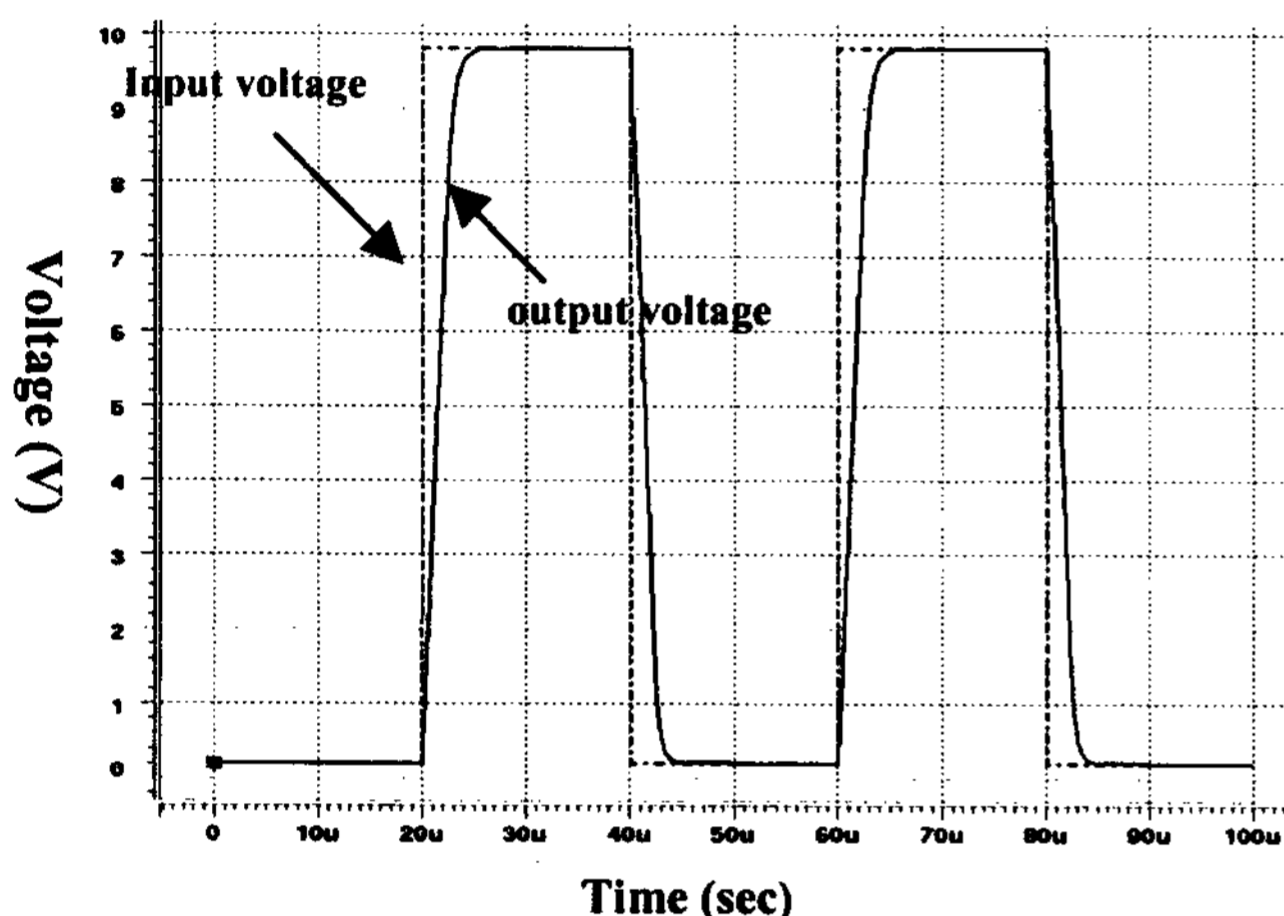
Figure 3.Transient simulation model.

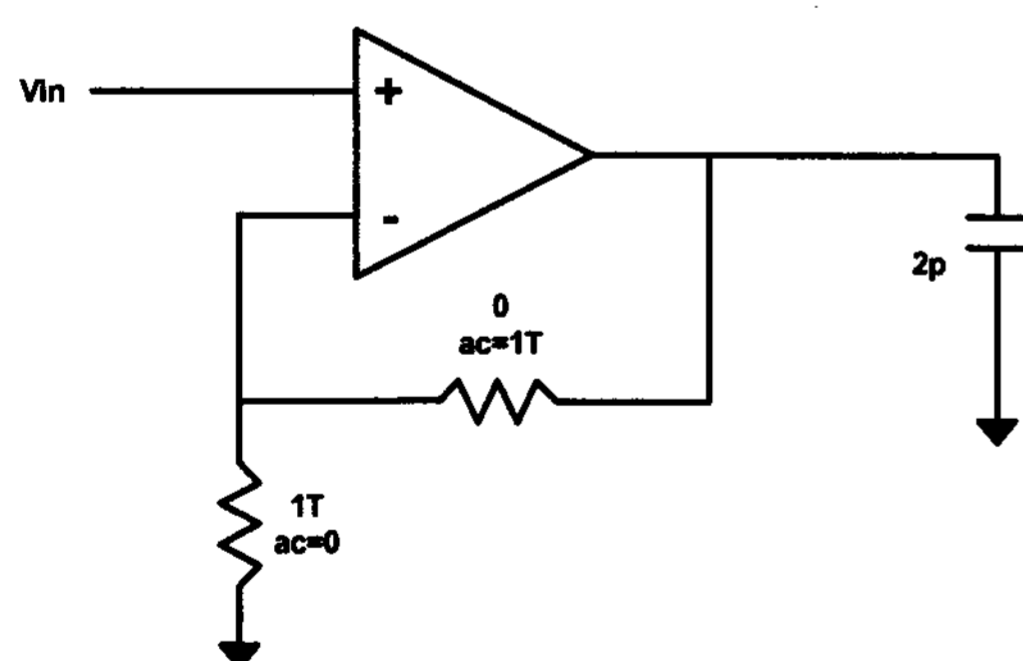**Figure 4.Transient simulation wave forms.**

Figure 5. AC characteristic simulation model.

figure 6 shows the AC characteristics simulation results. Open loop gain is about 130dB and phase margin is about 40°. The spec. of the proposed OP-AMP are summarized in table 1.

Figure 6. AC simulation results.

Table 1. OP-AMP specification.

VDD range (VSS=0)	8V~15V
Input range	0.2V ~ 9.8V
Open loop gain	≈ 130dB
Quiescent current	≈ 8μA
Slew-rate	≈ 3.14V/μsec
Phase margin	≈ 40°

4. Conclusion

Proposed OP-AMP with the driving circuit of class-AB output stage has slew-rate higher than 3V/μsec, quiescent current less than 8μA, open loop gain of 130dB and 40° of phase margin. Therefore, the proposed OP-AMP is suitable for the data drivers of large-area and high-resolution TFT-LCDs.

5. References

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