High temperature poly-Si thin film transistors on a molybdenum substrate

Do Young Kim, utpal gangopadhyay, Joong Hyun Park, Jae Kyung Ko, Junsin Yi
New material Lab., School of Information and Communication Engineering,
SungKyunKwan University, Kyunggi-do, Suwon, 440-746, Korea
Phone:+82-31-290-7139, E-mail: yi@yurim.skku.ac.kr

Abstract

The poly-Si thin film can be used in high mobility active matrix liquid-crystal display (AMLCD) and system on panel (SOP). In this paper, poly-Si thin films were grown by novel high temperature process on the molybdenum (Mo) substrate. By applying a high current above 48A on a Mo substrate. We obtained an improved crystalline Si films with the crystallinity over 80%. We exhibit the properties of structural and electrical properties of high temperature poly-Si thin film transistor on the Mo substrates.

1. Introduction

Many groups reported on the various low temperature poly-Si growth techniques such as excimer laser annealing[1] (ELA), metal induced crystallization[2] (MIC) and Electron cyclotron resonance plasma chemical vapor deposition[3] (ECR-CVD). But, Conventional glass using a TFT substrate had a limited anneal temperature and time. Others also have some limitations in terms of uniformity, impurity contamination, and the degree of crystallization. We developed the novel crystallization method that allows high temperature anneal and very fast crystallization. In this paper, we will illustrate the properties of poly-Si thin film transistors fabricated with high temperature process on Mo substrate.

2. Experiment

The schematic diagram for fabrication process of the proposed poly-Si TFT is show in Figure 1 Molybdenum substrate is about 150μm thick and was treated with H_3PO_4, HNO_3, and DI water solution for etching the natural oxide layer, followed by the rinsing with DI water, and drying with a nitrogen gas. A layer of n^+ a-Si:H having thickness of 25 nm was deposited by plasma enhanced chemical vapor deposition (PECVD), using PH_3, H_2, and diluted silane gas (20% SiH_4 in He gas), at 300℃ on the molybdenum substrate. The active a-Si:H layer of 900nm thickness was deposited by hot-wire chemical vapor deposition (HWCVD) using SiH_4 and H_2 mixture and was crystallized by RTP at various temperatures between 750℃ to 1050℃ for 3 minute. This process also can be applied for ohmic contact between a-Si and source/drain electrode also. Over the poly-Si, gate dielectric a-SiNx was deposited by PECVD using SiH_4 and NH_3 mixture gas at 300℃. A layer of 100nm thick aluminum film was deposited by thermal evaporation and defined as the gate electrode, using a photolithography. After the gate electrode definition, we attached the device to some material, such as glass, plastic, the other materials. At the last step, molybdenum substrate was defined as the source/drain electrode by photolithography.

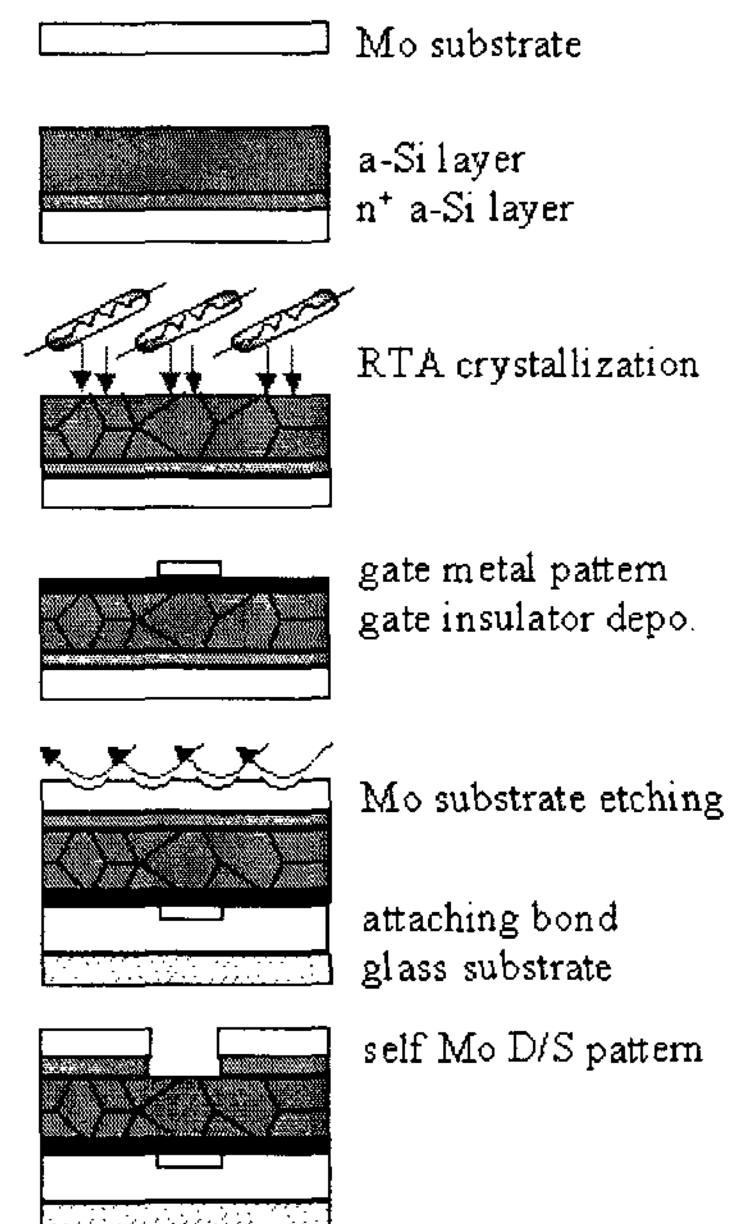

Figure 1. The procedure of high temperature thin film transistor on the Mo substrate

The proposed TFT devices have a channel width / channel length of 500, 300, 125μm /125, 100, 50 μm each other. The crystal volume fraction and the crystal structure of the poly-Si film was estimated using

Raman spectroscopy and X-ray diffraction (XRD), respectively. The electrical properties were measured by Fluke 5110B power source, Keithley 617 multimeter and computer system using GP-IB interface. Table 1 shows the several parameters used for films deposition.

Table 1. The conditions of sample preparation.

Deposition parameters	n^+ a-Si:H	a-Si:H	SiN_x
Pressure (mTorr)	140	57	160
Thickness (nm)	20	900	200
Deposition method	PECVD	HWCVD	PECVD
RF power (W)	400	-	200

The a-Si deposited by hot-wire CVD was crystallized from 750℃ to 1050℃ within 2min. Its film includes no any impurities and doesn't show chemical reactions between Mo substrates. The a-Si deposited by hot-wire CVD was crystallized at 850℃ within 2min. Its film includes no any impurities and doesn't show chemical reactions between Mo substrates. The thin film transistors were evaluated with a Fluke 5100B, Keithley 317, and Keithley 230 voltage source. All measurements were made with the probe station.

3. Result and Discussion

3.1 Active layer properties

For the study of the structural properties and crystal volume fractions, we carried out Raman spectrum. Figure 2 exhibits the Raman spectroscopy[4] as a function of the crystallization temperature. All of the sample have been observed Raman shift peak to the 521 cm^{-1}. It indicates crystallization in progress. It shows that crystal volume fraction (X_c) increases with the increase of crystallization temperature. We calculated X_c using the peak of 480 cm^{-1} indicating amorphous silicon and the peak 520 cm^{-1} indicating single crystal silicon. X_c can be expressed by following formula.

$$X_c = \frac{I_{520}}{I_{520} + \sigma I_{480}}$$

We assumed that grain size was very small and it is possible to hold σ=1. X_c of the devices varied with crystallization temperature and we achieved X_c of 92% at 1050℃. Also, the X_c is strongly influenced by crystallization temperature.

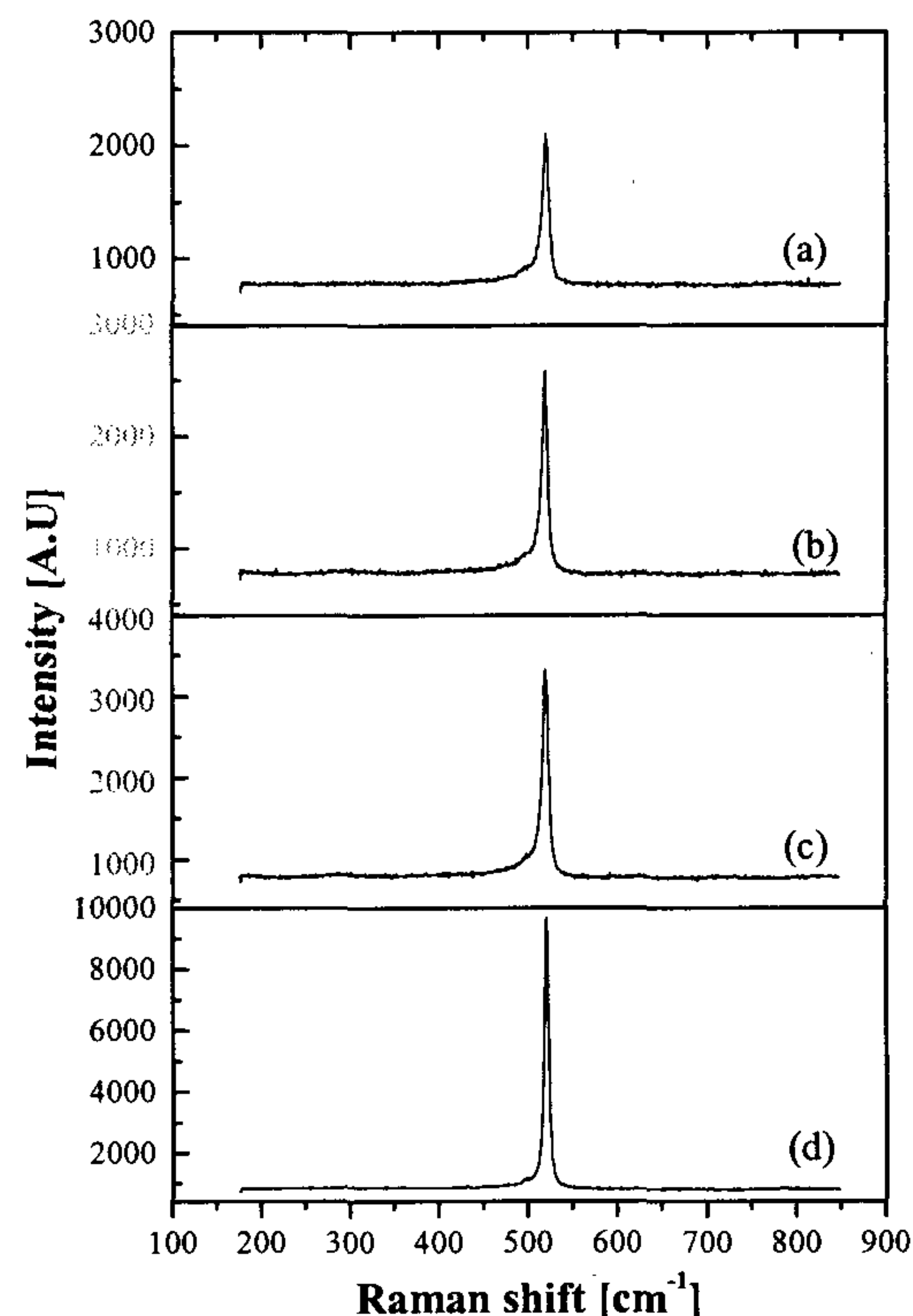

Figure 2. Raman spectroscopy as a function of crystallization temperature (a) 750℃, (b) 850℃, (c) 950℃, (d) 1050℃.

Fig. 3 shows the XRD patterns as a function of crystallization temperature. The peaks to the angle of 28° and 47° represent the Si (111), (220) orientation of samples. As the crystallization temperature increases, the intensity of the peaks increases with directions, gradually and decrease in full width at half maximum (FWHM)[5] that indicates crystallization degree. Though with increased crystallization time, such as 3 min, 5 min and 10 min, it could not show the change of XRD pattern much. And, it indicates that the crystal growth is dominated by not crystallization time, but temperature.

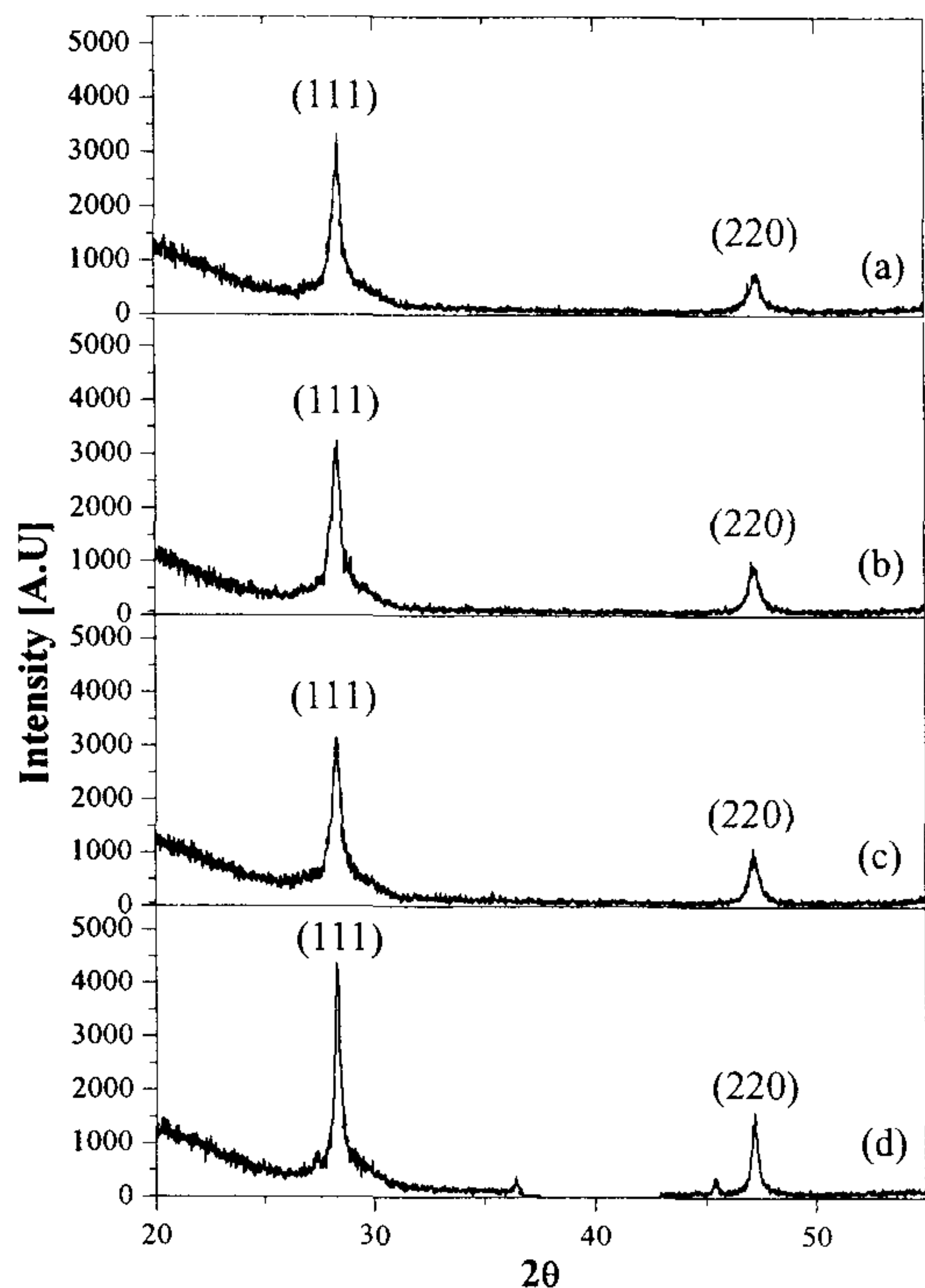

Figure 3. X-ray diffraction pattern as a function of crystallization temperature (a) 750℃, (b) 850℃, (c) 950℃, (d) 1050℃.

3.2 Thin film transistor characteristics

The optimum Si film thickness for TFT application was 1 μm.

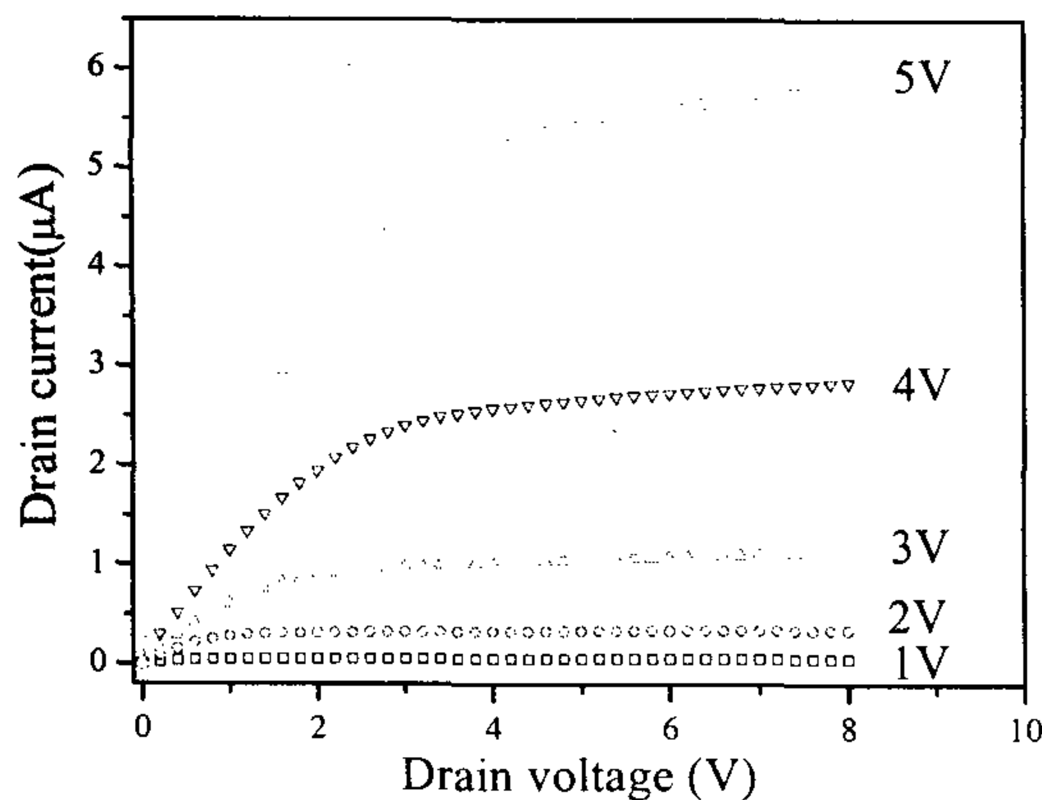

Figure 4. Drain voltage (V_d)-Drain Current (I_d) characteristics of high temperature poly-Si TFT.

Figure 4 shows the TFT output for a 1 μm thick film with increased drain current and transconductance. As Si film thickness was less then 1 μm, TFT output degradation was observed. This may have come from Si film non-uniformity due to the Mo substrate surface conditions. The TFT on a 1 μm thick Si film exhibited reduced drain current, reduced transconductance, reduced field effect mobility, and the drain current kink effect.

4. Conclusion

For getting good quality poly-Si, we tried to the high temperature crystallization, using RTP and achieved the high crystal volume fraction of 92%, the growth of (111) preferential orientation. We also have successfully fabricated poly-Si TFT having good characteristics. It was reserved that the device has a large I_{on} / I_{off} ratio and the field effect mobility is 68.6 cm^2/Vs. The inverted staggered type TFT gave a means of comparison for the a-Si:H versus poly-Si. Poly-Si TFTs have superior characteristics as compared with a-Si TFTs and is no doubt, a vary promising material. This flexible substrate is possible to treat high temperature and very promising roll-to-roll process. Also, molybdenum is useful for the flexible display application.

5. Acknowledgements

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6. References

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