Impact of Plasma Induced Degradation on Low Temperature Poly-Si CMOS TFTs during Etching Process

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Abstract

In this paper, we analyze the impact of plasma etching process induced device degradation on low temperature poly-Si TFTs. The results indicate the relationship between device degradation and PPID effect during plasma fabrication. The dual-gate structure, which is used to suppress leakage current, is also discussed in this research.

1. Introduction

In recent years thin film transistor liquid crystal displays (TFT-LCD) have been intensively investigated not only in active matrix liquid crystal displays but also in active matrix organic light emitter diode displays. In order to realize system on panel (SOP) technique, better device performance and reliability are necessary for circuit integration [1]. High electron mobility and low leakage current are the most concerns on the high-end displays research. Therefore, in order to suppress leakage current, dual-gate structure is inevitable applied on low temperature poly-Si TFT process, as shown in Figure 1.

Plasma process has a widely application in both semiconductor device and thin film transistor fabrication; such as plasma enhance thin film deposition, thin film sputtering, plasma etching, and ion doping. Unfortunately, it is one of critical reliability concerns in device manufacturing [2,3]. The impact to the devices might be occurred by crystal damage, exposure damage [4], radiation damage [5], and charging damage [6] during plasma processing. In this paper, the plasma process induced damage (PPID) of LTPS TFTs will be discussed.

In order to look into the process damage effect on low temperature poly-Si TFTs fabrication, the poly-Si etching issue and gate metal formation issue were studied in this work. This research results indicates the process damages of LTPS TFTs fabrication are really exist and cannot be ignored. It is essential to optimize the etching process on low temperature poly-Si TFTs manufacture.

2. Experimental

The basic process flow is described as follows. First, buffer oxide and 500 Å α-Si:H films were deposited on cleaned glass substrates by a plasma-enhanced chemical vapor deposition system (PECVD). The 50nm-thick channel film was formed by XeCl excimer laser crystallization and then the active area of TFT was patterned. The poly-Si etching experiments were executed in this step, the detail split conditions is shown in Table 1. Subsequently, 1000 Å gate insulator was deposited by plasma-enhanced chemical vapor deposition TEOS oxide followed by 410□ annealing. The low resistance molybdenum-tungsten (MoW) alloy was used for the gate metal. Different metal thicknesses were split from 2kÅ to 5kÅ

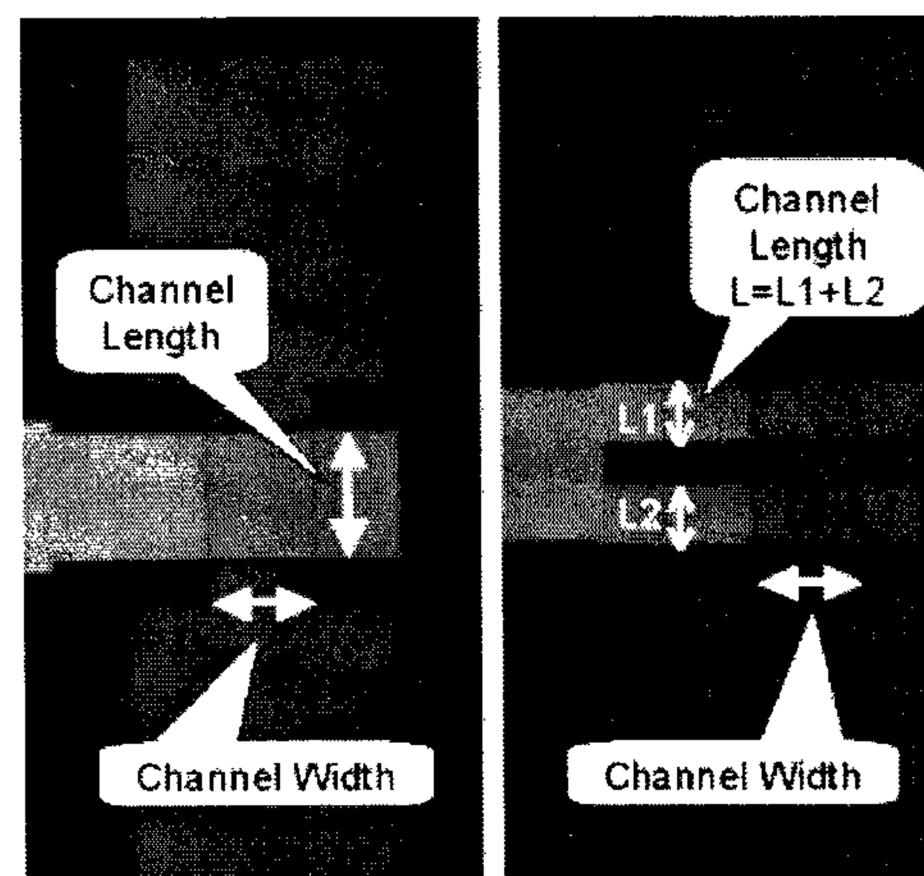


Fig. 1 Optical microscopy of single gate and dual gate structures LTPS TFTs.

	poly-Si etching recipe	Gate metal thickness
Exp. 1 poly-Si etch issue	Power 400W	MoW 3kA
	Power 600W	
	Power 1200W	
Exp. 2 gate metal etch issue	Power 600W	MoW 2kA
		MoW 3kA
		MoW 5kA

Table 1 Split conditions of plasma etching process for poly-Si etching and gate metal etching.

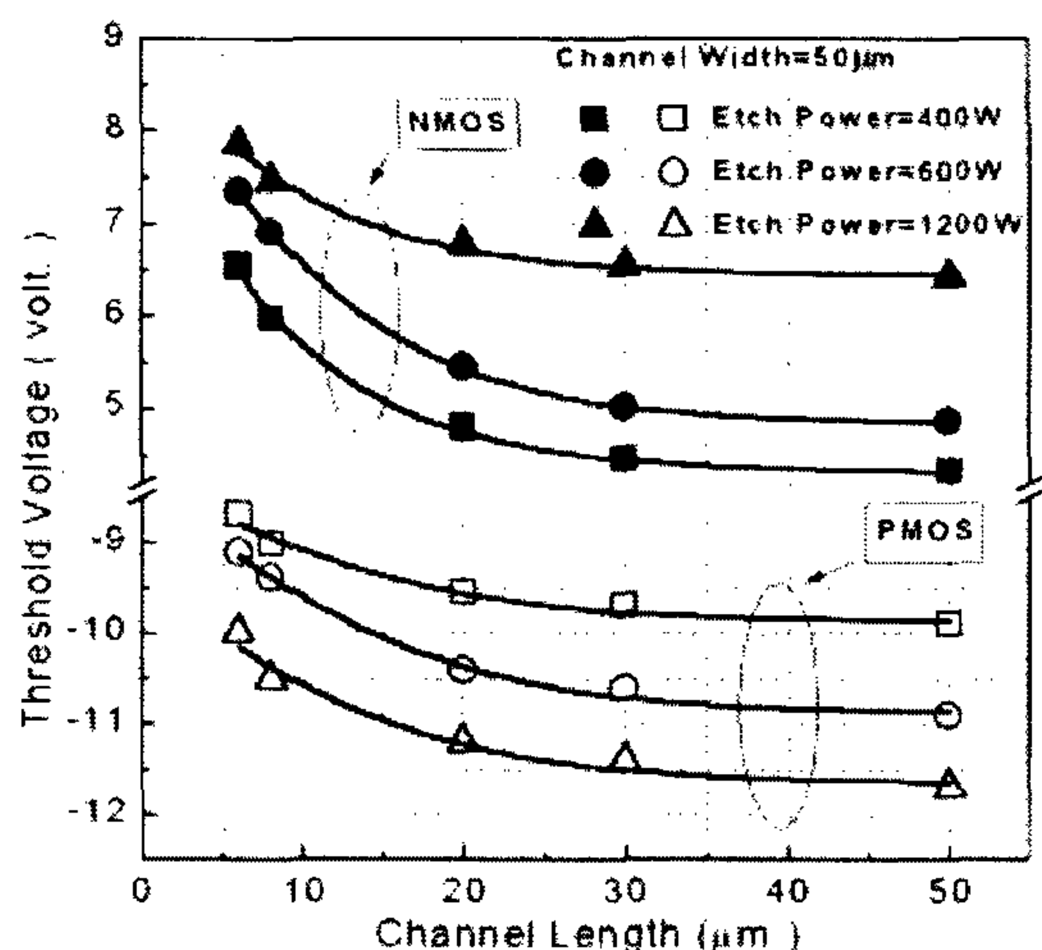


Fig. 2 Dependence of threshold voltage and channel length under various applied RF power.

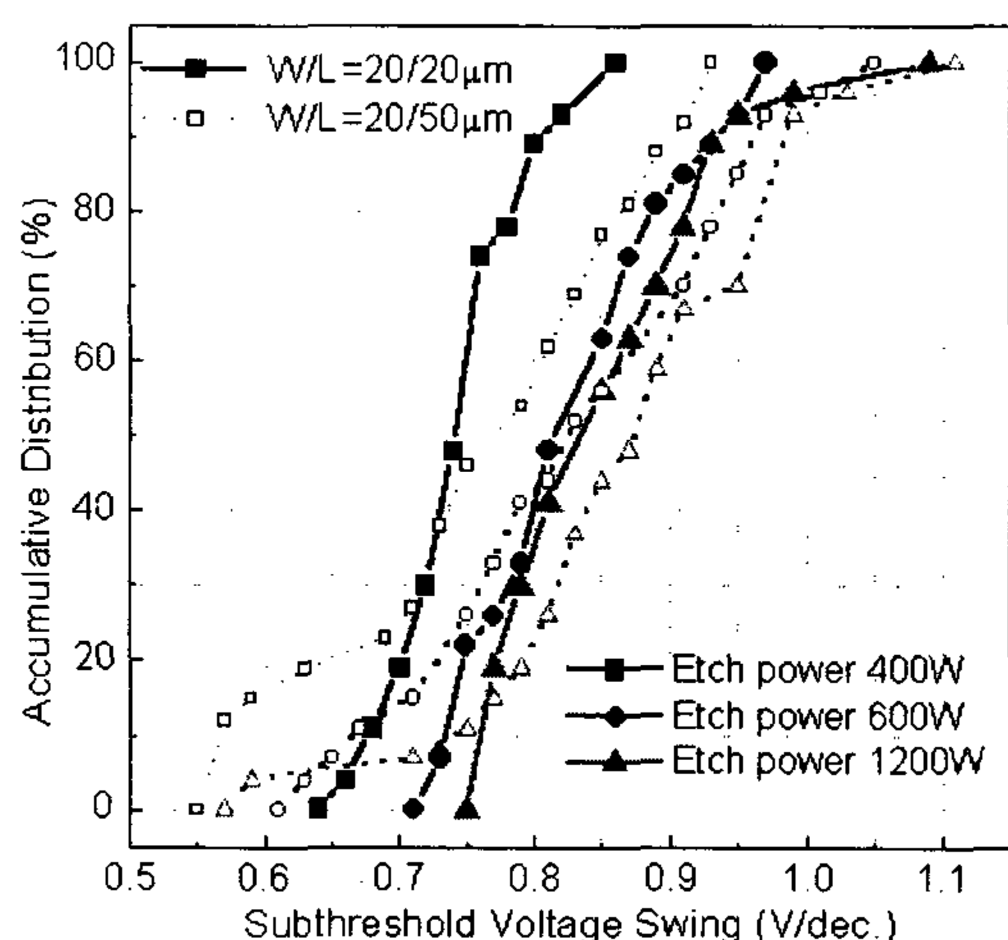
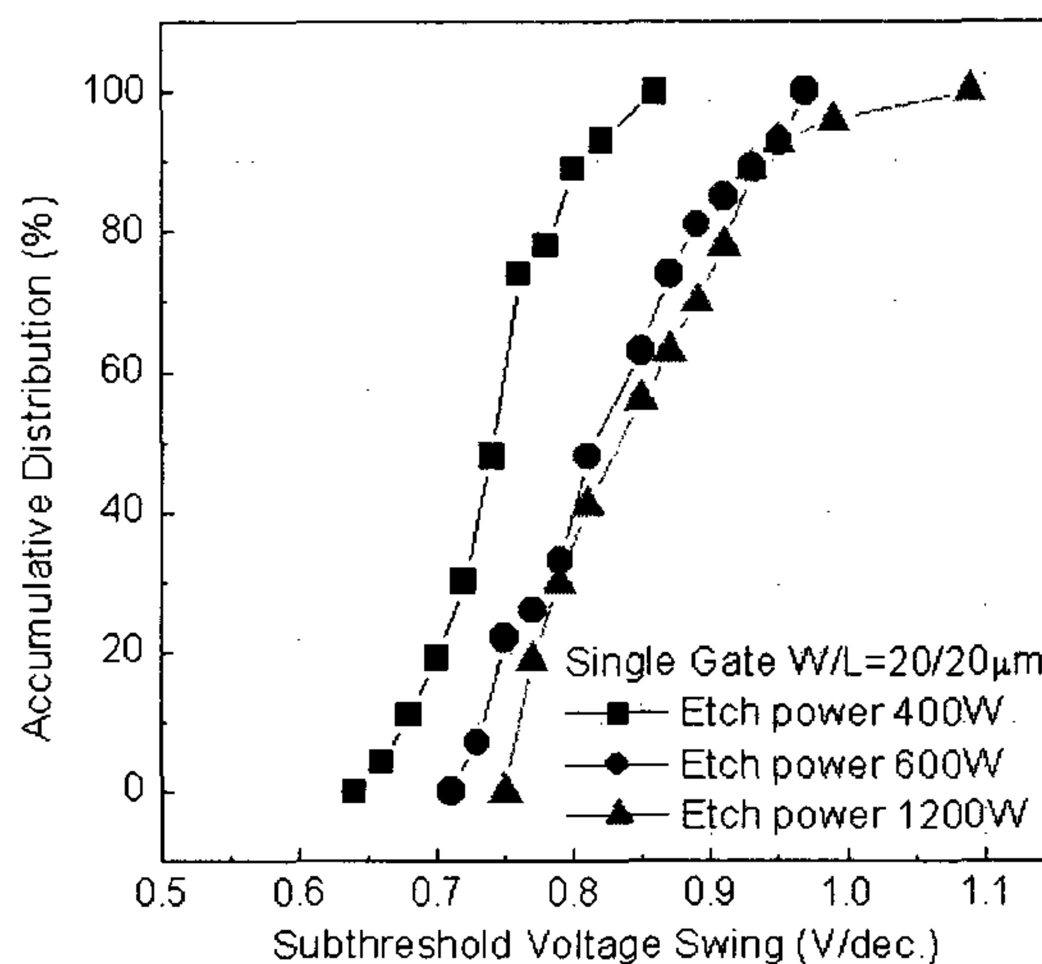
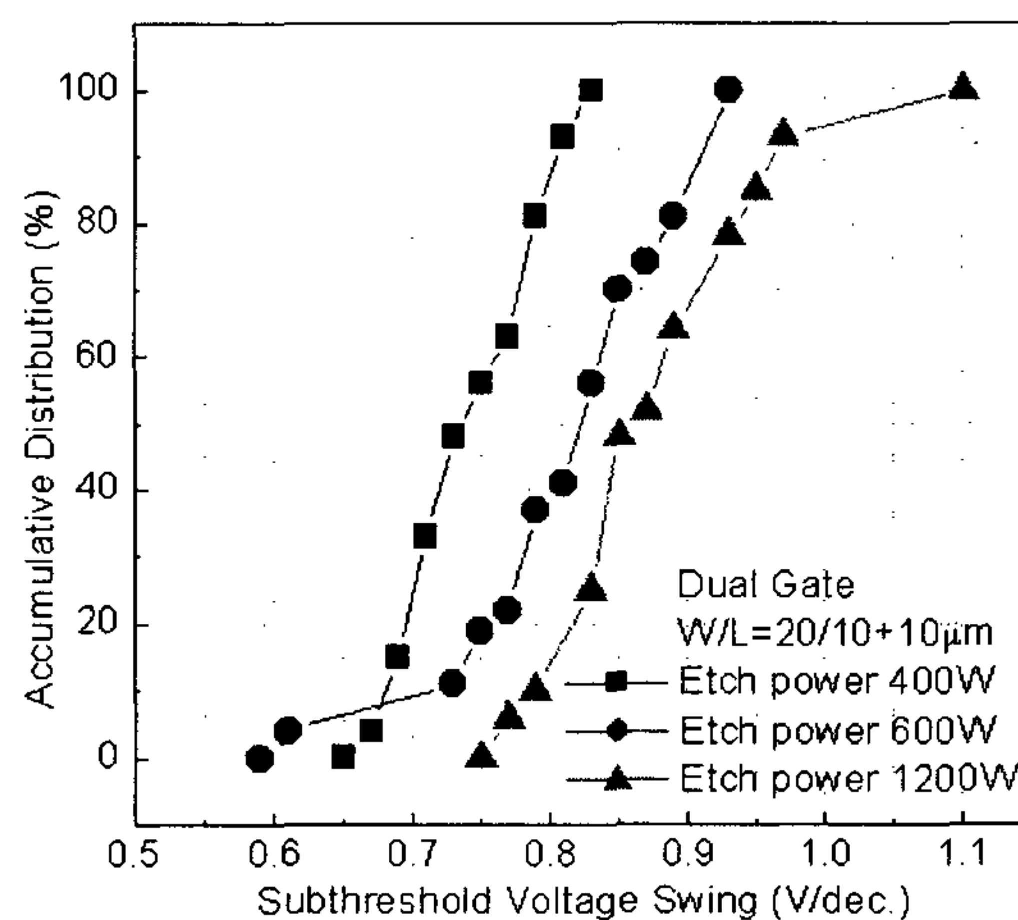


Fig. 3 Accumulative distributions of subthreshold voltage swing under various poly-Si etching RF power.



(a) Single gate structure



(b) Dual gate structure

Fig. 4 Accumulative distributions of subthreshold voltage swing under various poly-Si etching RF power of single/dual gate TFTs.

to verify the plasma process effect as Table 1 shown. After that, source and drain regions were formed by ion shower technique. Following the impurities doping and activation, the PECVD oxide interlayer was deposited. After source/drain contact holes etching and source/drain metal patterning, the devices were finished and ready for electrical measurement.

3. Results and Discussions

Figure 2 shows the dependence among threshold voltage, different channel length and various plasma RF powers on N-type and P-type TFTs. Obviously, the higher etching power was applied, the more damage was introduced in terms of threshold voltage degradation. It is believed that the seriously damaged region is the edge of channel because of ion bombardment under plasma environment.

Figure 3 plots the accumulative distributions of subthreshold voltage swing under various poly-Si etching RF power. The thick lines with solid samples indicate the subthreshold voltage swing on 20μm channel length TFTs. On the other hand, thin lines with open samples are 50μm channel length devices. It is easy to see that devices with longer channel length have worse characteristics due to larger probability to be attacked on the channel length under plasma process.

Figure 4 shows the accumulative distributions of subthreshold voltage swing under various poly-Si

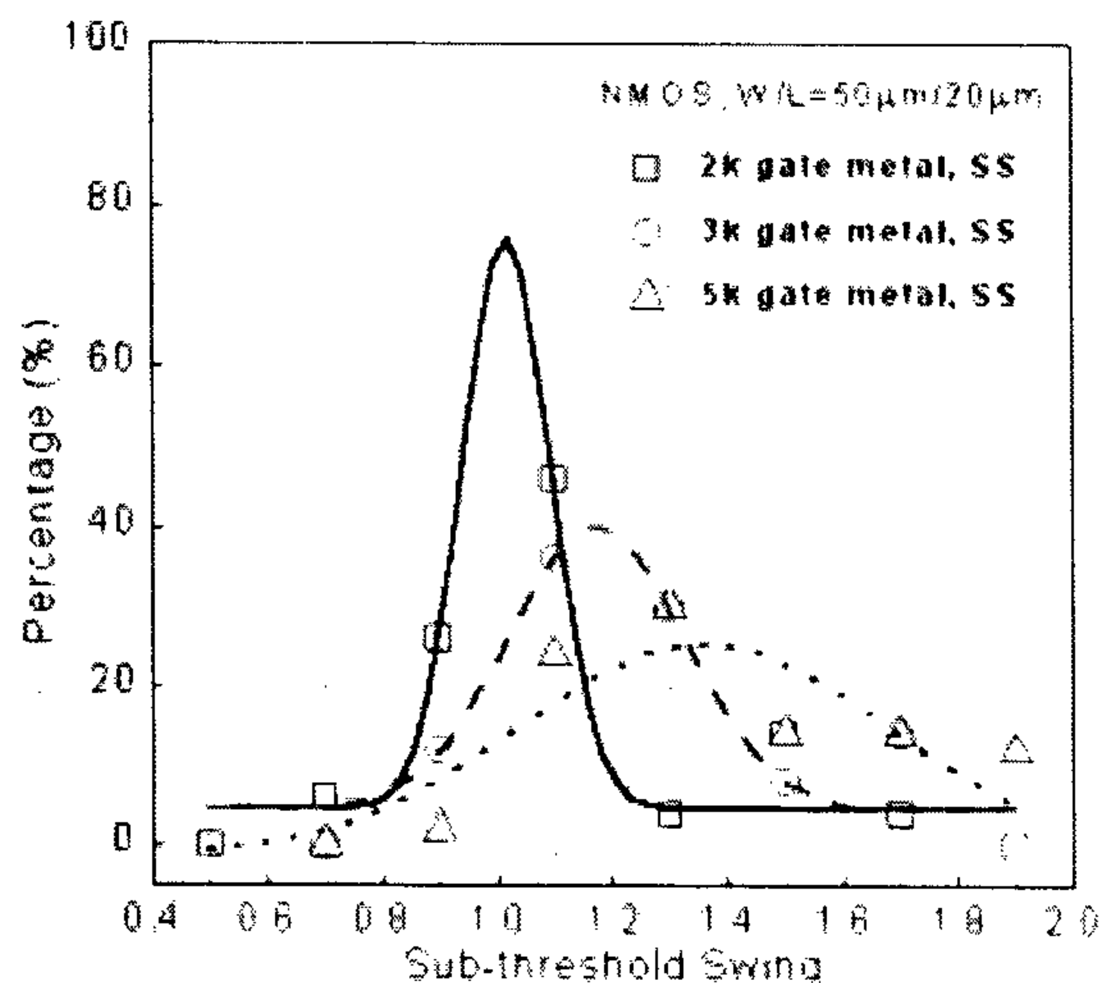


Fig. 5 Distribution of subthreshold voltage swing for various gate metal thicknesses.

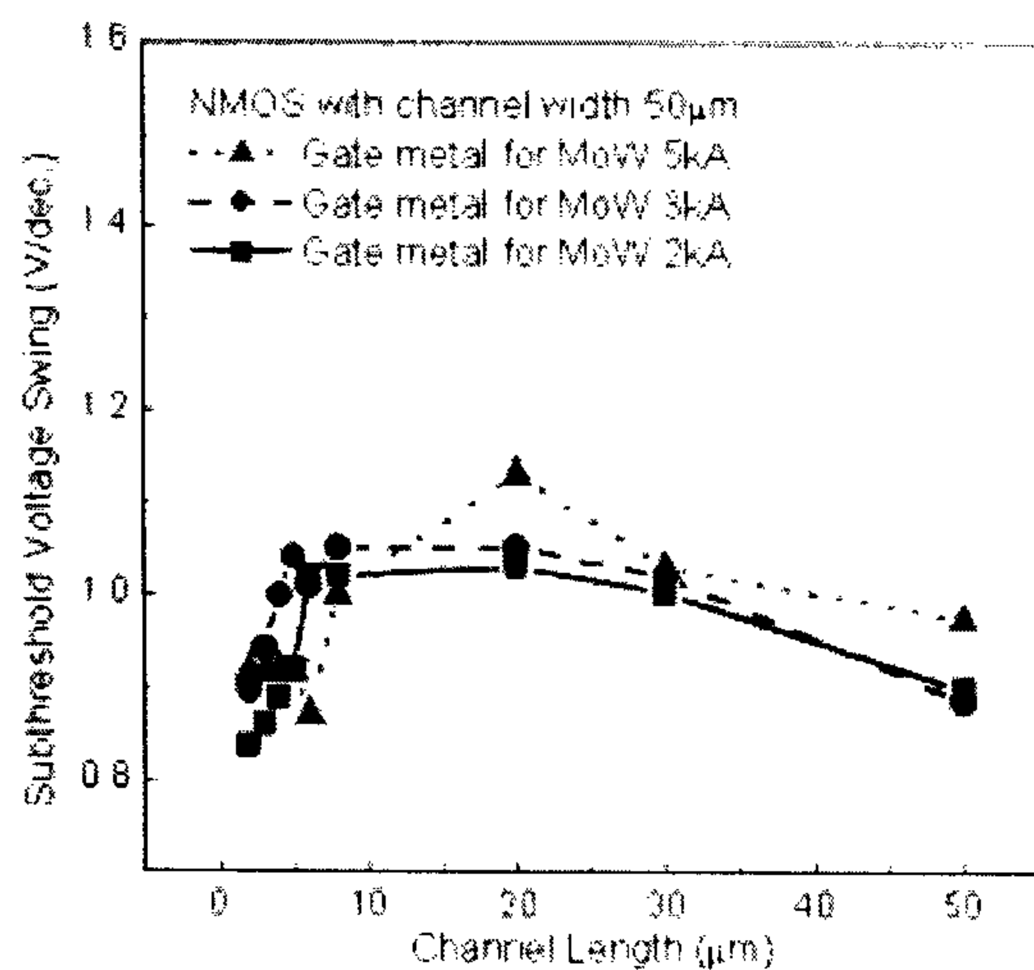


Fig. 6 Subthreshold voltage swing as a function of channel length.

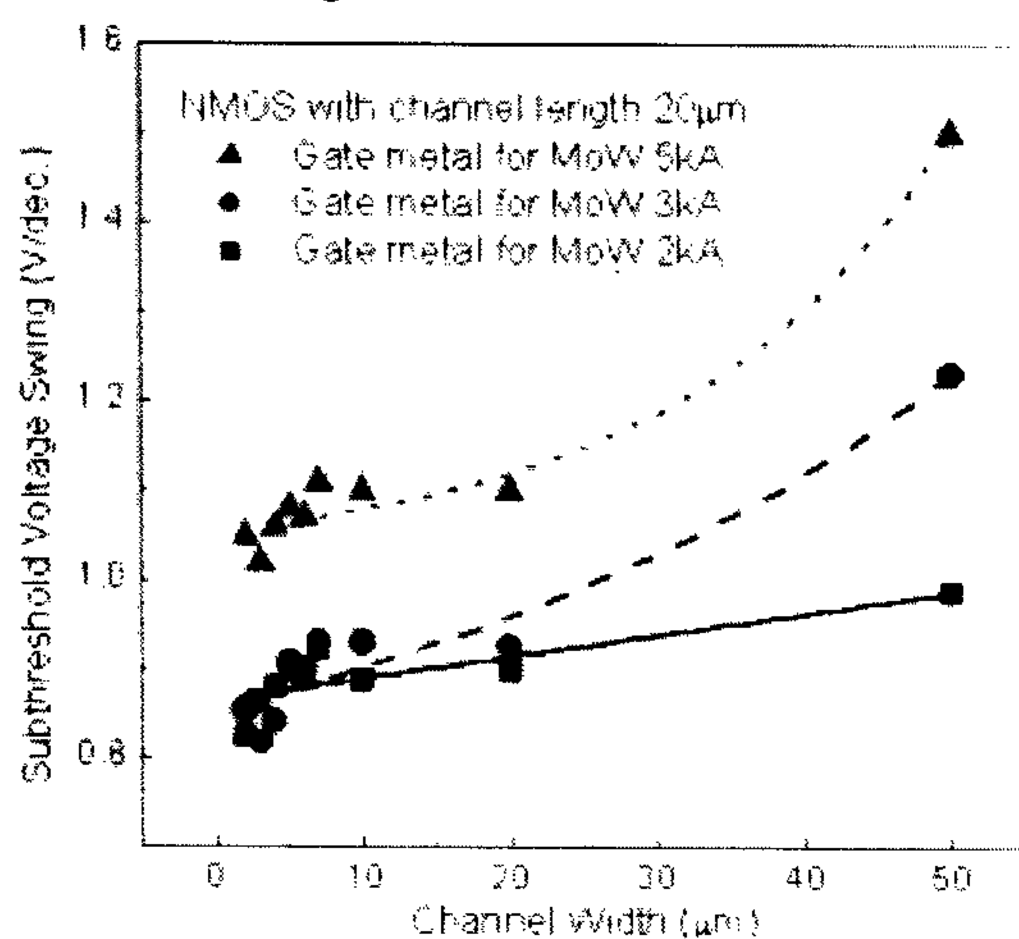


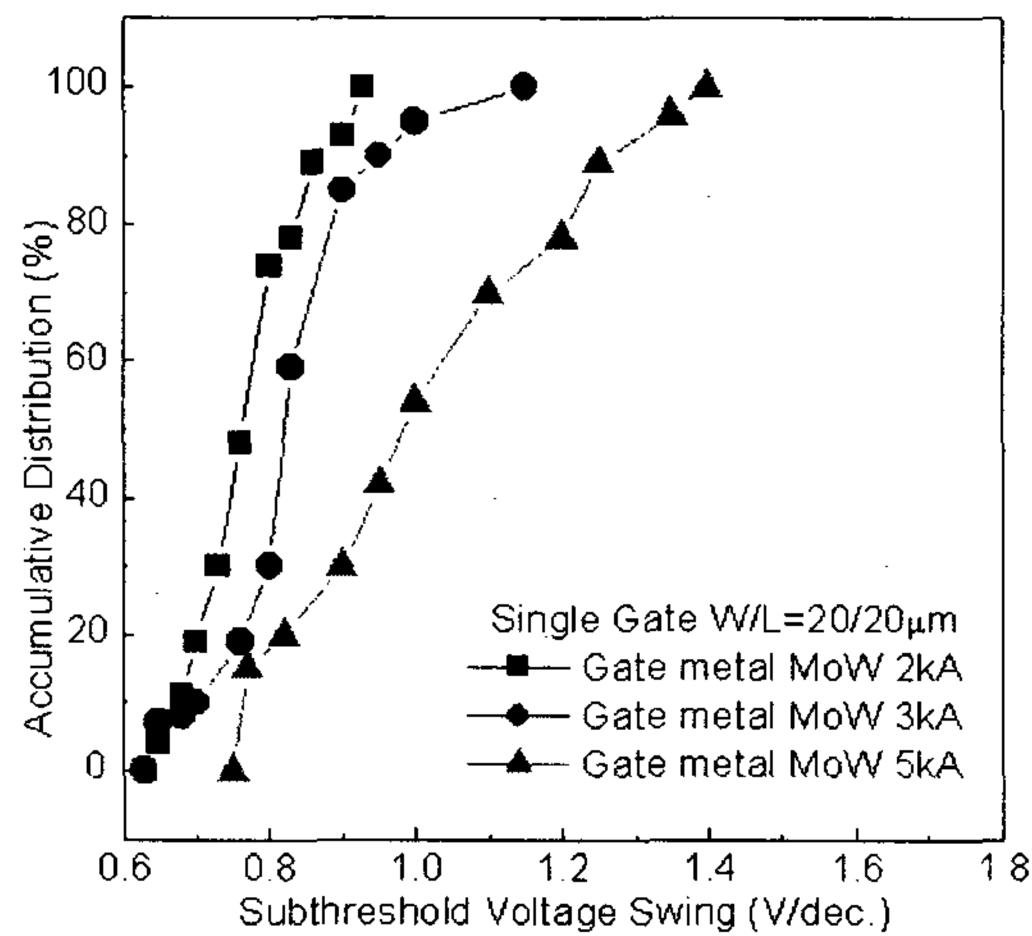
Fig. 7 Subthreshold voltage swing as a function of channel width.

etching RF power of single/dual gate TFTs. It doesn't have much affect between different gate structures. The reason is that poly-Si etching process induced damage is concluded to channel length dependant. Therefore, the dual gate structure devices have similar result as single gate devices due to equal channel length.

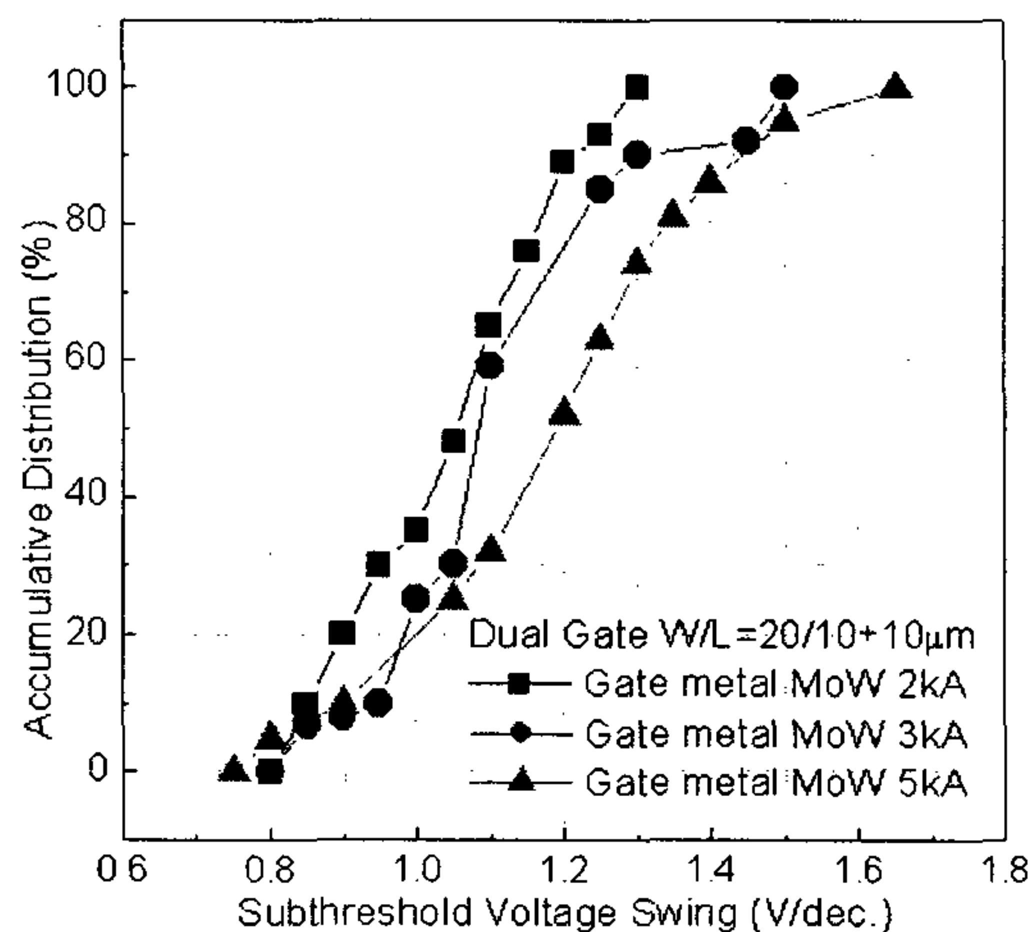
After discussing the poly-Si etching process issue, the gate metal formatting is another PPID topic. Figure 5 show the subthreshold voltage swing for different gate metal thickness devices. As the result shows, thicker gate metal with longer etching time would cause serious device degradation. Actually, it is hard to verify which kind of plasma damages would degrade the device characteristics during metal line manufacturing. So the final electrical characteristics of combined sputtering and dry etching plasma effect of MoW gate formation were investigate to reveal the final result.

Subthreshold voltage swing as a function of channel length and width are shown in Figure 6 and Figure 7. The same results of process induced damage were evidenced again. We believed that the contributing factors to this phenomenon are the damaged edge of gate oxide and damage poly-Si surface caused by ion bombardment and radiation exposure under plasma environment. Because of the mechanism of metal etching damage, it is reasonable that the curves look no affect for different channel length devices, as shown in Figure 6. In Figure 7, we can see the parallel shifting due to the thicker gate metal formation. And it shows almost no affect on three different conditions on the narrow channel width, except the parallel shift as mentioned on the first approach. But when the channel width reaches 20μm, it has a significantly increase on the subthreshold voltage swing. The results indicate that metal line formation issue is partial channel width dependant under plasma process induced damage.

Figure 8 shows the accumulative distributions of subthreshold voltage swing under different gate metal thicknesses of single/dual gate TFTs. It is quite different in comparing with poly-Si etching issue, as shown in Figure 4. Because the metal etching process induced damage is concluded to channel width dependant. The single gate devices, as shown in Figure 8(a), have better device performance than dual gate devices, as shown in Figure 8(b). The reason is that dual gate structure TFT has double channel width to be damaged than single one under plasma etching



(a) Single gate structure



(b) Dual gate structure

Fig. 8 Accumulative distributions of subthreshold voltage swing under different gate metal thicknesses of single/dual gate TFTs.

process. Therefore, the result is reasonable due to the mechanism of channel width dependent.

4. Conclusion

The evidences of PPID effect on LTPS TFTs during plasma etching process were evidenced in this paper. The process damages were both happened on poly-Si etching and gate metal etching process during TFT fabrication. The mechanism of poly-Si induced degradation is concluded to channel length dependent. On the other hand, the device degradation during metal formation is contributed to channel width dependent. The conclusion is also evidenced on both single gate and dual gate structures low temperature poly-Si TFTs.

5. Acknowledgements

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6. References

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