Reliability Aging of Oxide Integrity on Low Temperature Polycrystalline Silicon TFTs

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Abstract

In this paper, we demonstrate the impact of oxide interface-state on low temperature poly-Si TFTs. The TFTs with interface-state exhibit poor performance and serious degradation under hot carrier and gate bias stress. Our results indicate that the worse oxide integrity cause initial characteristic shift and device instability.

1. Introduction

Low temperature polycrystalline silicon (LTPS) technology has been the most promising method to manufacture high performance thin film transistors (TFTs). Compared to the conventional amorphous silicon TFTs, the benefit of LTPS was the cost reduction with integrated driver circuit on the LCD or OLED and realizes system on panel [1]. One of the major parameters to be controlled in low temperature polycrystalline silicon TFTs was the threshold voltage, but low temperature process tend to be subject to the threshold voltage shift which result in low noise immunity in driver circuit [2]. Plasma enhanced chemical vapor deposition method was most popular technique adopted in low temperature polysilicon process. The gate insulator formed by PECVD has benefits of large area deposition and low process temperature but higher leakage current and lower dielectric strength than thermal oxides grown on a single crystalline silicon wafer. The origins of threshold voltage shift have been attributed to the carrier trapping and interface-state in gate insulator [3-4]. To better understand the influence of the oxide integrity, we evaluated the hot carrier stress and gate bias degradation by using stacked insulator to enhance interface phenomenon. In this work, low temperature polysilicon thin film transistors were process with two kind of gate insulator: TEOS-base and double-layered oxide. The Electrical characteristic of oxide quality were analyzed and compared. We also discussed the reliability related to the gate oxide integrity.

2. Experimental

The top gate LDD n-channel and self-aligned p-channel transistor was fabricated on Corning 1737 glass substrate. The conventional low temperature polycrystalline silicon process-flow was adopted in this work. The buffer oxide layer and 50nm thickness a-Si:H films were deposited by plasma enhanced chemical vapor deposition. Then the polysilicon channel was formed by 308nm XeCl excimer laser crystallization. After polysilicon-island was patterned, 100nm thickness gate insulator was deposited by TEOS-base oxide and stacked gate insulator (double-layered of 10nm silane-based oxide and 90nm TEOS oxide), followed by a 410C annealing. The low resistance molybdenum-tungsten (MoW) alloy was used for the gate electrode. The source and drain regions were formed by the ion shower technique. The impurities were active at 450C thermal furnace. Finally, the interlayer oxide layer and molybdenum-tungsten inter-connection metal were deposited and patterned. The fabrication process has maximum temperatures of 450C. The cross-sectional view of gate structure on thin film transistors was shown in figure 1. It can see the interface between polysilicon and gate insulator and also the extra oxide interface created by double-layered gate insulator.

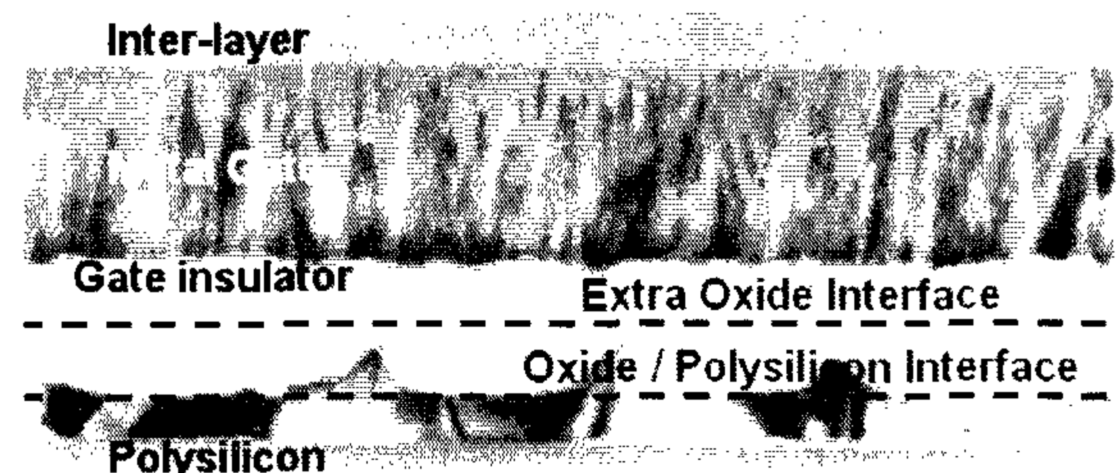

Figure 1. The cross-section view of low temperature polysilicon TFT with and without extra oxide interface.

3. Results and Discussions

The distributions of threshold voltage were shown in figure 2. The Threshold voltage at V_{ds}=0.1V was defined as the gate voltage for a drain current of (W/L)x10^{-8}A. The severe threshold voltage shift with extra interface was clear, especially in n-channel device. In n-channel device has about 3V positive shift and p-channel about 1.5V negative shift. We believed that the severe threshold voltage shift caused by carrier trapping in silane-based and TEOS insulator, which cause extra oxide interface-state.

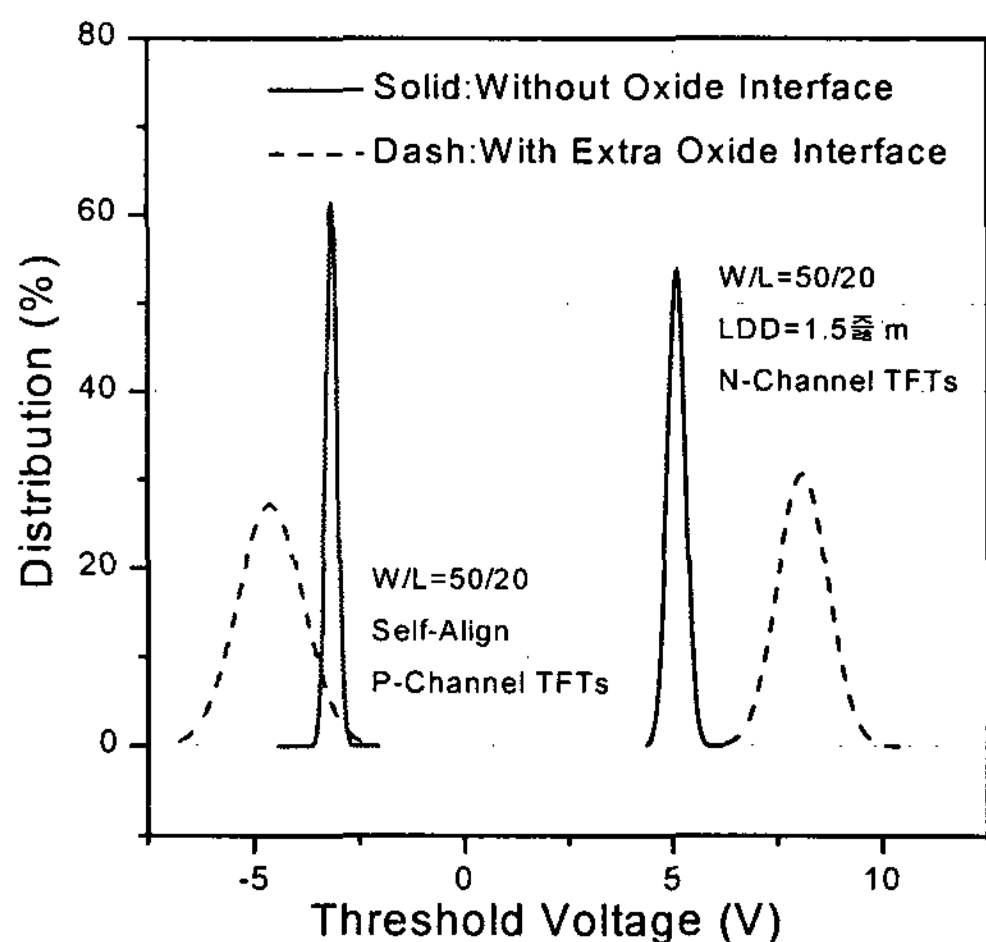

Figure 2. The distributions of threshold voltage with (Dash) and without (Solid) extra oxide interface.

Figure 3 shows the dependence of threshold voltage as function of channel length from 2 to 50□m and channel width was 50□m. The threshold voltage with extra oxide interface shows serious positive shift in n-channel thin film transistors. It can be attribute that the threshold voltage shift caused by trapping more electrons in the double-layered silane-base oxide and TEOS-base oxide interface but not conspicuous in p-channel TFTs. It can be inferred that the extra oxide interface tend to trap electrons more than holes from figure 3. The asymmetry of threshold voltage characteristic for CMOS low temperature polysilicon TFTs may cause the push-pull circuit non-balance and narrow the panel design window.

As it well knows, hot carrier effect caused carrier trapping in insulator and degrade device reliability [3]. Figure 4 shows the n-channel LDD TFTs structure with W/L=50/20□m under different hot carrier injecting condition. In order to determine the degradation of interface effect, stresses were forced in a fixed drain voltage (V_d=12, 30V) with varying gate bias (V_g=4~16V) for 100sec. A threshold voltage shift severe in the positive direction can be observed and thin film transistors with extra interface in low field injection shows more serious. In the small drain voltage, the impact ionization induced hot electrons were injected into gate insulator and trapped in oxide interface. This phenomenon not observes under high field stress which drain avalanche hot carrier (DAHC) was mainly responsible this degradation.

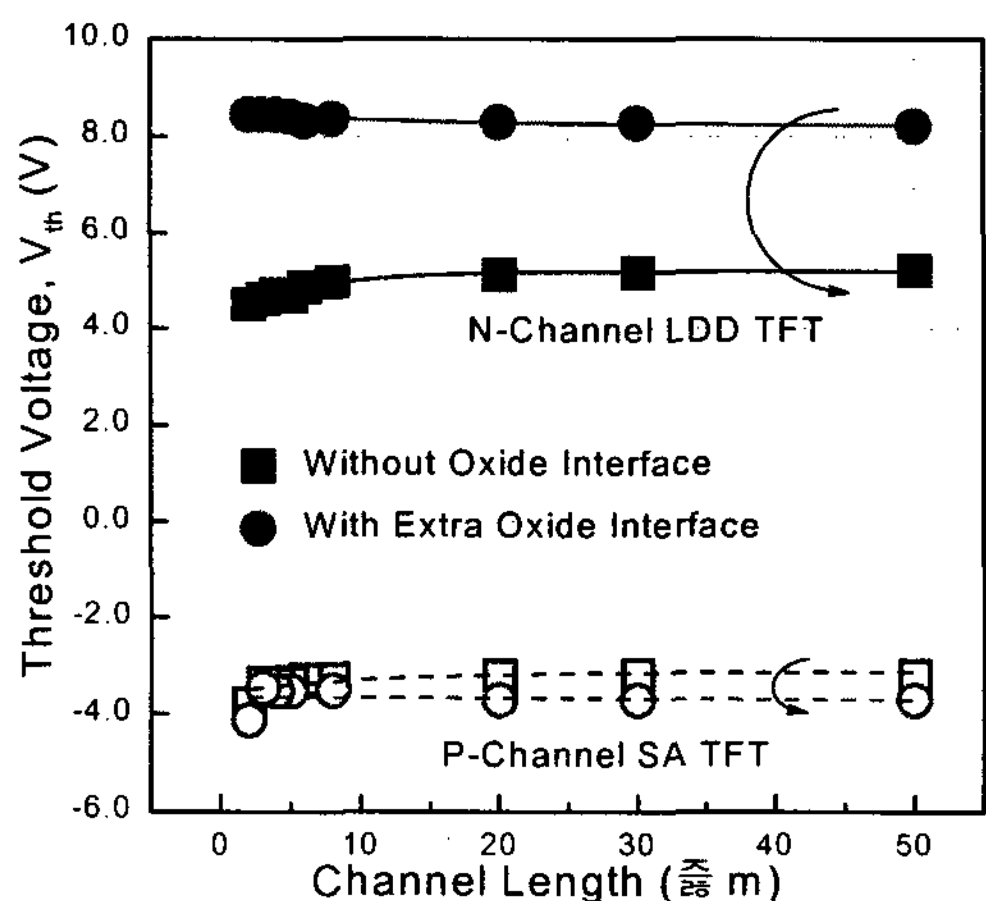

Figure 3. The relationships between threshold voltage characteristic and channel length.

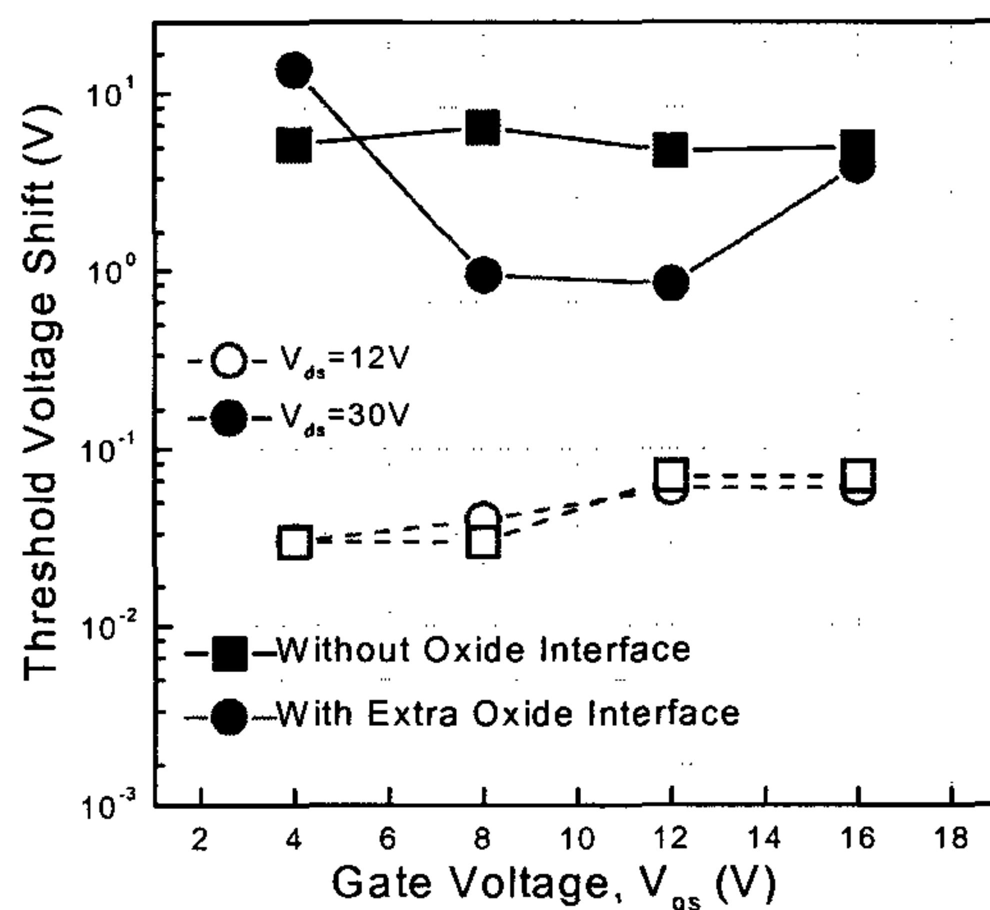

Figure 4. Dependence of threshold voltage shift under hot carrier stress (Open: V_{ds}=12 and Solid: V_{ds}=30V)

The hot carrier stress-induced degradation characteristics of n-channel LDD TFTs were illustrated in figure 5. It was shows that time dependence of the threshold voltage shift with and without extra interface under hot carrier stress (V_{ds} =12V and V_{gs} =4~16V). It was clear that with oxide interface device has severe threshold voltage degradation. As the gate stress voltage increasing, the aging characteristics were more observed. The more threshold voltage shift with increasing V_{gs} as shown in figure 5 suggest less stability with extra interface-state at higher current density. During hot carrier stress condition a power time-dependent law was observed and without extra interface was about 0.335 and with extra interface was about 0.461 [4,6]. We believed that device with extra oxide interface has more generated and trapped in the oxide interface-states and dominate the aging mechanism. Moreover, the slope of aging with and without oxide interface device has a big gap, which means that extra interface exit a fix amount of trapping state. As operating in hot carrier condition, carrier injecting format close drain junction and damage gate insulator [5]. We believed that thin film transistors with oxide interface were more sensate to channel hot carrier effect (CHE).

Figure 6 shows the lifetime versus the inverse supply voltage for n-channel thin film transistors under hot carrier operating (V_d=V_g). The lifetime was defined as the time required for a degradation of □ $G_{m,max}/G_m$ was 10% [6]. From figure 6 clearly shows that the low temperature polysilicon thin film transistors device with extra oxide interface has fewer lifetimes. It can be estimates that the less interface-state density, the more life cycles in device operating. In order to improve panel lifetime, keep gate insulator from interface-state can boost up the performance.

The gate bias-induced degradation characteristics of n- and p-channel thin film transistors were illustrated in figure 7 and figure 8. It was shows that the time dependence of threshold voltage shift under gate bias stress (V_g= □ 30V). Form figure 7 was clearly showed that threshold voltage of n-channel device with extra interface in positive bias condition has large negative degradation. Those were due to large amount of positive charge trapping in double-layered insulator, which created extra oxide interface-state [7]. In fact, because of problems such as plasma deposition damage and interface cleaning issue, the double-layered insulator device suffers from severe degradation and instability.

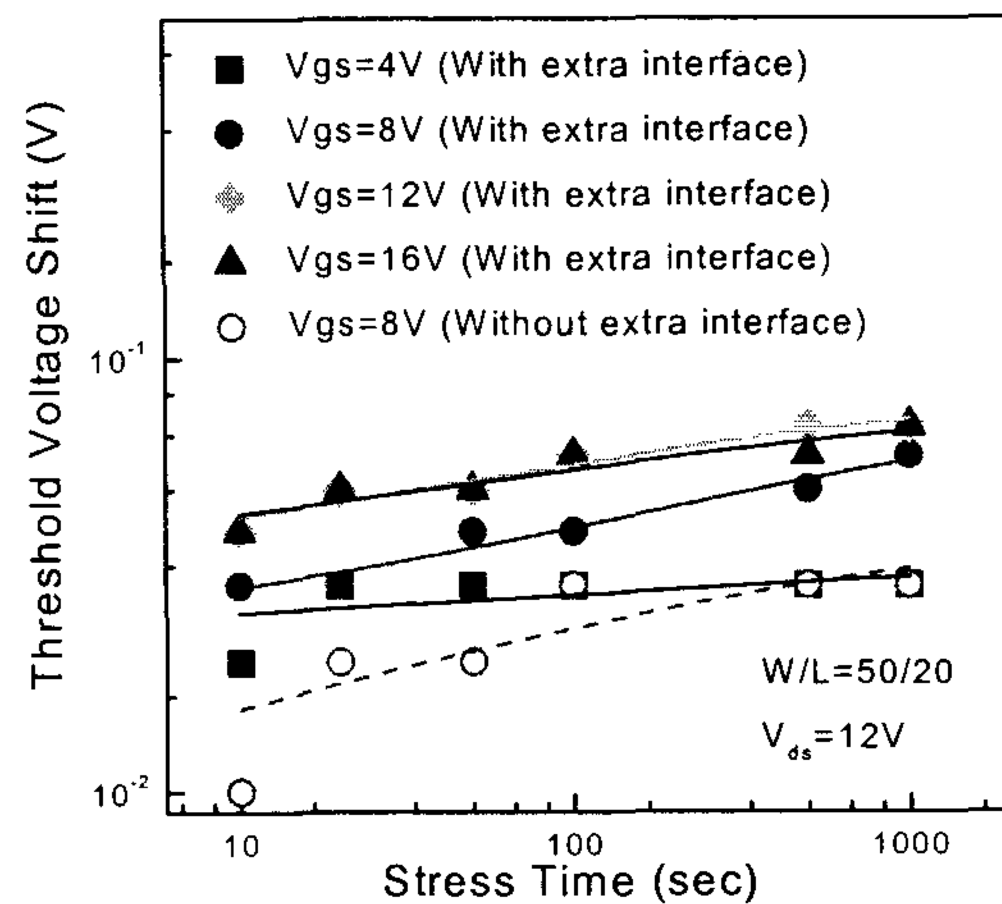

Figure 5. A comparison V_{th} shift with (Solid symbol) and without (Open symbol) oxide interface in hot carrier stress.

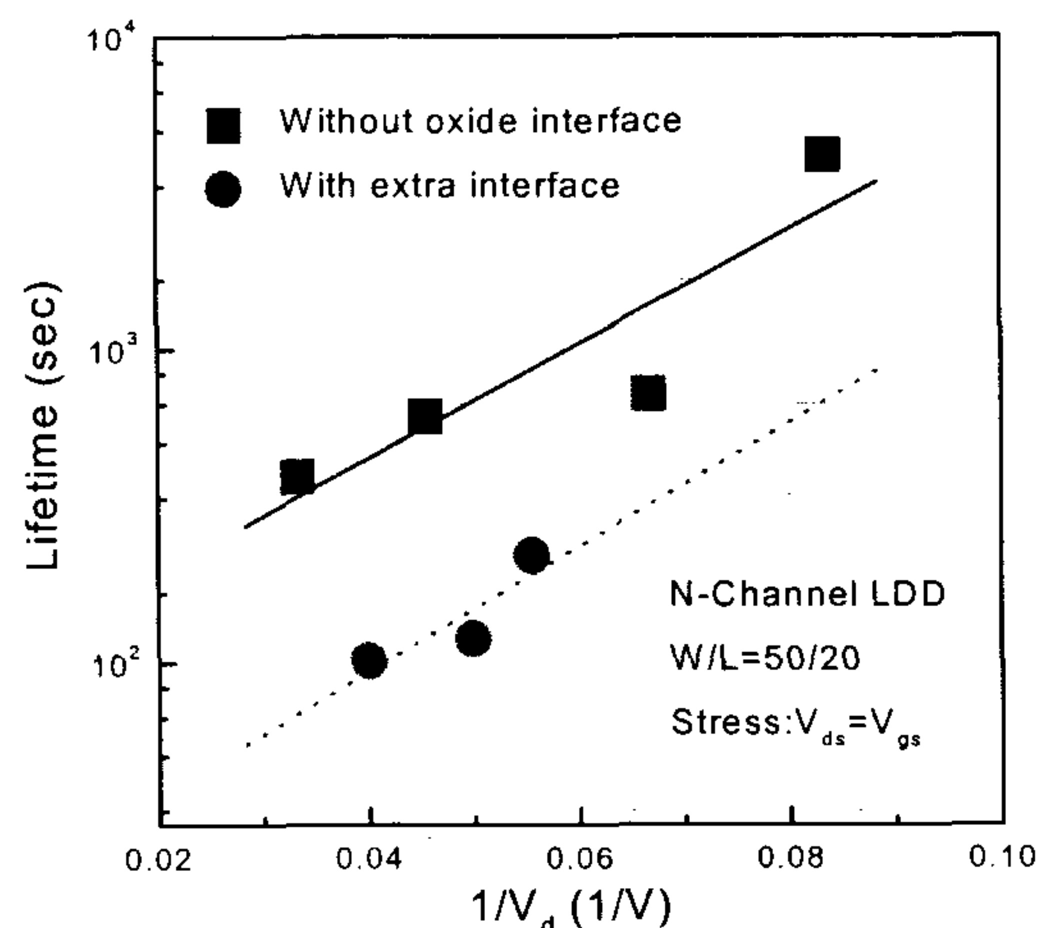

Figure 6. Lifetime versus $1/V_{ds}$ with and without extra oxide interface in hot carrier stress (V_{ds}=V_{gs}).

Figure 8 shows the positive and negative gate bias stress in threshold voltage of p-channel TFTs. It was clear that the threshold voltage shifts for negative bias were large than those for positives stress. This indicates that the dominant mechanism was hole trapping in gate insulator rather than electron trapping. It was also ruled out the degradation were much more readily associated with extra interface effect both in n- and p-channel thin film transistors. Thus, we believe that the improved stability of low

temperature polysilicon thin film transistors was attributed to reduce the interface and trapping-state in gate insulator.

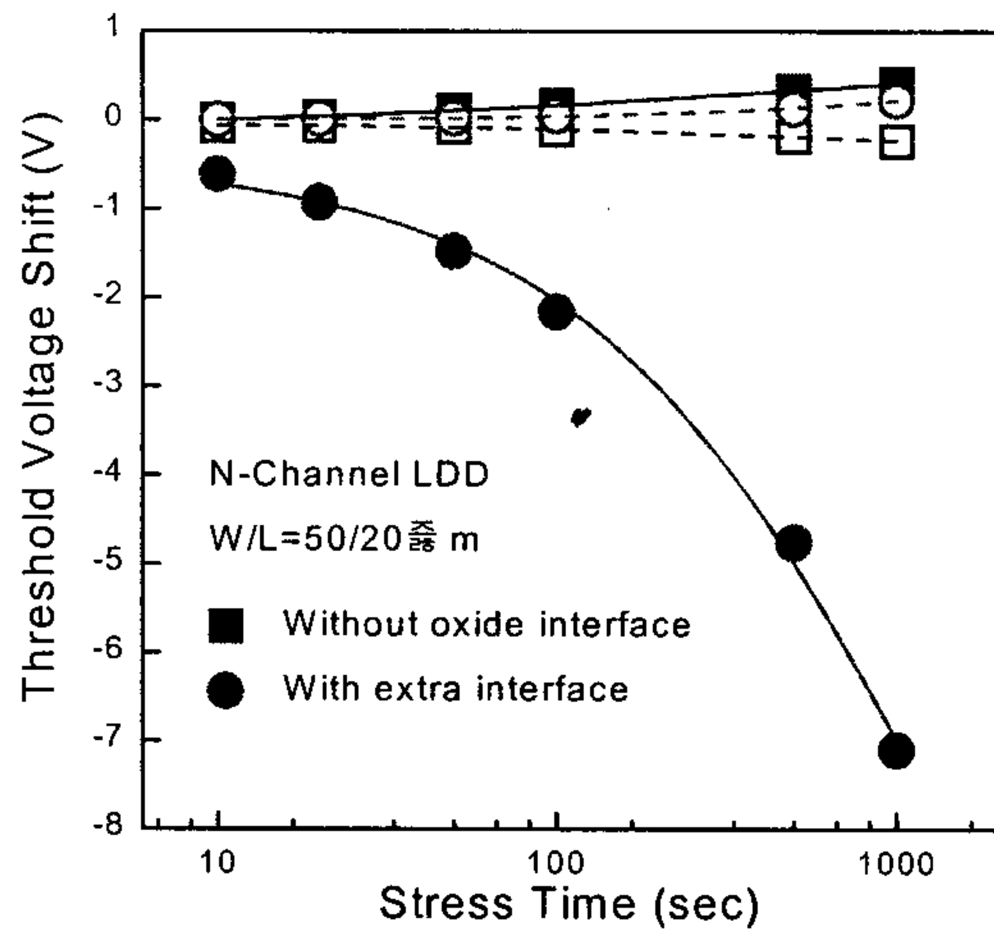

Figure 7. Variation of threshold voltage shift in n-channel TFTs by gate bias stress as function of time (Solid symbol: V_g =+30V and Open symbol: V_g=-30V).

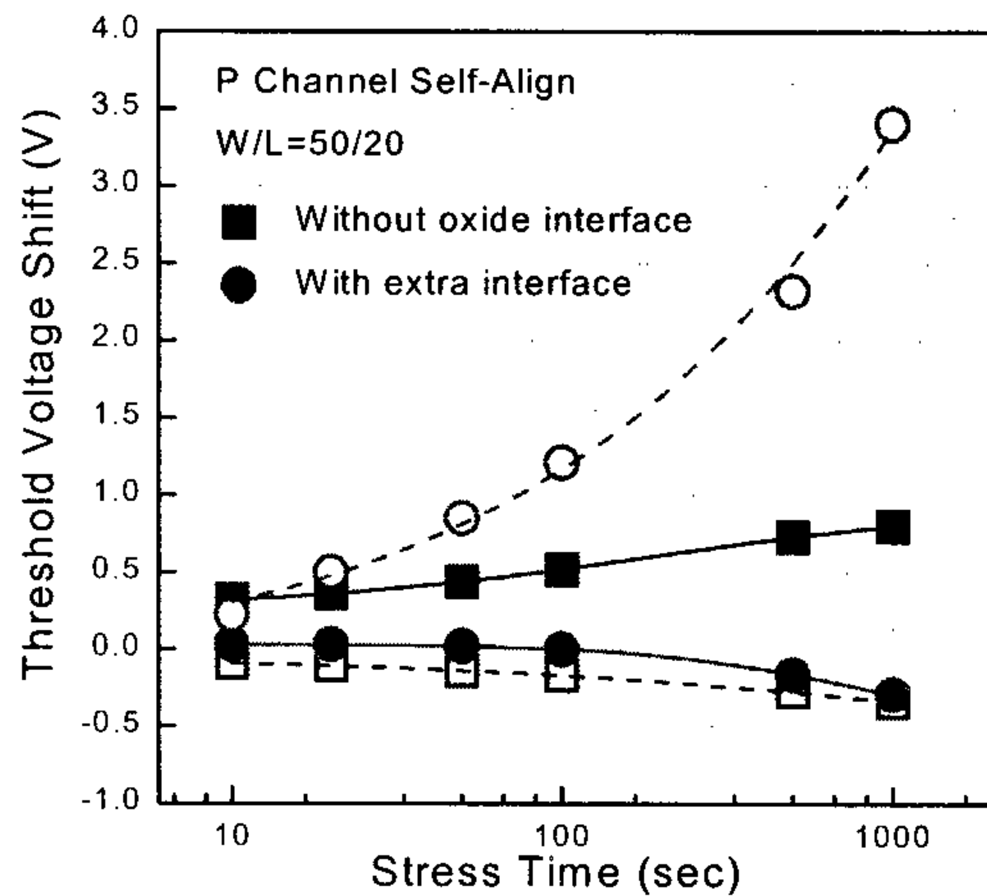

Figure 8. Variation of threshold voltage shift in p-channel TFTs by gate bias stress as function of time (Solid symbol: V_g =+30V and Open symbol: V_g=-30V).

4. Conclusion

In summary, we have investigated the effect of oxide interface induced degradation on low temperature polysilicon thin film transistors. The relationship between the oxide integrity and threshold voltage shift was observed. The degradation phenomena caused by hot carrier injecting and gate bias stress has been evaluated by using extra oxide interface method. We also found that the worse oxide integrity cause initial characteristic shift and device instability.

5. Acknowledgements

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6. References

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