Development of New COG Technique Using Eutectic Bi-Sn and In-Ag Solder Bumps for Flat Panel Display

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Abstract

We have developed a new COG technique using flip chip solder joining technology for excellent resolution and high quality LCD panels. Using the eutectic Bi-Sn and the eutectic In-Ag solder bumps of 50-80 μm pitch sizes, a ultrafine interconnection between IC and glass substrate was successfully made at or below 160 ℃. The contact resistance and reliability of Bi-Sn solder joint showed the superiority over the conventional ACF bonding.

1. Introduction

The trend in LCD driver IC packaging has been to move the driver IC closer to the LCD itself. The chip on glass (COG) technique is currently being used in a number of products such as high pixel density and small area LCD's. Many kinds of COG bonding techniques have been developed: Au bump bonding using anisotropic conductive adhesive (ACA) or anisotropic conductive film (ACF), and stud bump bonding using isotropic conductive adhesive[1-3]. However, COG technique using ACF have been only applied in high volume applications. Generally, the COG technique using conventional ACF has high contact resistance on the order of hundred milliohms[4-5]. For high-definition LCD's, contact resistance will increase due to the decrease of the pitch size and the contact pad size. The high contact resistance of the COG technique using ACF bonding may be a serious problem in the field of ulatrafine pitch packaging below 45 μm which will be used in near future. The COG technique using conventional ACF also requires more precise alignment for chip bonding and uniformity of bump height.

For fine pitch packaging in high resolution LCDs, we developed a new COG technique using the flip chip solder joining technology. The COG technique using flip chip solder joining technology has the several advantages compared with the COG technique using the ACF[6];

(1) It is easy to be used in ultra-fine pitch applications due to the self-alignment of liquid solder during the relfow process.

(2) The solder bumps form metallurgical bonding with metal pads, whereas the ACFs form mechanical contacts at the substrate surface. So, flip chip solder joining technology has lower contact resistance than ACF bonding.

(3) The bonding pressure of solder bumped flip chip bonding is lower than that of ACF bonding. An excessive pressure on bumps can cause the cracks in glass.

(4) The rework process is easy by raising the temperature above the melting temperature of solder.

(5) It can lower the material cost because it is possible to eliminate the expensive ACF.

Even though flip chip solder bumped technology has many advantages, the conventional flip chip solder joining technology which commonly used solders such as eutectic Pb-Sn and Pb-5Sn has not been used in LCD driver IC packaging. It requires the high temperature more than 200℃ during solder reflow process. These solders cannot be applied to LCD since the high temperature processing degrades the liquid crystal or the color filter in LCD module. Therefore, the low temperature solders which can be processed below 160℃ should be developed for this application.

We selected eutectic Bi-Sn (mp: 138℃) and eutectic In-Ag (mp: 143℃) solders, developed the COG process using solder joints which can be applicable for fine pitch packaging of driver IC in LCDs, and evaluated the contact resistance of ultrafine solder joint.

2. Experimental

Au/Cu/Cr or Au/Ni/Ti thin films were deposited for under bump metallurgy (UBM) on Si wafers using DC magnetron sputtering system without breaking the vacuum of the chamber. The octagonal shaped UBMs with the pitches of 50 μm or 80 μm were fabricated

through the photolithographic process and the wet chemical etching.

The thick photoresist (PR) was used as the solder mask. The solder mask was fabricated through two-step spin coating to acquire the adequate height. Solders were evaporated on UBMs and solder bumps were formed by the lift-off process. Reflow process was performed in N_2 using RTA system. The heating rate was 90℃/min and the peak temperature were 150℃ or 160℃. The holding times at peak temperature were 4 min or 9 min.

The solder bumps in a chip were aligned to the corresponding metal pads in a glass substrate using a flip chip bonder and all solder joints were made simultaneously during the reflow process at 160℃. The epoxy resin for underfill required a post cure of 5 minutes at 160℃. The basic procedure for fabricating the low temperature solder joints is shown in Fig. 1.

For the electrical test of solder joint, Ti(0.1 ㎛)/Au(0.1 ㎛)/Cu(3 ㎛)/Ti(0.05 ㎛) or Ti(0.1 ㎛)/Au(0.1 ㎛)/Ni(0.5 ㎛)/Cu(3 ㎛)/Ti(0.05 ㎛) metal films were deposited for interconnection of the daisy chains on SiO_2/Si wafer. The UBMs were fabricated through opening terminal vias by the wet chemical etching of Ti top layer. Similarly, metal pads and conductor lines were formed on the glass substrate in order to join the chip. The electrical assessment was done using four-point technique to address the contact resistance of the daisy chain running through the chip and the glass substrate. One daisy chain has maximum 112 transitions. The contact resistance (R_c) was measured using Bi-Sn solder joints of 80 ㎛ pitches. The average R_cs were obtained from at least 4 specimens. For the reliability test, the specimens were stored in 85℃/85% RH high humidity and temperature condition up to 500 hours.

3. Results and discussion

3-1. Solder bump formation & flip chip bonding

Figure 2 is SEM images showing the thick PR solder mask and the as-deposited solder bumps. The solder mask through conventional process showed the inverse-trapezoid vias, shown in Fig. 2-(a). Using the conventional solder mask, the solders can be deposited at the wall of vias due to the inverse-trapezoid vias and the irregular solder particles were observed at the edge of solder bumps (Fig. 2-(c)). After reflow process, the irregular bump formation raised the problems of the large variation of solder sizes and heights. Therefore, we modified the solder mask formation process in following sequence: first spin coating, blank exposure without E-beam mask, second spin coating, and exposure. The overhang structural solder mask was fabricated through modified process (Fig. 2-(b)). In the case of overhang structural solder mask, the clean solder bumps were formed, shown in Fig. 2-(d). The overhang-structural solder mask is the key factor of the successful lift-off because the overhang structure helps the perfect strip of the solder mask after solder deposition.

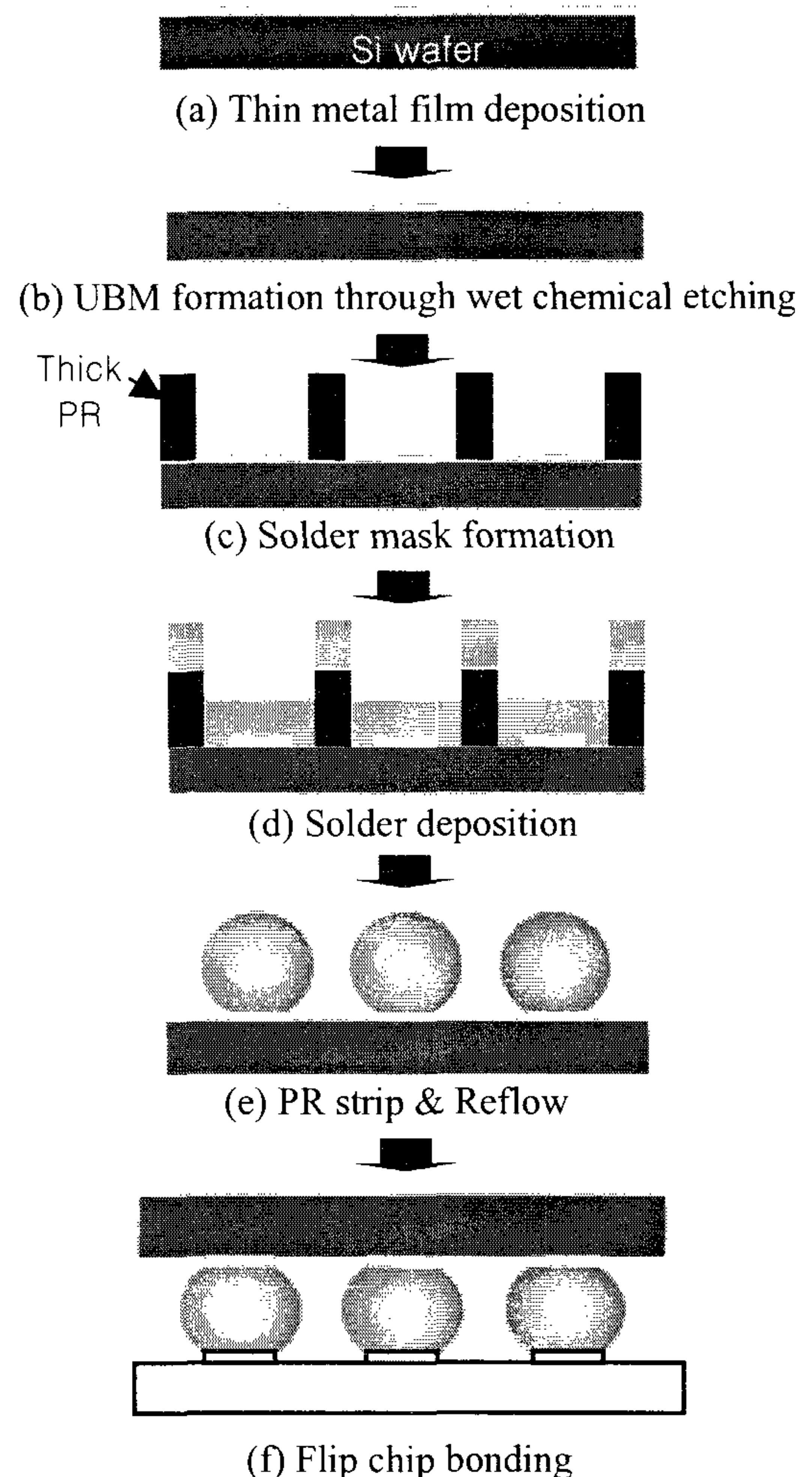

Figure 1. Schematic diagram showing the flip chip bonding process.

Figure 3 is the SEM images showing the eutectic Bi-Sn solder arrays which are reflowed at 160℃ for 9 min and solidified at the high cooling rate. Controlling the microstructure of solder bumps can form uniform, smooth, and spherical solder bumps during reflow process[7]. As shown in Fig. 3-(a), the height and the diameter of solder bumps, which were controlled by

the volume of as-deposited solders, were about 40 μm and 46 μm, respectively. In the case of 50 μm pitch solder bumps, the height and diameter of solder bumps were about 24 μm and 27 μm. It is believed that ultrafine interconnection below 50 μm pitches can be easily formed using this technique due to the surface tension of liquid solder.

The test chips were mounted on the glass substrates using the joining reflow at 160℃. Figure 4 is cross-sectional micrographs of the 50 μm pitch In-Ag solder joints assembled at 160℃. Si chip and glass substrate were successfully joined through solder bumps.

3-2. Contact resistance measurement

Table I shows the average contact resistances (R_cs) of Bi-Sn solder joints with Au/Cu/Ti and Au/Ni/Cu/Ti metal pads of the glass substrate. These values included the contact resistance of solder joints and the resistance of conductor lines on chip and glass substrate. As can be seen from Table I, the R_cs of Bi-Sn solder joints with Au/Cu/Ti and Au/Ni/Cu/Ti metal pads of glass substrate were 18.6 m and 34.6 m , respectively. Even though the R_cs include the resistances of conductor lines, these values are much lower than the contact resistance in the conventional ACF bonding which is the order of hundred milliohms[4,5]. If the resistances of conductor lines on chip and substrate were calculated and removed from the R_cs presented in Table 1, the real contact resistances of Bi-Sn solder joints with Au/Cu/Ti and Au/Ni/Cu/Ti metal pads were 8.1 m and 12.0 m . This indicates that the resistance of Au/Ni/Cu/Ti metallization is larger than that of Au/Cu/Ti metallization and the real contact resistances of Bi-Sn solder joints are almost same in both specimens.

Table II shows the R_cs of Bi-Sn solder joints before and after underfill process. The solder joints were additionally reflowed at 160℃ for 5 minutes during underfill process because the epoxy resin for underfill required a curing. After the underfill process, the R_c of Bi-Sn solder joint remained within the error range from initial value. This value is also much lower than the contact resistance of conventional ACF bonding. These results are interpreted in terms of bonding characteristics and bonding area between ACF bonding and soldering. The interconnection using ACF is mechanically and partially contacted through conductive particles between Au bump of driver IC and ITO pad of LCD panel. On the other hand, the interconnection using solder bump is metallurgical bonding in a whole area between UBM of driver IC and metal pad of LCD panel.

The R_cs of the Bi-Sn solder joints without or with underfill process were measured during 85℃/85% relative humidity condition up to 500 hours. The results are shown in Fig. 5. The R_c of the Bi-Sn solder joint without underfill increased twice as large as the initial value after 500 hours. This value is still lower than the contact resistance of conventional ACF bonding. On the other hand, the R_c of the Bi-Sn solder joint with underfill was almost the same even after 500 hours. The comparison of reliability results between Bi-Sn solder joint without underfill and solder joint with underfill reveals that the increase of contact resistance is mainly due to the humidity attack on the solder surface and the conductor lines. It is found that the epoxy resin for underfill protects solder joint from the humidity and improves the reliability of solder joint. The results of hot humidity test indicate that the COG technique using eutectic Bi-Sn solder bumps has excellent reliability.

4. Conclusion

Using Bi-Sn and In-Ag solder materials, we developed the COG technique of 50 μm pitch at the temperature below 160℃. The overhang-structural solder mask was effective for perfect lift-off. The spherical-shaped solder joints having minimum 50 μm pitches were successfully connected through the metallized pads between Si and glass substrate. The contact resistance of Bi-Sn solder joint containing the resistance of conductor line was 19 m and the contact resistance excluding conductor line was calculated as low as 8 m . This value was much lower than the contact resistance of the conventional ACF bonding. The COG technique using eutectic Bi-Sn solder joints with underfill had excellent reliability at a hot humid environment in the electrical aspect. In conclusions, the COG technique using low temperature solder bumps has several advantages to the COG technique using ACF in the field of ultrafine pitch LCD driver IC packaging. The COG technique using low temperature solder bumps can be applied to the advanced LCDs to require higher quality, better resolution and lower power consumption.

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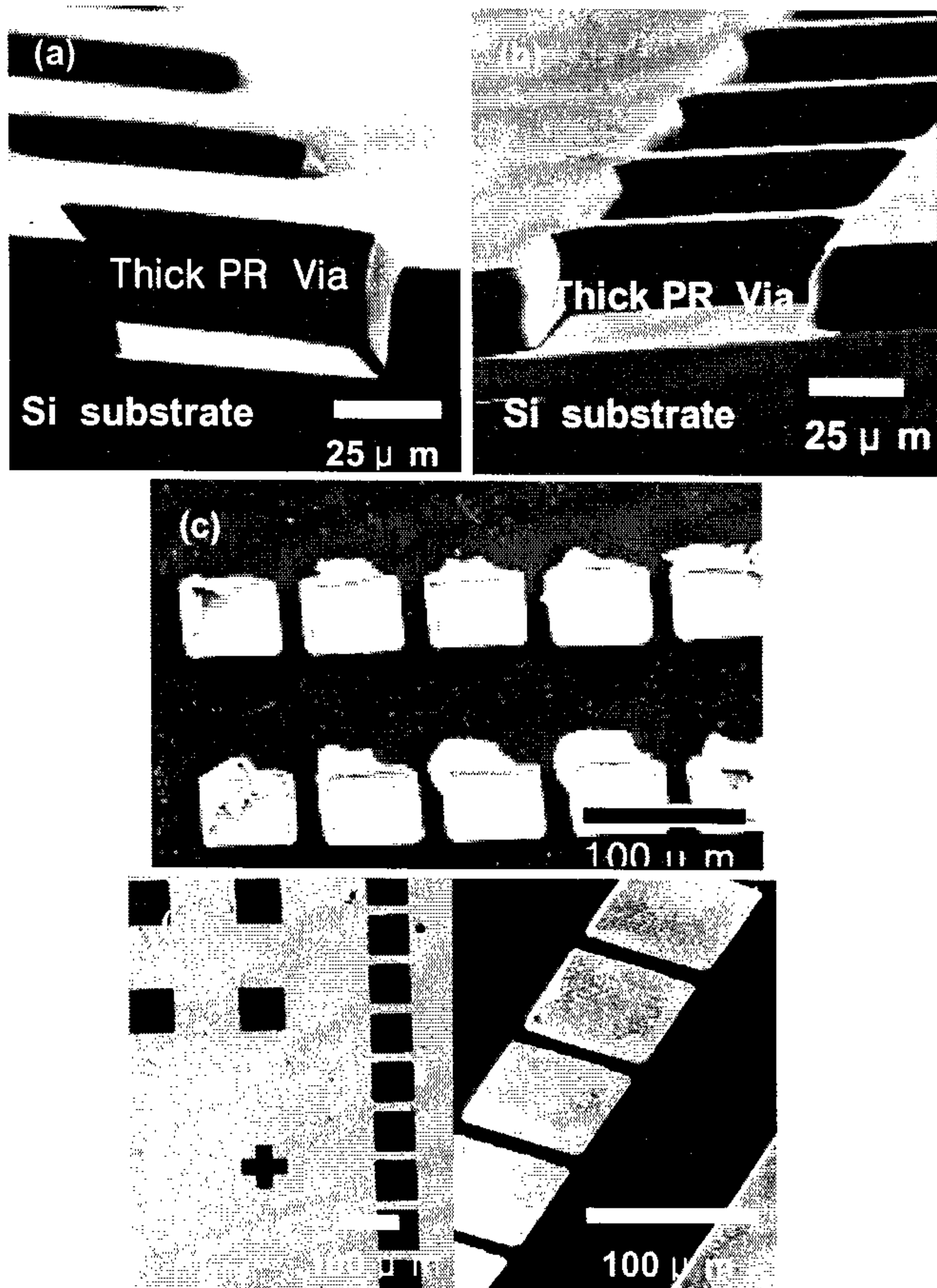

Figure 2. SEM images of (a) solder vias in conventional mask, (b) overhang-structural solder vias in modified mask, (c) as-deposited solder bumps using conventional solder mask, and (d) as-deposited solder bumps using overhang structural solder mask.

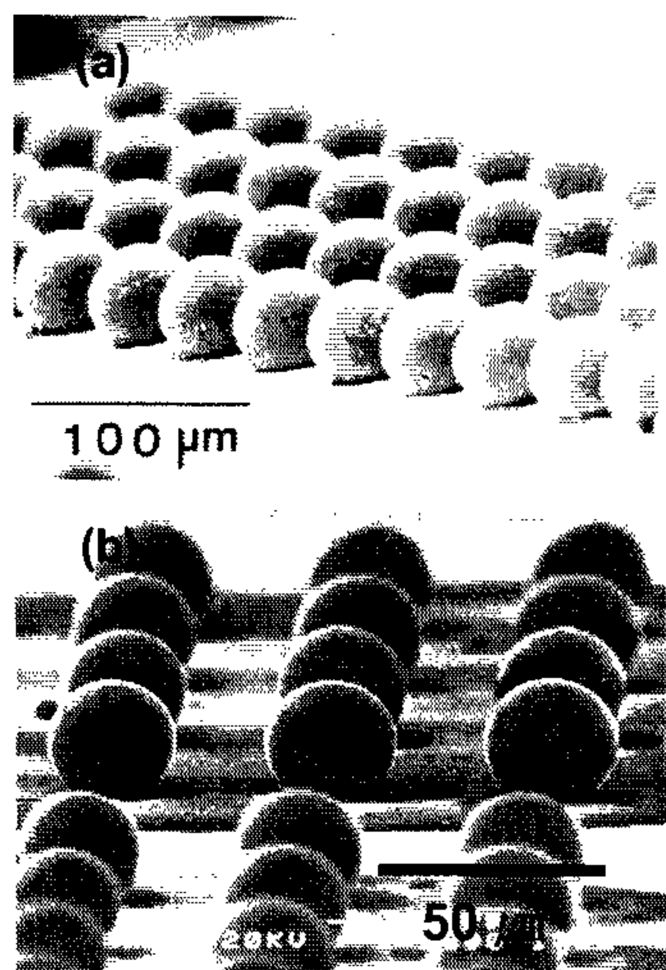

Figure 3. SEM images of eutectic Bi-Sn solder bump arrays having (a) 80 μm and (b) 50 μm pitches.

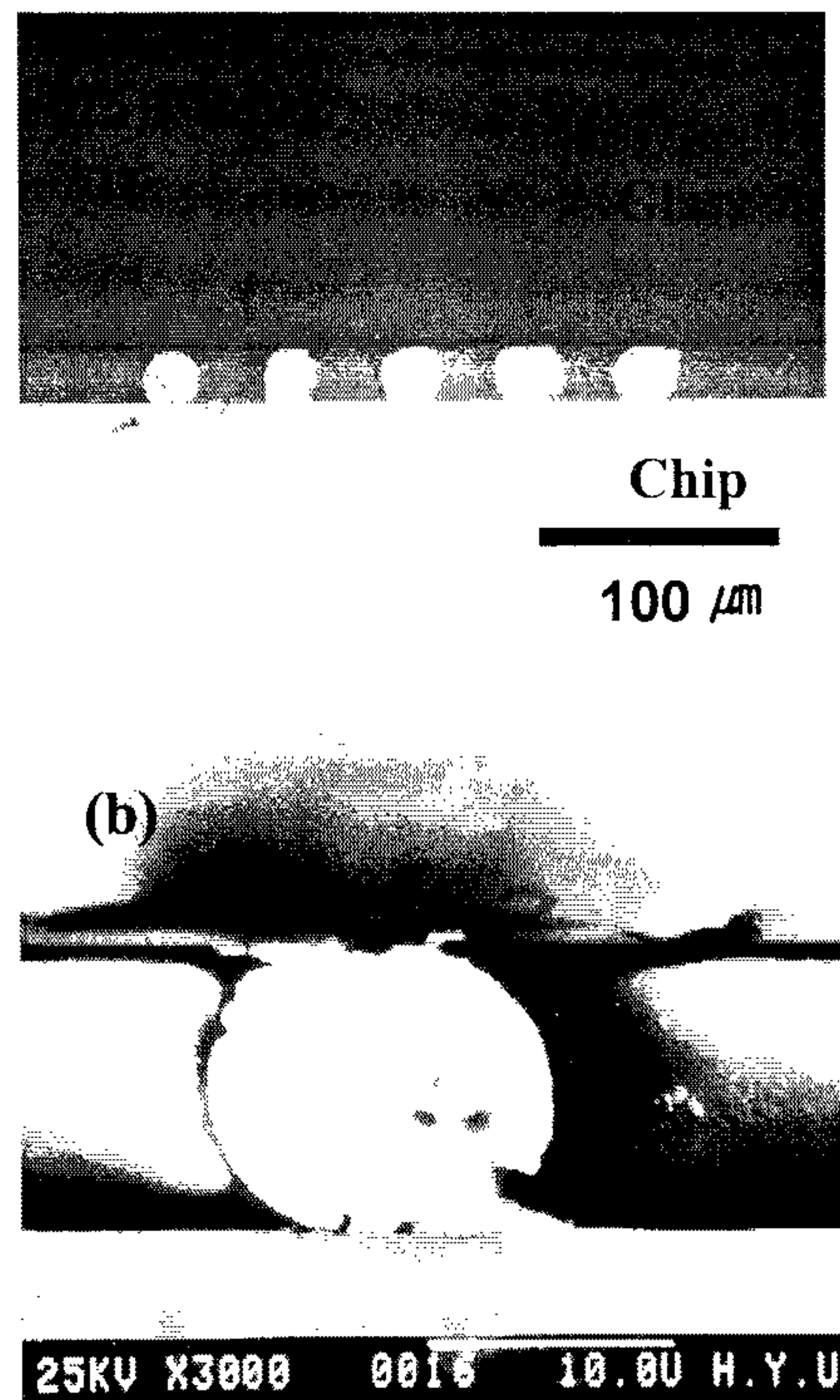

Figure 4. (a) Optical image showing the solder joints of 50 μm pitches and (b) SEM image showing the solder joint of 50 μm pitches.

Table I. Contact resistances of Bi-Sn solder joints before underfill process.

Glass Metallization	R_c (m)	Standard deviation
Au/Cu/Ti	18.6	3.0
Au/Ni/Cu/Ti	34.6	6.3

Table II. Contact resistances of Bi-Sn solder joints before and after underfill process.

Glass metallization	Underfill	R_c (m)	Standard deviation
Au/Cu/Ti	X	19.5	4.1
	O	23.4	6.7

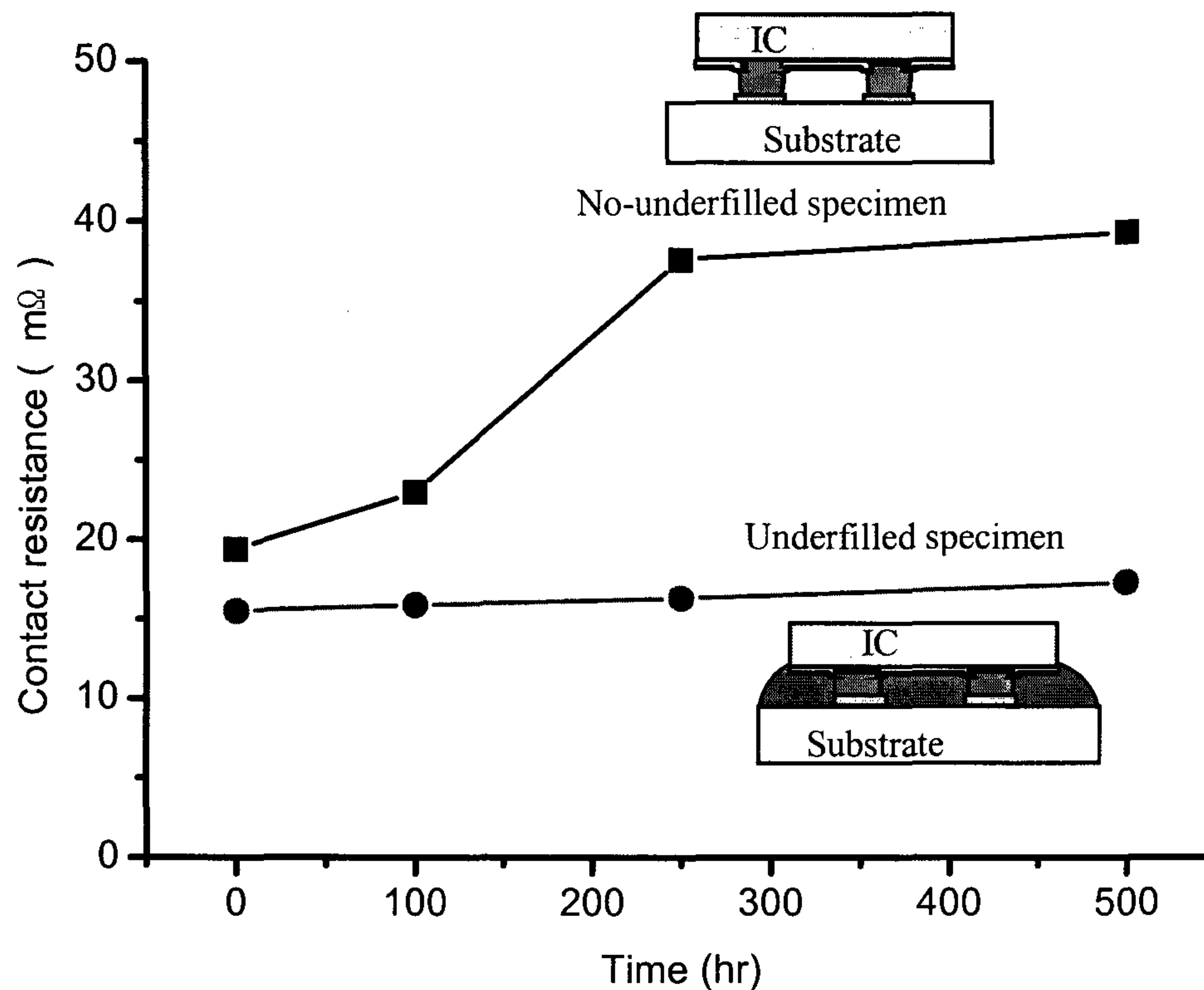

Figure 5. Contact resistances of Bi-Sn solder joint without and with underfill after storage at 85℃/85% RH condition.

6. References

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