Silicon Thin-film Transistors on Flexible Foil Substrates

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Abstract

We are standing at the beginning of the industrialization of flexible thin-film transistor backplanes. An important group of candidates is based on silicon thin films made on metal or plastic foils. The main features of amorphous, nanocrystalline and microcrystalline silicon films for TFTs are summarized, and their compatibility with foil substrate materials is discussed.

1. Introduction

Flexible displays are attractive because flexibility implies light weight and ruggedness. These are desirable features for portable electronics today, and even more so for large-area and wallpaper displays in the future. High-performance flexible displays need a thin-film transistor (TFT) backplane. A number of techniques are available for placing silicon transistors on flexible foils. Our own work concentrates on the fabrication *n* and *p* channel TFTs from silicon deposited on foil substrates of steel or organic polymers ("plastics").

2. Silicon for thin-film transistors

TFT grade silicon can be made on foil substrates in three ways: (1) direct deposition of the channel semiconductor; (2) deposition of a precursor film followed by crystallization; (3) physical transfer of separately fabricated circuits. Today techniques (1) and (2) are explored seriously for large-area display applications. Table 1 lists the three grades of thin-film silicon that are available for the fabrication of TFT backplanes on foil substrates [1]. Amorphous silicon backplanes can be made on steel [2,3] and plastic [4-11] foil substrates, and have been in development for several years. Nanocrystalline silicon TFTs [12-15] are made at the same low temperatures as a-Si, and can be made with p or n channels. Thus they are capable of CMOS [15], but their device and process technology is immature. Micro (or poly) crystalline silicon provides CMOS with the highest mobilities but requires high-temperature processing [16,17]. Furnace processing is acceptable for steel substrates. Laser crystallization for steel [18] and plastic [19] substrates has been demonstrated. In view of the early stage of silicon TFT technology on foil substrates, and of the still uncertain future of organic and CdSe TFT technologies, considerable opportunities exist for establishing proprietary positions in TFT backplanes.

Table 1. Properties of silicon materials for thin-film transistors on plastic substrates

Attribute	a-Si:H	nc-Si:H	μc-Si
Deposition T (°C)	250	250	150
Highest T process / material (°C)	350 SiN_x	280 n^+	Laser μc-Si
Lowest proc. T (°C)	110	150	Laser
Electron mobility Hole μ (cm^2/Vs)	0.5-1 ~0.01	40 0.2	300 50
Conductivity (S/cm)	10^{-11}	10^{-7}-10^{-3}	10^{-6}
Growth rate (nm/s)	0.1-1	0.1	0.1-1
Gate geometry	Bottom	Top	Top
Gate insulator	SiN_x	SiO_2	SiO_2

3. Foil substrates

Foil substrates may be of plastic or of metal. Table 2 lists properties of typical substrate materials, and Table 3 presents a chart of TFT/substrate compatibility. Because steel foil can be processed up to 1000°C, all conceivable silicon TFT fabrication can be carried out on it, from *a*-Si:H to *μc*-Si like on quartz glass. However, steel is opaque. Plastic foils can be transparent and even clear, but may be processed up to only 100°C or 200°C. Plastic substrates present many new challenges, which have not yet been fully recognized. Nearly arbitrary foil thicknesses can be chosen, with *a*-Si:H TFTs having

Table 2. Substrate materials for silicon thin-film transistors. Crystalline silicon is included for comparison.

Material	Glass	Steel	Organic polymer	Cryst. silicon
Working T (°C)	600	1000	100-250	1100
Young's modulus (GPa)	70	190	0.1 - 5	190
Coeff. thermal exp. (ppm/°C)	5	18	10 - 100	2.4

been fabricated on stainless steel foils as thin as 3 μm. We have found 25-μm thick stainless steel foil and 50-μm thick polyimide foil convenient to work with.

4. Thin-film transistors on steel foil

Steel can be used as substrate for all grades of silicon and all device processes. Steel foils typically come with rolling marks (Figure 1(a)) and need planarization and electrical insulation [2, 16]. Steel substrates can be processed like substrates of quartz glass. a-Si TFT backplanes on steel already have been introduced for electrophoretic displays [3]. Standard microcrystalline (also called polycrystalline) silicon TFTs can be made on steel foil. Fabrication can include ion implantation for self-alignment, and even thermal oxidation for growing the gate dielectric. A complete CMOS technology based on *μc*-Si/steel has been explored. [21]

Table 3. Compatibility of silicon with substrate materials

Substrate material and T limits ⇨ TFT use ⇩	Plastic ≤150°C	Glass ≤600°C	Steel ≤1000°C
Matrix switch (*n* channel)	*a*-Si:H	*a*-Si:H	*a*-Si:H
Matrix switch, and peripheral circuits (*n* and *p* channel)	*nc*-Si:H	*μc*-Si *nc*-Si:H	*μc*-Si *nc*-Si:H

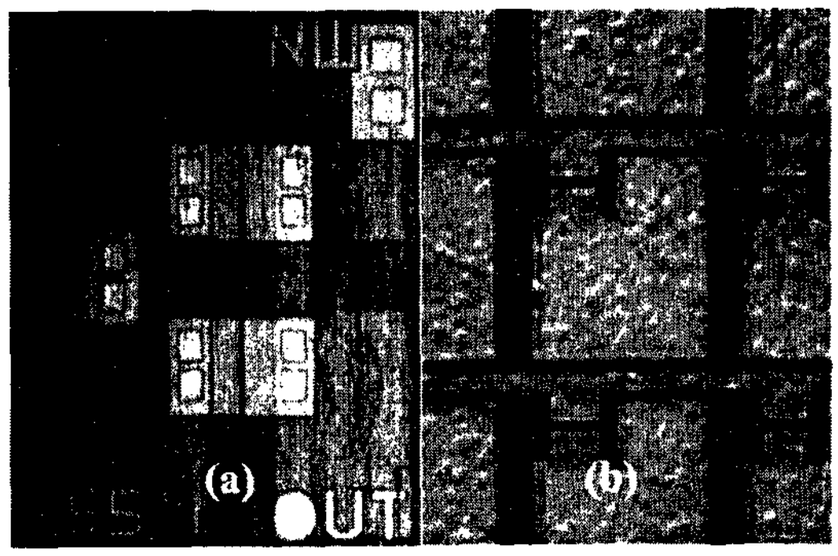

Figure 1. Illustration of surface roughness underneath (a) a CMOS inverter on steel foil (60-μm wide gates) [From ref. 21], and (b) a backplane pixel (50 dpi) on polyimide foil [From ref. 11]

5. Direct deposition of silicon on plastic

The direct deposition of device grade silicon onto plastic brings up many substrate issues: Thermal and chemical stability, high softening or glass transition temperature, high coefficients of thermal and humidity expansion, shrinkage during circuit fabrication, considerable solubility for water, permeability by water and oxygen, film adhesion, and surface roughness [10,11]. The roughness of Kapton E does not seem to impair TFT operation (Fig. 1(b)). Because the criteria for selection of plastic substrates are not sufficiently well defined, at present trial-and-error is best for selecting suitable plastic substrates. We select plastic substrates for (i) high thermal stability, (ii) low coefficient of thermal expansion, and (iii) film adhesion. The first layer to go down is critical as it provides adhesion, planarizes, passivates the substrate against process chemicals, and encapsulates against degassing and contamination. Our standard combination of plastic substrate and encapsulant are the polyimide Kapton and a film of silicon nitride as shown in the schematic cross section of Figure 2 [10].

The direct deposition of both *a*-Si:H and *nc*-Si:H by plasma-enhanced chemical vapor deposition (PE-CVD) can be adapted to T = 150°C. PE-CVD of *a*-Si:H at T = 250°C to 300°C is a well-characterized baseline process and provides reproducible material. The advantage of PE-CVD for the deposition of

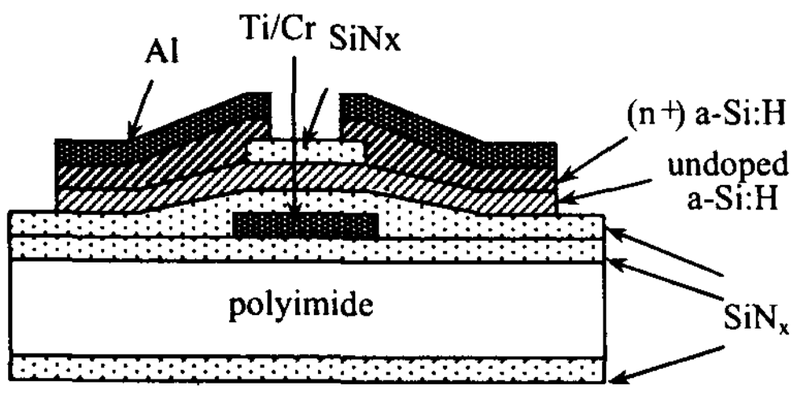

Figure 2. Cross section through an amorphous Si TFT made on SiN passivated polyimide foil [From ref. 10]

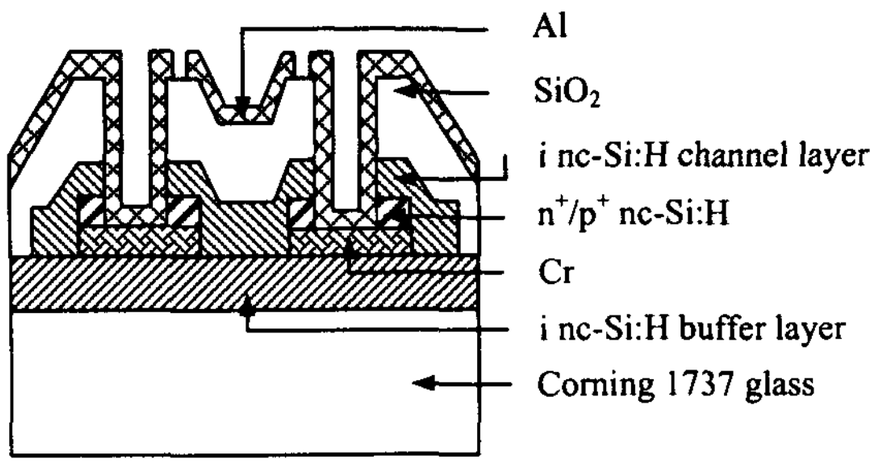

Figure 3. Cross section of a nanocrystalline Si TFT [From ref. 22]

device-grade silicon at 150°C is that it requires only an extension instead of a new deposition technique. This advantage is demonstrated by the field-effect mobilities measured in *a*-Si:H ($\mu_n \cong 0.5$ $cm^2V^{-1}s^{-1}$) and in *nc*-Si:H ($\mu_n \cong 40$ $cm^2V^{-1}s^{-1}$ and $\mu_p \cong 0.2$ $cm^2V^{-1}s^{-1}$) deposited at 150°C.

Lower-temperature processing requires the re-optimiziation of all higher-temperature steps. It is known that the quality of the amorphous silicon (a-Si:H) and silicon nitride (SiN_x) deposited by PECVD deteriorates with decreasing deposition temperature. To overcome this problem the source gases are diluted with hydrogen to ensure that the electronic properties of a-Si:H and SiN_x layers are comparable to those of a-Si:H / SiN_x grown at the optimum temperature of 250-350°C. When a device process is brought from high to low temperature, the most critical re-optimization is that of the highest-temperature process and material. In the a-Si TFT that is the SiN gate dielectric. Device quality SiN_x gate dielectric deposited at the standard temperatures of 300-350°C usually is slightly nitrogen rich. Nitrogen rich SiN_x results in better TFT characteristics and is more stable than silicon-rich SiN_x. Nitrogen rich SiN_x contains a large amount of hydrogen, 20-35 at.%, with the larger fraction bound in N-H groups. The threshold voltage of the TFTs is lowest when the refractive index of the SiN_x layer lies in the range of 1.85 to 1.90. The index of refraction is related to the stoichiometry of the film, being larger for silicon-rich films. Our optimized film has a growth rate of 1.5 Å/s, index of refraction n = 1.80, dielectric constant ε = 7.46, dielectric breakdown field > 3.4 MV/cm, Si/N ratio of 0.67, and H content of ~ $2x10^{22}$ cm^{-3}.

We fabricated arrays of a-Si:H TFTs on 51 μm thick Kapton E at the maximum process temperature of 150°C (Figure 2). First, the polyimide substrate is coated on both sides with a 0.5 μm thick layer of SiN_x. The TFTs have a staggered bottom gate geometry with the channel passivated by SiN_x. All TFTs have the following structure: ~ 100 nm thick Ti/Cr layer as gate electrode, ~ 360 nm of gate SiN_x as gate dielectric, ~ 100 nm of undoped a-Si:H as channel material, 180 nm of passivating SiN_x, ~ 50 nm of (n^+) a-Si:H, and ~ 100 nm thick Al for the source-drain contacts. The stress is optimized in all TFT layers to make the substrate come out flat after fabrication. The cross-sectional view of a-Si:H TFTs is shown in Figure 2. The transistors were annealed after fabrication.

nc-Si:H TFT fabrication needs considerably more research than the 150°C *a*-Si:H TFT technology, which is ready for scale-up. Clearly, the top-gate geometry (Figure 3) produces the highest mobilities. But the *nc*-Si:H growth schedule (direct or pre-nucleation), the location of source/drain contacts (in-plane or staggered), efficient source/drain doping (particularly *p*+), the type of gate dielectric (SiO_2 or SiN_x), and techniques for post-process annealing are not settled. All TFT technologies for plastic (silicon, organics, CdSe) share the same need for a high-quality gate dielectric made at ultra-low temperature. The gate dielectric will remain at the focus of research for some time to come, regardless of the type of semiconductor used for the channel.

6. Flexing and shaping the TFT backplane

Especially when made on compliant plastic substrate foils, *a*-Si:H TFTs become surprisingly inert to bending. They can continue to operate at bending

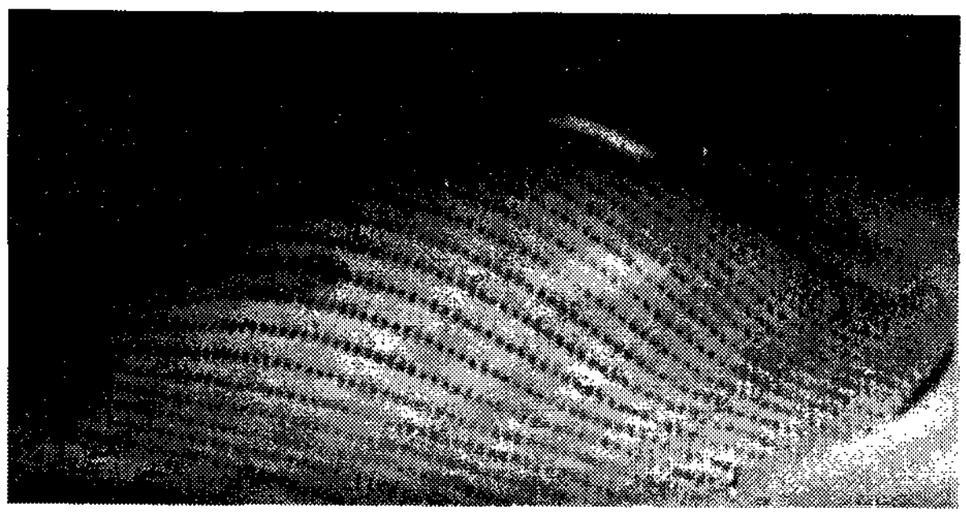

Figure 4. a-Si islands on a spherically deformed polyimide foil. The dome is 6 cm wide.

[From ref. 23]

radii as sharp as 1 mm. The elastic deformation that accompanies bending slightly raises μ_n in tension and reduces μ_n in compression. The transistors fail electrically when one of their layers fractures under mechanical stress. The fracture mechanisms are different for tensile and compressive stresses, and fracture occurs more readily under tension. It is possible to shape TFT backplanes permanently by plastic deformation (Figure 4) [23]. The principle is to build TFTs on islands of a size and thickness such that most strain is diverted to the inter-island regions of the compliant substrate. Then the TFT islands experience only subcritical strain during and after deformation of the backplane from planar to non-planar shape. Techniques for interconnecting these islands on non-planar substrates are under research [24].

7. Outlook

The field of flexible and conformal TFT backplanes is only at its beginning. During the next few years we will see considerable technological innovation in this part of display research and development. Flexibility will be relatively easy to achieve once the fabrication of TFTs on foil substrates has been developed. However, ultralow temperature TFT process steps are posing considerable challenges. Backplanes conformally shaped to fit arbitrary surfaces require new concepts for the placement of circuits, and for the structure and fabrication of interconnects and barrier layers.

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